

NPN 3.5 GHz wideband transistor

T-33-05

BFR95

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DESCRIPTION

NPN resistance-stabilized transistor in a SOT5 (TO-39) metal envelope, with collector connected to the case.

The transistor features low cross modulation, intermodulation and second order intermodulation distortion. Due to its high transition frequency, it has a high power gain combined with excellent wideband properties and low noise up to high frequencies.

It is primarily intended for CATV and MATV applications.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector

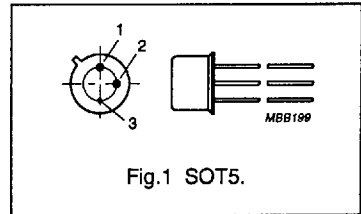


Fig.1 SOT5.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	30	V
V_{CEO}	collector-emitter voltage	open base	–	25	V
I_C	DC collector current		–	150	mA
P_{tot}	total power dissipation	up to $T_s = 125\text{ °C}$ (note 1)	–	1.5	W
f_T	transition frequency	$I_C = 80\text{ mA}$; $V_{CE} = 20\text{ V}$; $f = 500\text{ MHz}$; $T_j = 25\text{ °C}$	3.5	–	GHz
F	noise figure	$I_C = 80\text{ mA}$; $V_{CE} = 18\text{ V}$; $f = 200\text{ MHz}$; $T_{amb} = 25\text{ °C}$	9	10	dB
d_{im}	intermodulation distortion	$I_C = 80\text{ mA}$; $V_{CE} = 18\text{ V}$; $R_L = 75\text{ }\Omega$; $T_{amb} = 25\text{ °C}$; $V_O = 60\text{ dBmV}$; $f_{(p+q-r)} = 194.25\text{ MHz}$	–64	–	dB
d_2	second order intermodulation distortion	$I_C = 80\text{ mA}$; $V_{CE} = 18\text{ V}$; $T_{amb} = 25\text{ °C}$; $V_O = 48\text{ dBmV}$; $f_{(p+q)} = 210\text{ MHz}$	–62	–	dB

Note

- T_s is the temperature at the soldering point of the collector lead.

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LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	-	30	V
V_{CEO}	collector-emitter voltage	open base	-	25	V
V_{CER}	collector-emitter voltage	$R_{BE} = 100 \Omega$	-	35	V
V_{EBO}	emitter-base voltage	open collector	-	3	V
I_C	DC collector current		-	150	mA
I_{CM}	peak collector current	$f > 1 \text{ MHz}$	-	300	mA
P_{tot}	total power dissipation	up to $T_s = 125 \text{ }^\circ\text{C}$ (note 1)	-	1.5	W
T_{stg}	storage temperature		-65	200	$^\circ\text{C}$
T_j	junction temperature		-	200	$^\circ\text{C}$

THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITIONS	THERMAL RESISTANCE
$R_{th j-s}$	thermal resistance from junction to soldering point	up to $T_s = 125 \text{ }^\circ\text{C}$ (note 1)	50 K/W

Note

- T_s is the temperature at the soldering point of the collector lead.

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CHARACTERISTICS

 $T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector cut-off current	$I_E = 0; V_{CB} = 20\text{ V}$	–	–	50	μA
h_{FE}	DC current gain	$I_C = 50\text{ mA}; V_{CE} = 20\text{ V}$	30	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 20\text{ V}$	30	–	–	
f_T	transition frequency	$I_C = 80\text{ mA}; V_{CE} = 20\text{ V}; f = 500\text{ MHz}$	–	3.5	–	GHz
		$I_C = 150\text{ mA}; V_{CE} = 20\text{ V}; f = 500\text{ MHz}$	–	3.5	–	GHz
C_c	collector capacitance	$I_E = I_B = 0; V_{CB} = 20\text{ V}; f = 1\text{ MHz}$	–	3.5	–	pF
C_{re}	feedback capacitance	$I_C = 10\text{ mA}; V_{CE} = 20\text{ V}; f = 1\text{ MHz}$	–	1.6	–	pF
F	noise figure	$I_C = 80\text{ mA}; V_{CE} = 18\text{ V}; f = 200\text{ MHz}; T_{amb} = 25\text{ °C}$	–	9	10	dB
d_{im}	intermodulation distortion	note 1	–	–64	–	dB
d_2	second order intermodulation distortion	note 2	–	–62	–56	dB

Notes

- $I_C = 80\text{ mA}; V_{CE} = 18\text{ V}; R_L = 75\ \Omega; T_{amb} = 25\text{ °C};$
 $V_p = V_o = 60\text{ dBmV}$ at $f_p = 196.25\text{ MHz};$
 $V_q = V_o - 6\text{ dB}$ at $f_q = 203.25\text{ MHz};$
 $V_r = V_o - 6\text{ dB}$ at $f_r = 205.25\text{ MHz};$
measured at $f_{(p+q-r)} = 194.25\text{ MHz}.$
- $I_C = 80\text{ mA}; V_{CE} = 18\text{ V}; T_{amb} = 25\text{ °C};$
 $f_p = 66\text{ MHz}; f_q = 144\text{ MHz}; f_{(p+q)} = 210\text{ MHz}; V_o = 48\text{ dBmV}.$