BGF109

10 Channel LCD Filter Array with ESD Protection

Small Signal Discretes

Never stop thinking

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BGF109

Revision History: 2008-02-11, V2.1

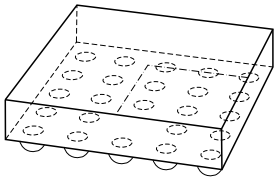
Previous Version: 2007-09-17, V2.0

Page	Subjects (major changes since last revision)
7	**Figure 6** with edge tolerances
7	**Figure 7** updated cavity size

10 Channel LCD Filter Array with ESD Protection

Feature

- 10 channel integrated RC filter array
- ESD protection according to IEC61000-4-2 up to 15 kV contact discharge on all IOs
- Wafer Level Package with SnAgCu solder balls
- RoHS and WEEE compliant package



WLP-24-6

RoHS

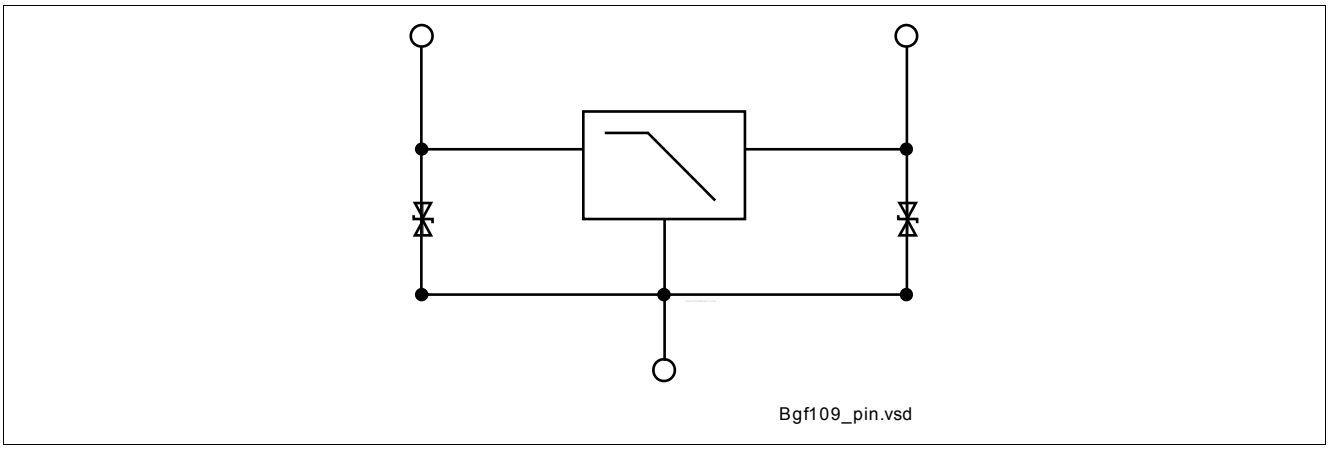


Figure 1 Blockdiagram

Description

The BGF109 is a 10 channel RC filter array to provide attenuation of undesired signals in the 800 - 2000 MHz range. All pins are protected against ESD up to 15 kV according to IEC61000-4-2 (contact discharge). The wafer level package is a green package with a size of only 1.95 mm x 2.07 mm and a total height of 0.60 mm.

Type	Package	Marking	Chip
BGF109	WLP-24-3 / WLP-24-6	BGF109	N0716

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_P	-7		7	V	
Operating temperature range	T_{OP}	-40		+85	°C	
Storage temperature range	T_{STG}	-65		+150	°C	
Summed up input power for all pins	P_{IN}			60	mW	T_S < 70 °C
Electrostatic discharge according to IEC61000-4-2[1)] at all pins	V_E	-15		15	kV	

1) Contact discharge

Table 2 Electrical Characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Series Resistors R_1... R_{10}	R	56	70	84	Ω	
Line capacitance of each line to GND	C_T		28 17	30	pF	V_R = 0 V V_R = 3 V
Leakage currents of lines to GND	I_R			100	nA	V_R = 3 V

1) at T_A = 25 °C

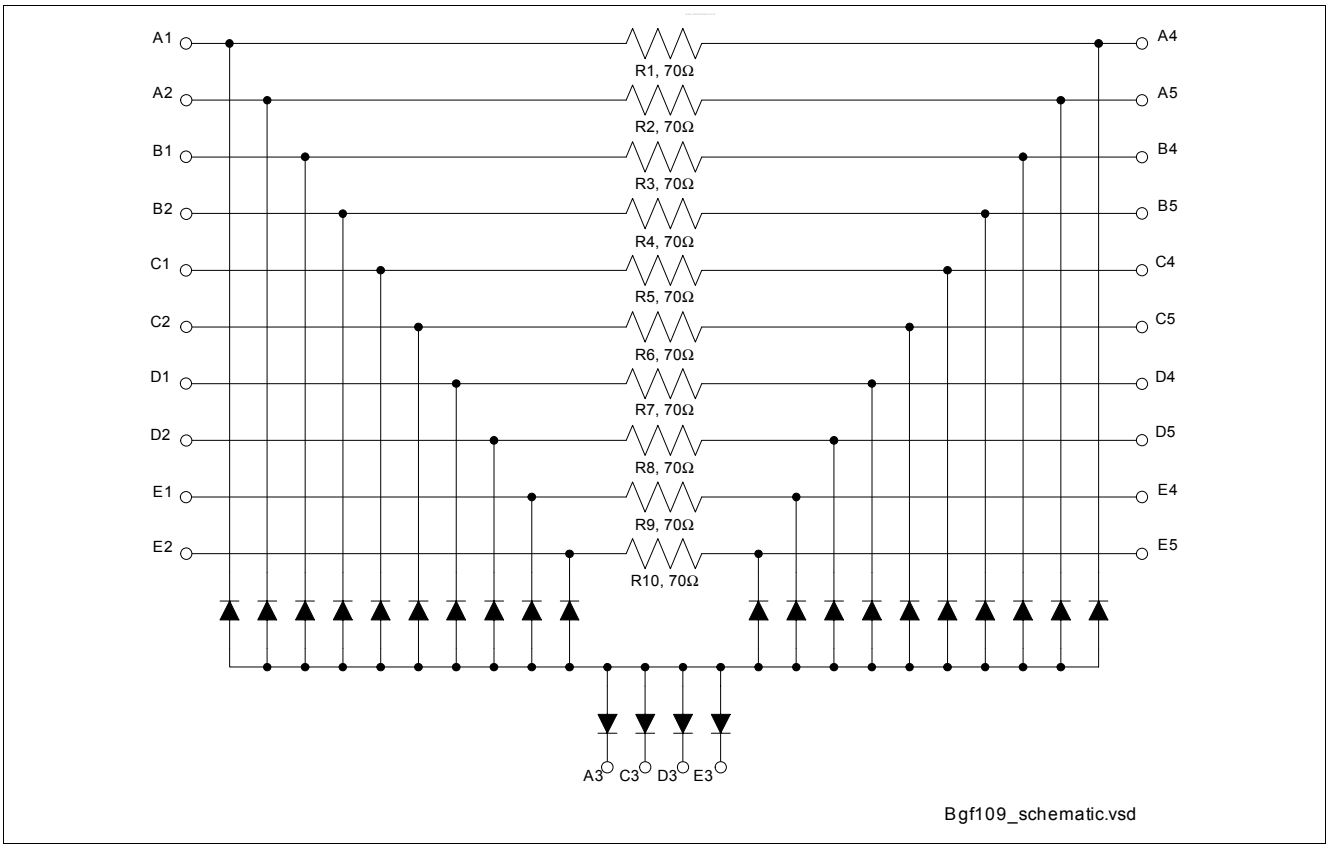


Figure 2 Schematic

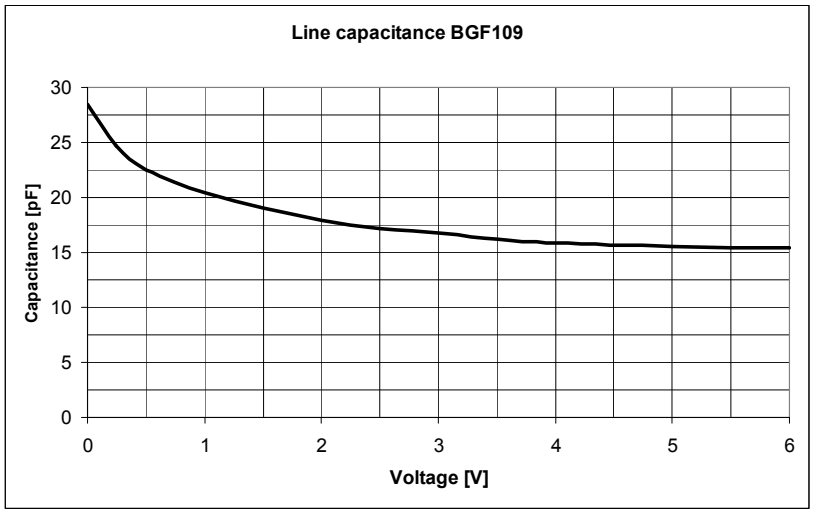


Figure 3 Capacitance of one line to GND versus DC voltage

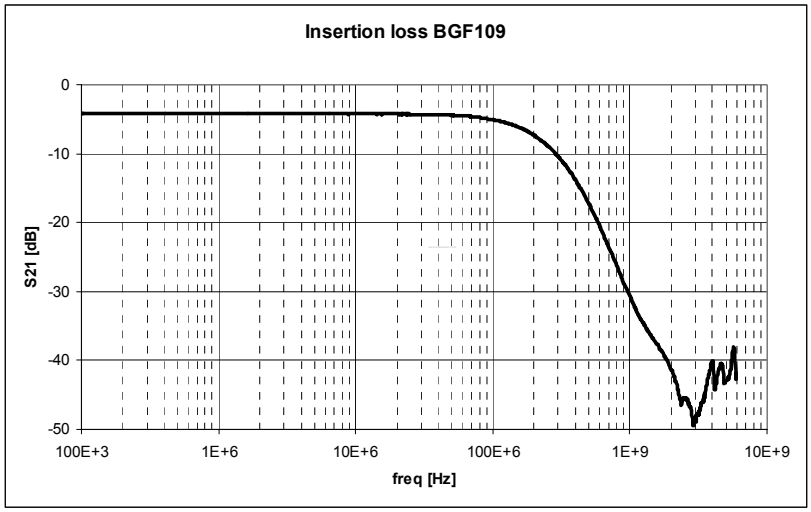


Figure 4 Typical filter characteristics of one filter channel (Z_S = Z_L = 50 Ω, V_R = 0 V)

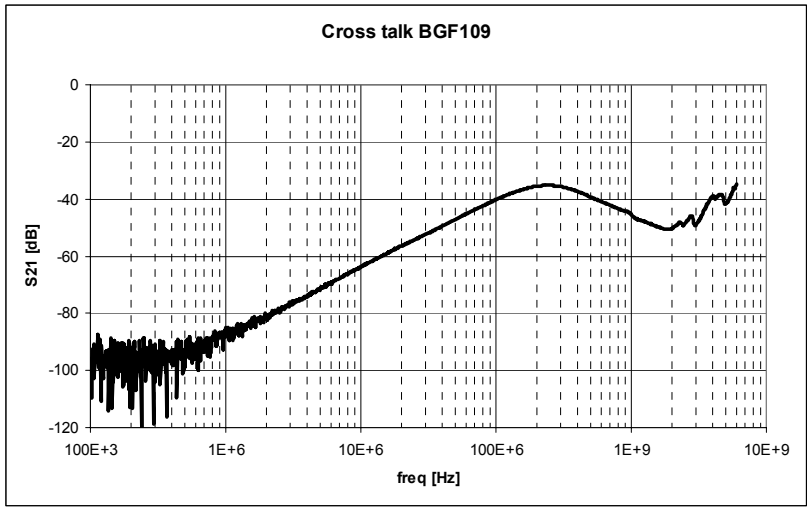
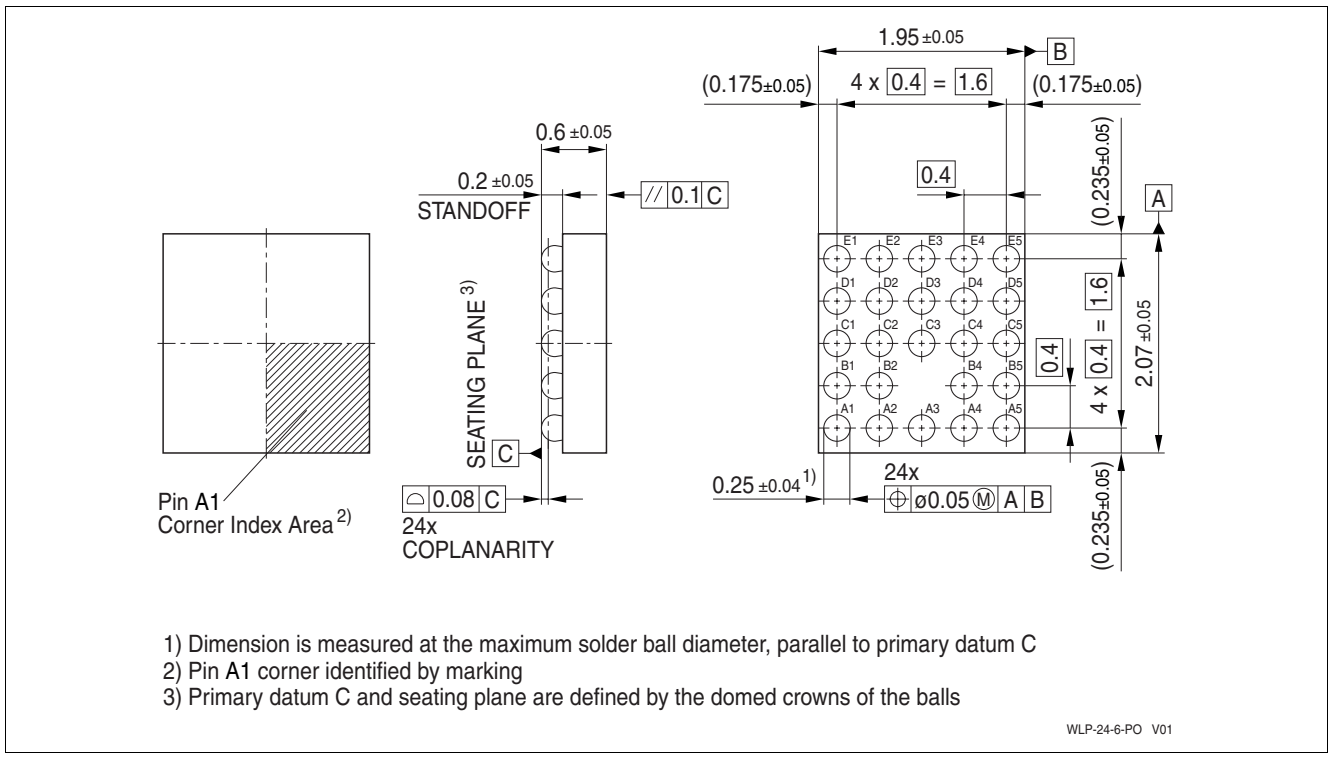


Figure 5 Typical cross talk between two filter channels (Z_S = Z_L = 50 Ω, V_R = 0 V)

Package Outline



1) Dimension is measured at the maximum solder ball diameter, parallel to primary datum C
2) Pin A1 corner identified by marking
3) Primary datum C and seating plane are defined by the domed crowns of the balls

Figure 6 Package WLP-24-3 / WLP-24-6

Tape and reel specification

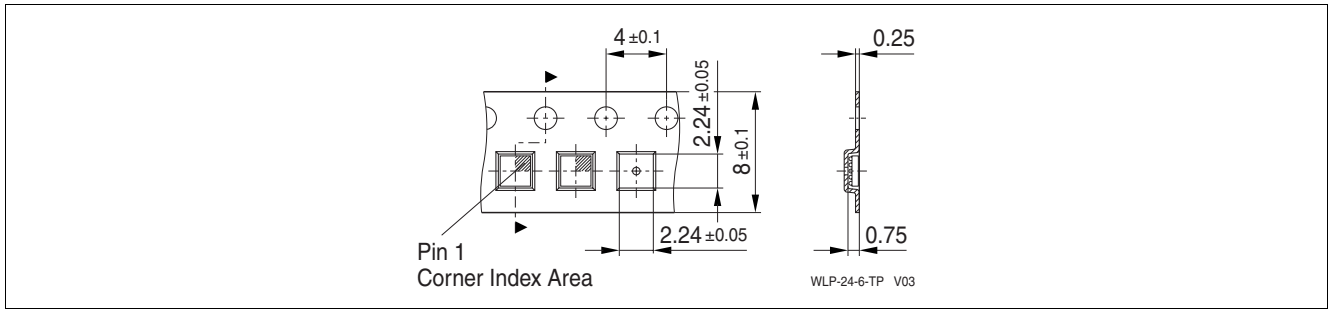


Figure 7 Tape for WLP-24-3 / WLP-24-6