AV I/F Device with ESD Protection

**Small Signal Discretes** 



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# BGF112 AV I/F Device with ESD Protection

BGF112	
Revisio	n History: 2008-11-19, V3.0
Previous	s Version: 2008-10-07, V2.0
Page	Subjects (major changes since last revision)
All	Preliminary status removed



# **BGF112**

#### **Features**

- ESD protection circuit and filter for AV I/F interface
- Integrated ESD protection at external pins of 15 kV contact discharge according to IEC61000-4-2
- · Wafer level package with SnAgCu solder balls
- · RoHS and WEEE compliant package
- 400 μm solder ball pitch



WLP-5-1



## **Description**

BGF112 is an ESD protection circuit and EMI filtering device for an AV I/F interface for mobile applications. The external pins are protected against ESD pulses of 15 kV contact discharge according to IEC61000-4-2. The wafer level package is a green leadfree package with a size of only 0.76 mm x 1.16 mm and a total height of 0.6 mm

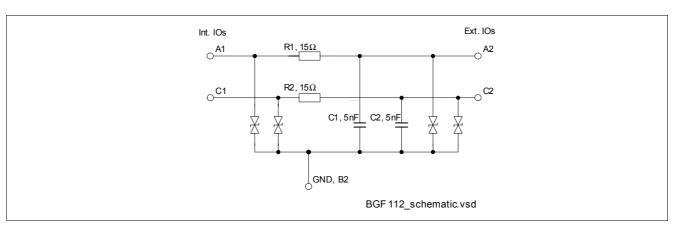


Figure 1 Schematic

Туре	Package	Marking	Chip
BGF112	WLP-5-1	112	N0736

Table 1 Maximum Ratings

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		Test Condition
Voltage at all pins to GND	$V_{P}$	0	_	4	V	_
Operating temperature range	$T_{OP}$	-40	_	+85	°C	_
Storage temperature range	$T_{STG}$	-65	_	+150	°C	_
Power dissipation each line	$P_{in}$	_	_	70	mW	T <sub>S</sub> < 70 °C
Electrostatic Discharge According to IEC6	1000-4-2					
Contact discharge from A2 or C2 to GND	$V_{ESD}$	-15	_	15	kV	_
Contact discharge between all other pins	$V_{ESD}$	-2	_	2	kV	_



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**BGF112** 

Table 2 Electrical Characteristics<sup>1)</sup>

Parameter	Symbol	Values			Unit	Note /
		Min.	Тур.	Max.		<b>Test Condition</b>
Resistors $R_1$ , $R_2$	$R_{1,2}$	13.5	15	16.5	Ω	_
Capacitors C <sub>1</sub> , C <sub>2</sub>	C <sub>1,2</sub>	4	5	6	nF	_
Total ESD junction capacitance of each line to GND	$C_{T}$	_	18	30	pF	V = 0 V
Leakage currents ESD diodes to GND	$I_{R}$	_	0.1 0.1	100 100	nA μA	$V = \pm 3 \text{ V}$ $V = \pm 14 \text{ V}$

<sup>1)</sup> at  $T_{A} = 25 \, ^{\circ}\text{C}$ 



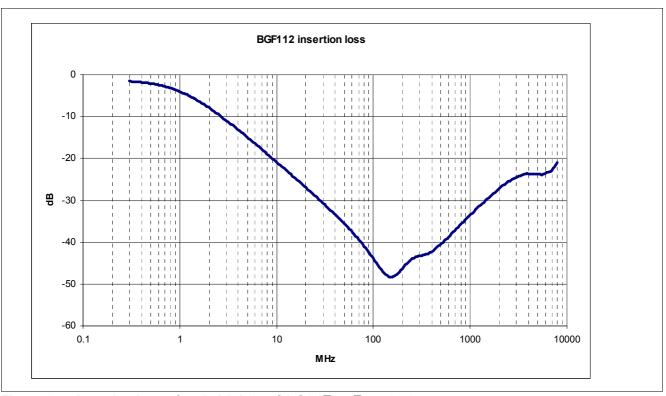


Figure 2 Insertion loss of path A1-A2 or C1-C2 ( $Z_S = Z_L = 50 \Omega$ )

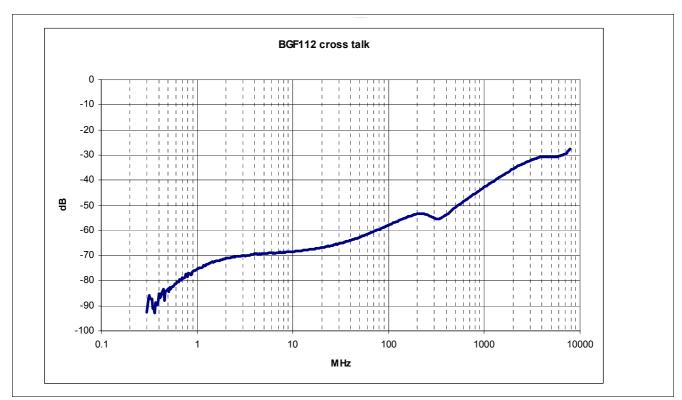


Figure 3 Cross talk of path A1-C2 or C1-A2 ( $Z_S = Z_L = 50 \Omega$ )



# **Package Outlines**

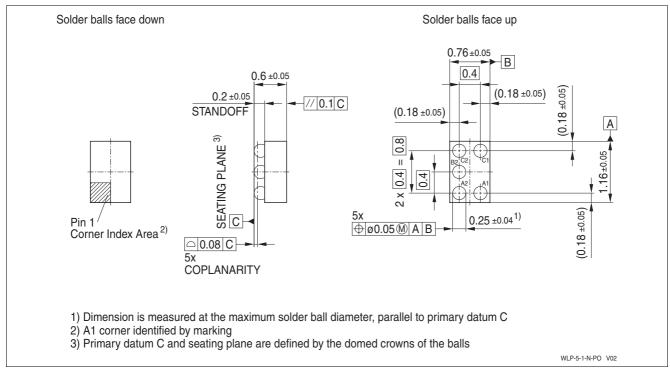


Figure 4 WLP-5-1 (dimensions in mm)

## Tape and reel specification

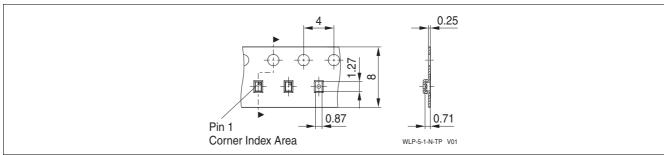


Figure 5 Tape for WLP-5-1 (dimensions in mm)

You can find all of our packages, sorts of packing and others in our Infineon Internet Page "Products": http://www.infineon.com/products

Data Sheet 7 V3.0, 2008-11-19