

BGF148

7 line ESD and EMI interface protection device

BGF148

Datasheet

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Final

Power Management & Multimarket

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Revision History Rev. 1.9.1, 2014-01-17

Page or Item	Subjects (major changes since previous revision)
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Revision 1.9.2, 2014-04-02

5	Table 2-1) updated

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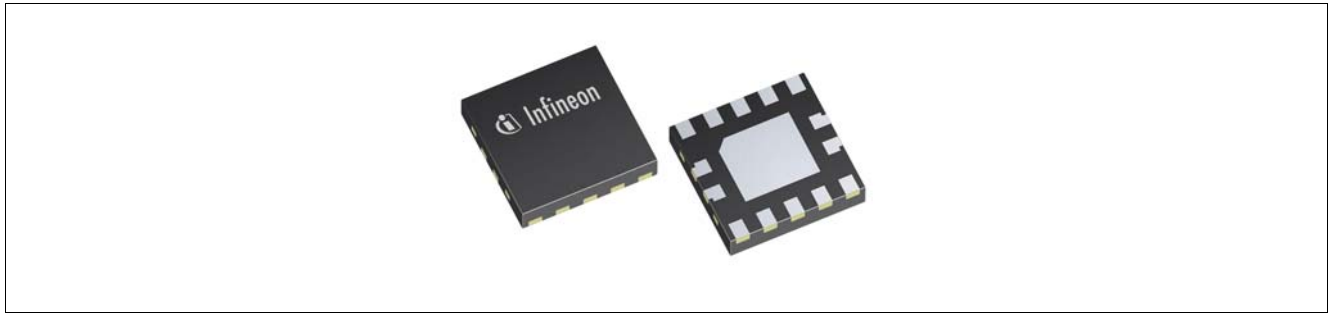
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Last Trademarks Update 2011-11-11

1 7 line ESD and EMI interface protection device

1.1 Features



- 7 line bidirectional ESD protection
- ESD protection according to IEC61000-4-2 for ± 15 kV contact discharge on all external I/Os
- ESD protection according to IEC61000-4-2 for ± 8 kV contact discharge on all internal I/Os
- 6 line pi-type EMI filter for superior EMI filtering and very low cross-talk due to low parasitics
- Suitable for high speed applications due to low line capacitance of typical 1.2 pF
- Very low voltage dependency of line capacitance
- Very low leakage currents
- Application requires very small PCB area using an optimized I/O arrangement
- Small sized Plastic Package with 400 μm pitch
- Pb-free (RoHS compliant) and halogen free package
- Complies with following standards: SD Card Specification V4.1 including UHS104 mode



1.2 Application

- High-Speed Mini-/Micro- SD Card ESD protection and EMI filter
- SD3.0 card Interface (Mini, Micro), down compatible to SD2.0 and lower
 - feature phones, smart phones, tablets, digital still cameras, digital video cameras, computers and other devices using SD card interfaces

1.3 Product Description

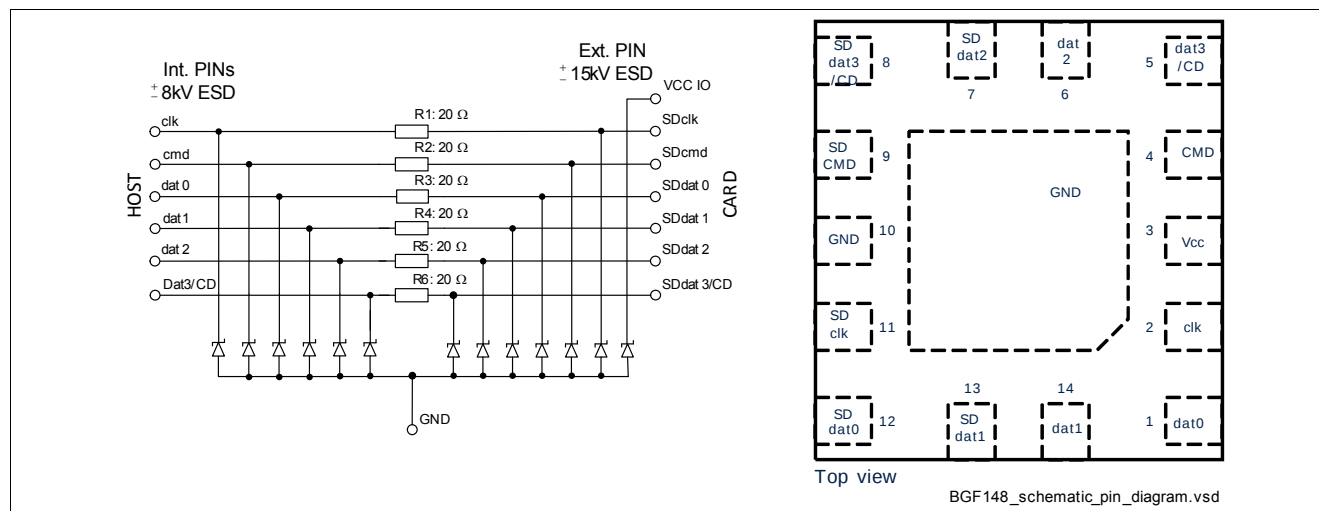


Figure 1-1 Schematic

Type	Package	Marking	Chip
BGF148	TSNP-14-2	48	N0756

2 Electrical Characteristics

2.1 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Voltage at all pins to GND	V_F	0	-	5.5	V	
Operating temperature range	T_{OP}	-40	-	+85	$^\circ\text{C}$	
Storage temperature range	T_{STG}	-65	-	+150	$^\circ\text{C}$	
ESD contact discharge ¹⁾	V_{ESD}	-	-	-	kV	
External IOs		-15		15		
Internal IOs		-8		8		

1) V_{ESD} according to IEC61000-4-2

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.2 Electrical Characteristics

Table 2-2 DC Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistor $R_1...R_6$	$R_1...R_6$	18	20	22	Ω	
Reverse current of ESD diodes	I_R	-	5	100	nA	$V_R = 5.5\text{ V}$
Breakdown voltage of ESD diodes	V_{BR}	-	6.5	-	V	$I_{BR} = 1\text{ mA}$

Table 2-3 RF Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance (Capacitance of each line to GND)	C_L		1.2		pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$

Table 2-4 ESD Characteristics at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾²⁾	V_{CL}	-	8.5	-		$I_{TLP} = 1\text{ A}$
		-	9	-		$I_{TLP} = 16\text{ A}$
Dynamic resistance ¹⁾²⁾	R_{DYN}	-	0.03	-	Ω	

1) Pulse at external pins, measurements at related internal pins

2) ANSI / ESDSTM5.5.1-Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$, I_{TLP} and V_{TLP} average window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 2\text{ A}$ and $I_{TLP2} = 15\text{ A}$. Please refer to Application Note AN210[1]

3 Typical Characteristics

Curves specified at $T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise specified

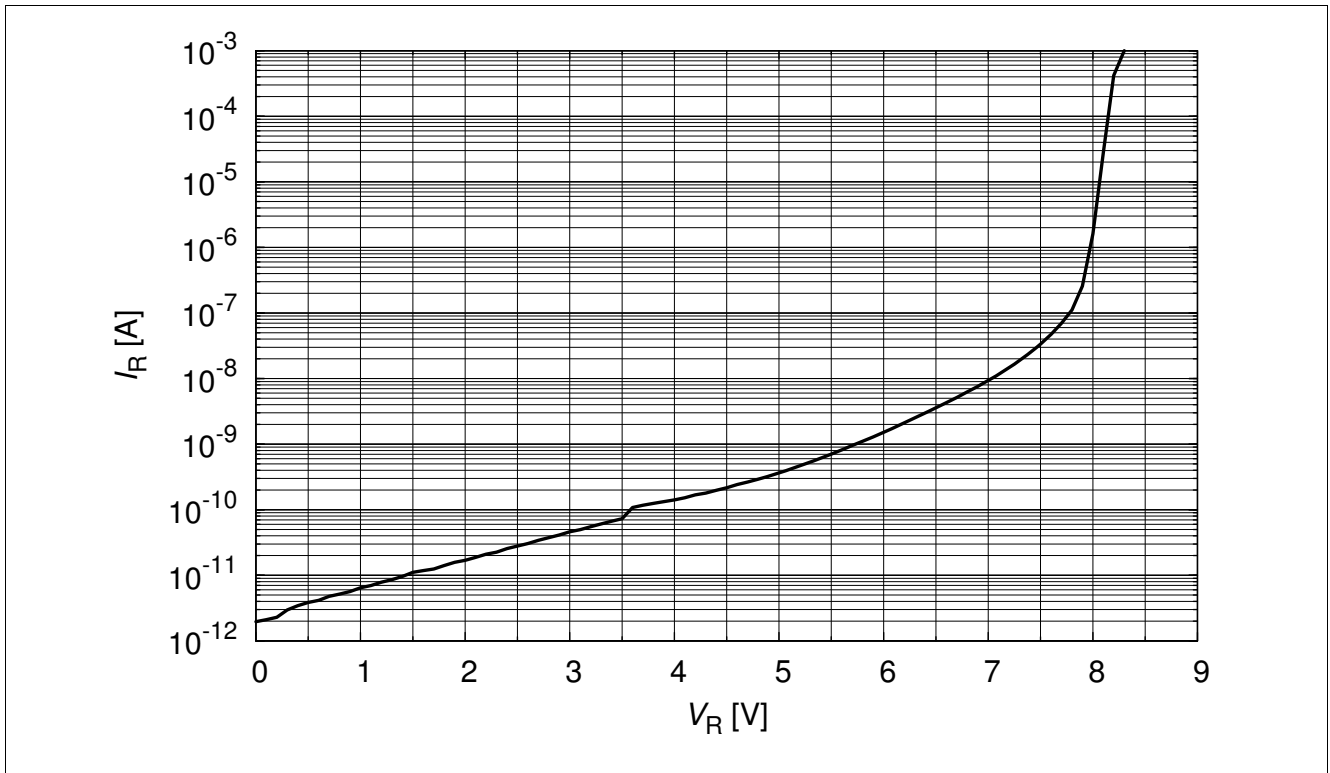


Figure 3-1 Reverse current: $I_R = f(V_R)$

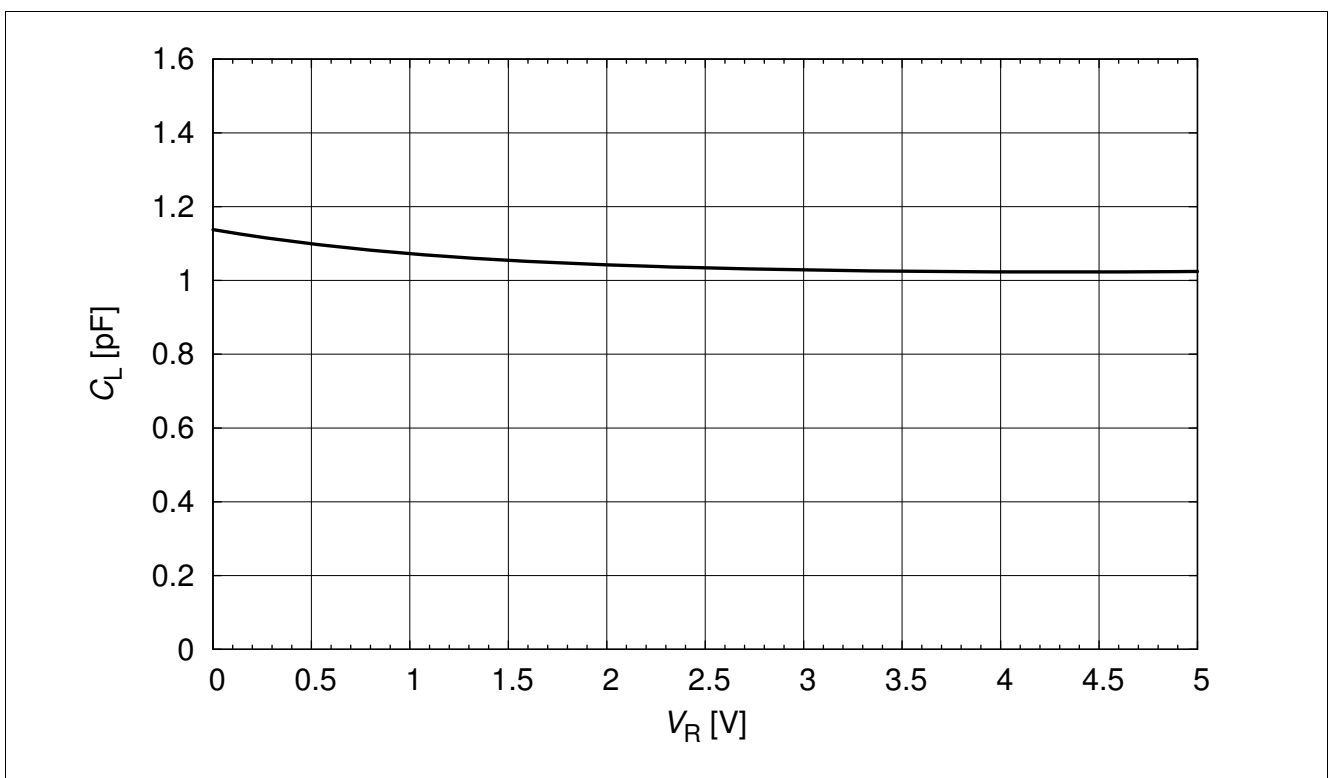


Figure 3-2 Line capacitance of line A1 - A4: $C_L = f(V_R)$, $f = 1\text{ MHz}$

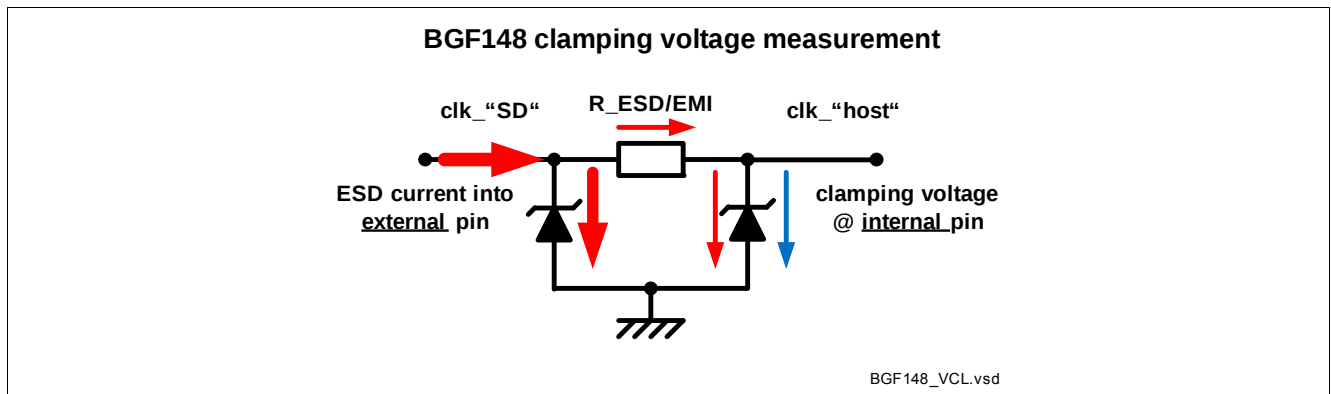


Figure 3-3 Measurement setup for clamping voltage

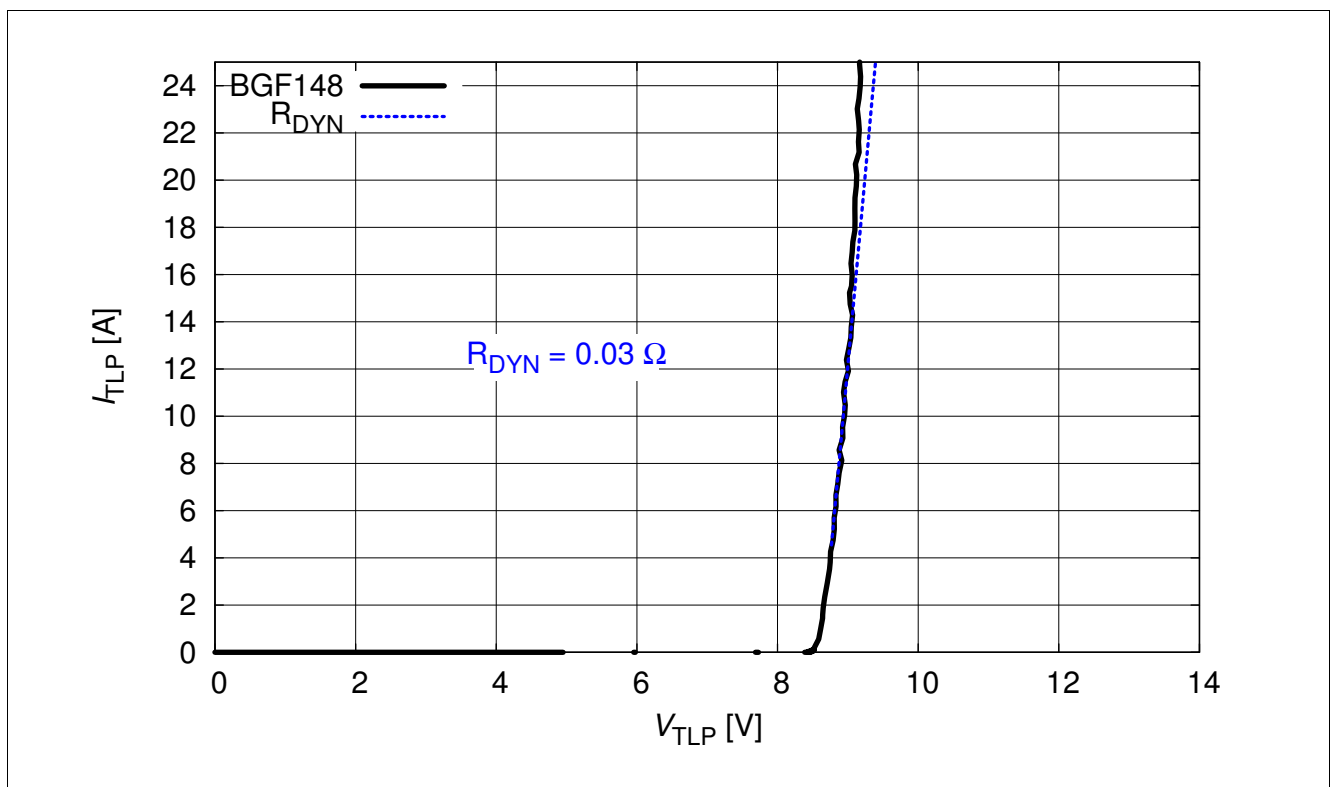


Figure 3-4 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESDSTM5.5.1-Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: $Z_0 = 50 \, \Omega$, $t_p = 100 \, \text{ns}$, $t_r = 0.6 \, \text{ns}$, I_{TLP} and V_{TLP} average window: $t_1 = 30 \, \text{ns}$ to $t_2 = 60 \, \text{ns}$, extraction of dynamic resistance using squares fit to TLP characteristics between $I_{TLP1} = 2 \, \text{A}$ and $I_{TLP2} = 15 \, \text{A}$. Please refer to Application Note AN210[1]

5 Package

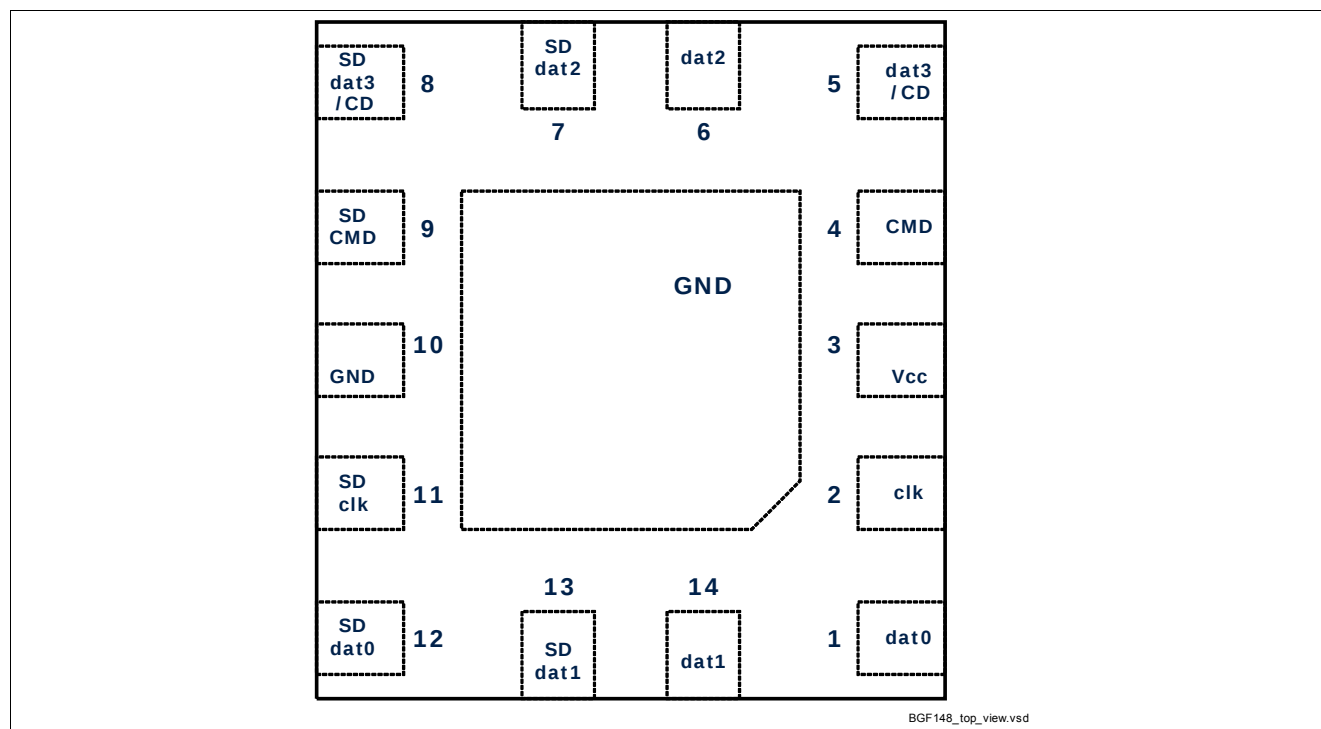


Figure 5-1 Top view through the device

Table 5-1 Pin and Function

Pin #	Function		ESD (IEC61000-4-2, contact discharge)
1	Dat0	Int. PIN	±8 kV
2	Clk	Int. PIN	±8 kV
3	VccIO	Ext. PIN	±15 kV
4	CDM	Int. PIN	±8 kV
5	Dat3/CD	Int. PIN	±8 kV
6	Dat2	Int. PIN	±8 kV
7	SDdat2	Ext. PIN	±15 kV
8	SDdat3/CD	Ext. PIN	±15 kV
9	SDCMD	Ext. PIN	±15 kV
10	GND		
11	SDclk	Ext. PIN	±15 kV
12	SDdat0	Ext. PIN	±15 kV
13	SDdat1	Ext. PIN	±15 kV
14	Dat1	Int. PIN	±8 kV
Center	GND		

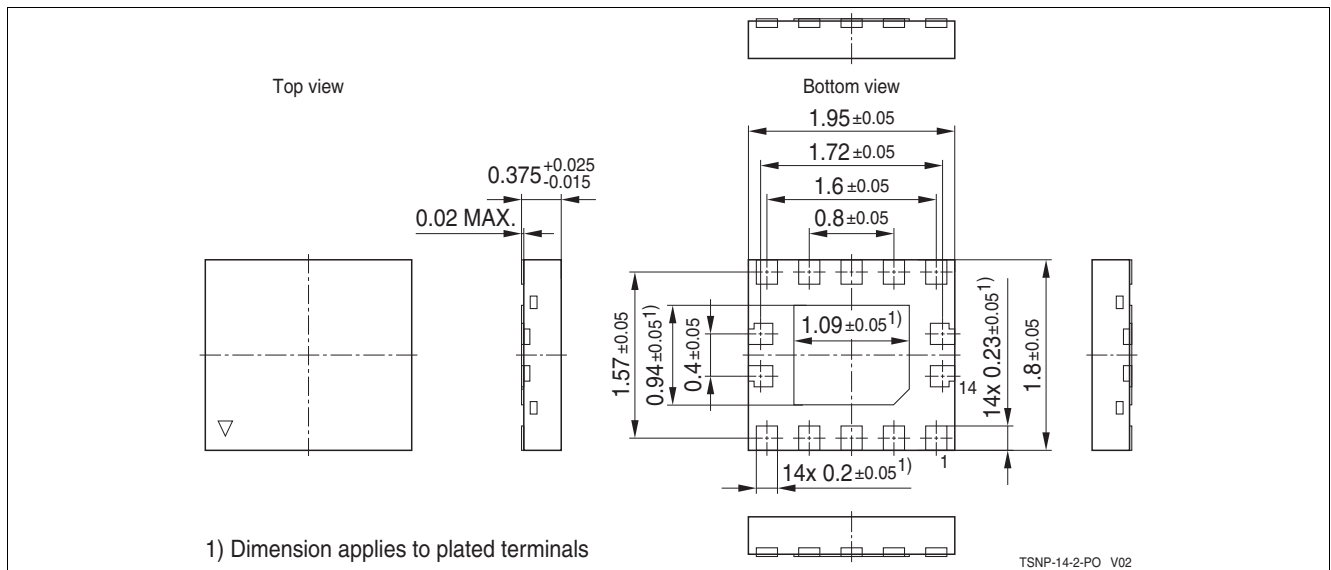


Figure 5-2 Package outline for TSNP-14-2 (dimension in mm)

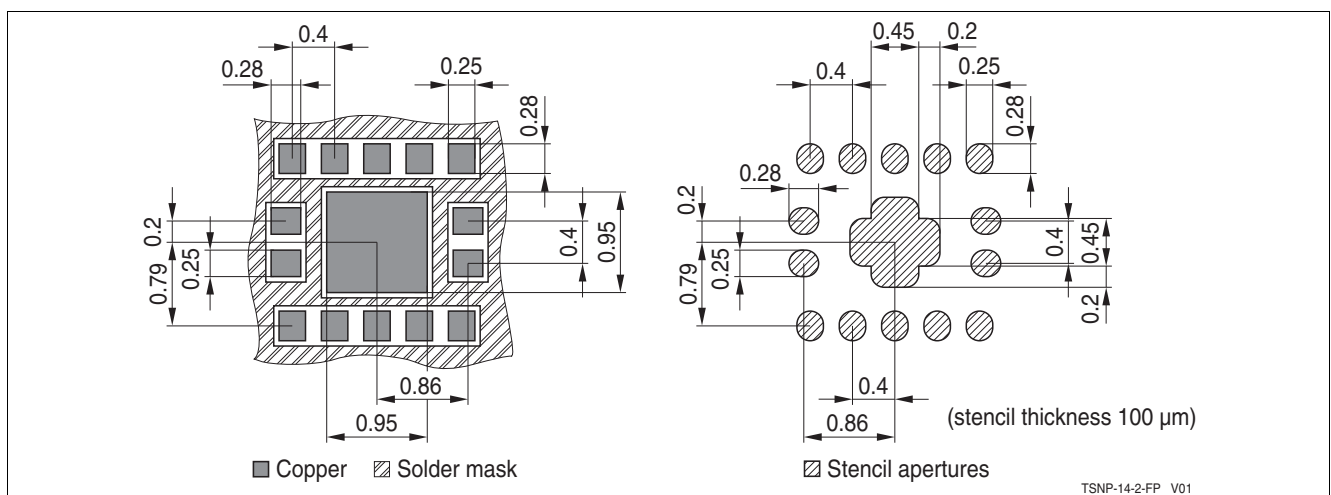


Figure 5-3 Footprint and stencil recommendation for TSNP-14-2

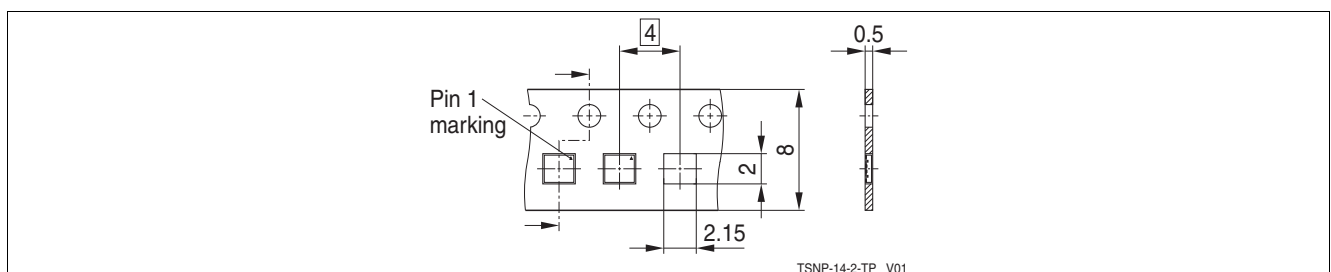


Figure 5-4 Tape (dimension in mm) for TSNP-14-2

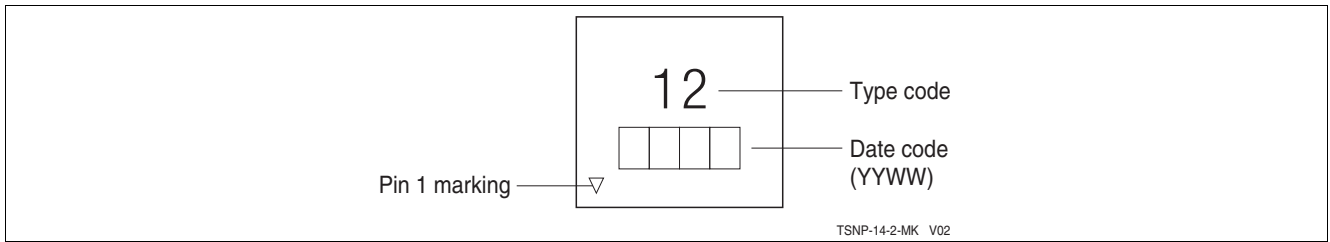


Figure 5-5 Marking example

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

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