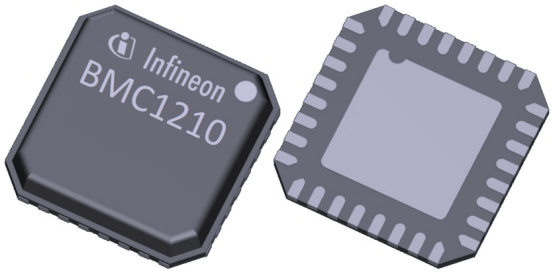
BGMC1210

Power Amplifier Bias and Control IC

Features

- 2x 4 analog outputs with up to 50mA sourcing and 20mA sinking capability
  - 12 Bit DACs with programmable ranges:
    - 0...3.5V and 0...7V
    - bipolar range support: from -7…0V up to 0…7V
  - Programmable offset for range adaption
  - Internal voltage reference
  - Configurable tracking mode
  - Optional temperature compensation of analog outputs via Look-Up Table (LUT)
  - Configurable gate bias compensation
- 2x 2 bias switches for time-division-duplex (TDD) support with configurable clamp voltage:
  - Fixed to VREF
  - Neighbouring DAC (tracking opt.)
  - Tracking clamping DAC
- 2x Current Shunt ADC
  - 12 Bit SD ADC with internal reference
  - Programmable Full-Scales: 15mV, 30mV, 60mV, 120mV, 240mV
  - Offset compensated
  - Floating input stage up to 60V common mode
- Voltage ADC:
  - 11 Bit SAR ADC with internal reference
  - Available Inputs:
    - 2x 60V Full-Scale
    - 2x 3V Full-Scale
    - Supply pins



PG-VQFN-32 5x5mm^2

RoHS Halogen-Free
Green Lead-Free

- Die Temperature Sensor
  - 9 bit resolution
  - Measurement Range: -40°C to 160°C
  - 2.5°C accuracy
  - Can be used for temperature compensation
- I3C Serial Interface with I^{2}C support
  - SDR (12.5MBit/s) and HDR-DDR (25MBit/s) transmission modes supported
  - Device ID selection via 3-state inputs
- Temperature Range (junction): -40°C to 150°C

Potential applications

Cellular Base Stations: Bias & control circuit for power amplifiers

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The BGMC1210 is a bias and control IC for Power Amplifiers (PA) that operate with negative Gate-Source voltages (e.g. GaN) and/or positive Gate-Source voltages (e.g. LDMOS). The BGMC1210 supports up to 2 PAs

Pin Configuration

with 4 DAC outputs per each side of the IC. DACs have a resolution of 12 Bit each, supplied by an internal reference voltage and buffered by an amplifier providing up to 50mA driving current. Block diagram of the BGMC1210 is shown in Figure 1 and simplified typical PA application circuit is shown in Figure 2. The ranges and output voltages can be programmed via an I3C interface, which is backward compatible with I^2C. The DACs are separated into two groups A and B, which can support independent output voltage ranges. Supported output voltage ranges are 0…7 V and 0…3.5 V, which can be offset into negative voltage domain depending on the selected DAC supply voltage for corresponding group at pins VREF_A/VREF_B and VDDA_A/VDDA_B. Thus, four DACs can support positive voltage range of 0…+7V or 0…+3.5V, whereas the other group of four DACs can support negative voltage range of -7…0V or -3.5…0V (or any range in between defined by lower DAC supply voltage at pins VREF_A/VREF_B, such as e.g. -6…+1). On top of that there is an OFFSET parameter, which allows to shift the voltage within the supply range.

Biasing switches for Time-Division-Duplex (TDD) support are present on 2 outputs per side (OUT_xy), directly controlled via dedicated pins EN_OUT_x (x = [A, B]; y = [0, 2]). The grouping of switched outputs by EN_OUT_x inputs can be defined. Clamping voltages for switched outputs can be set to a fixed VREF_x potential, DAC_x1/DAC_x3 output or a dedicated 6-bit clamping DAC voltage.

The output values of the DAC can be configured to compensate the power amplifier temperature drift via a Look-Up Table (LUT) and an integrated temperature sensor.

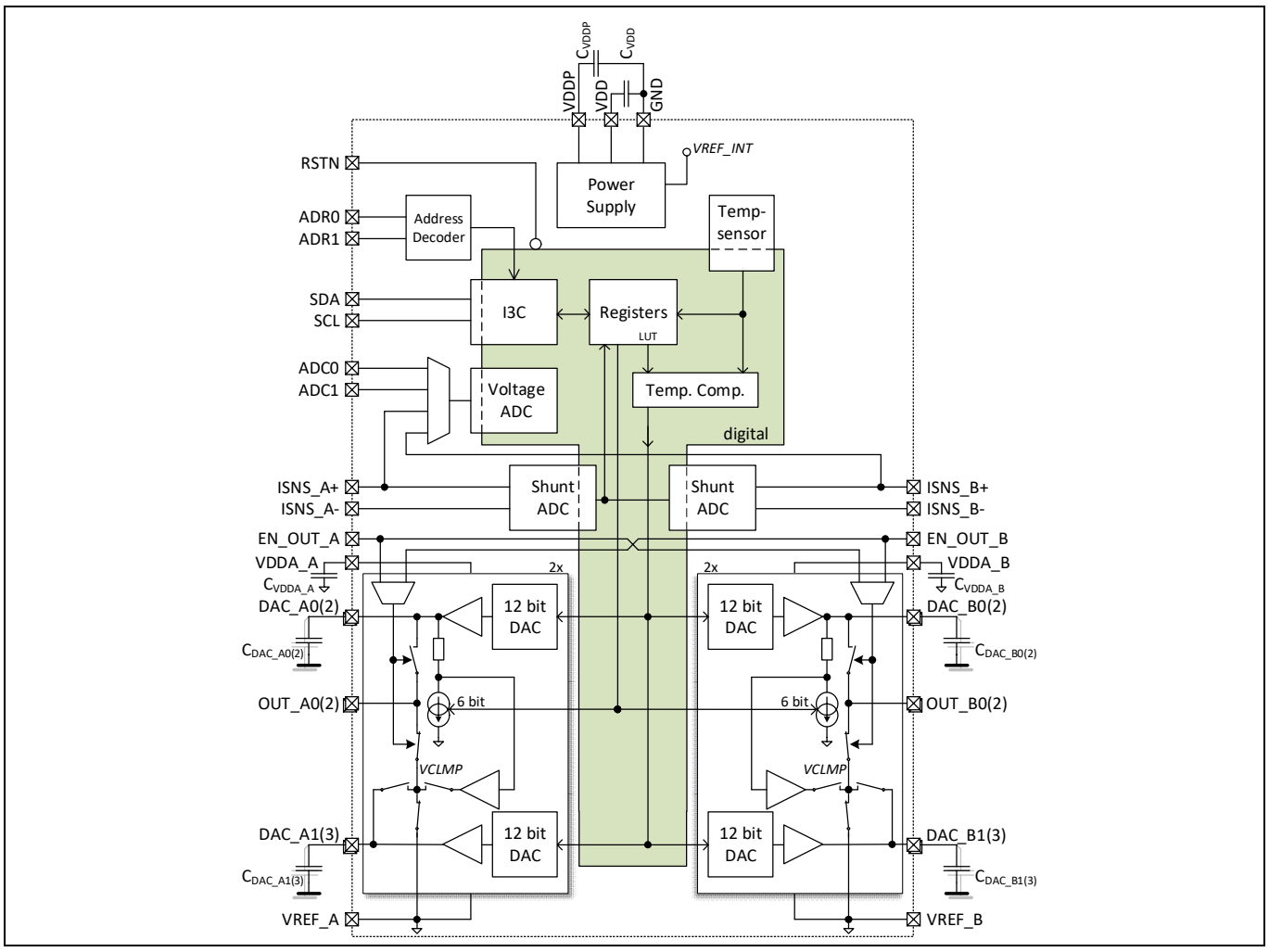


Figure 1 Functional Block Diagram

Pin Configuration

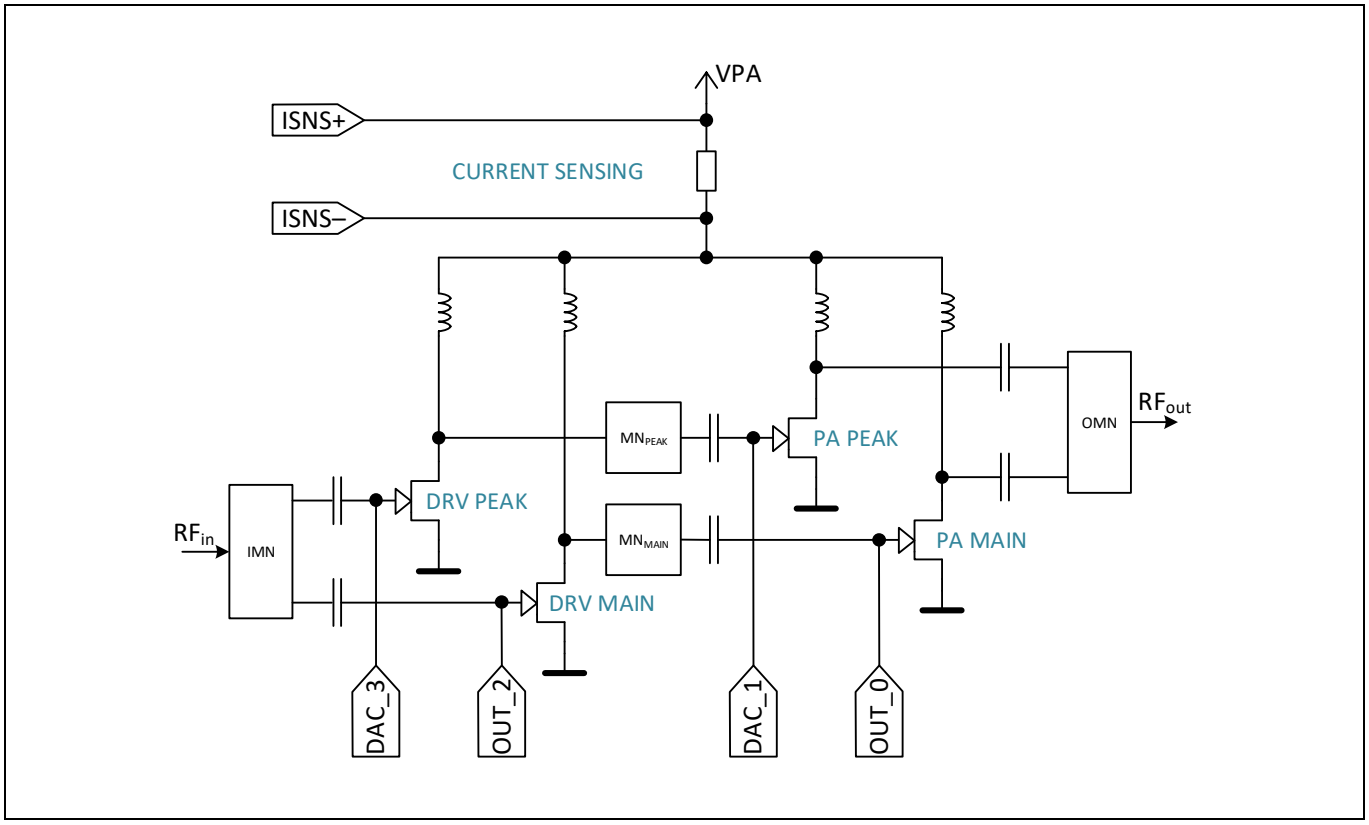


Figure 2 Typical Power Amplifier application circuit

Table of contents

1 Pin Configuration

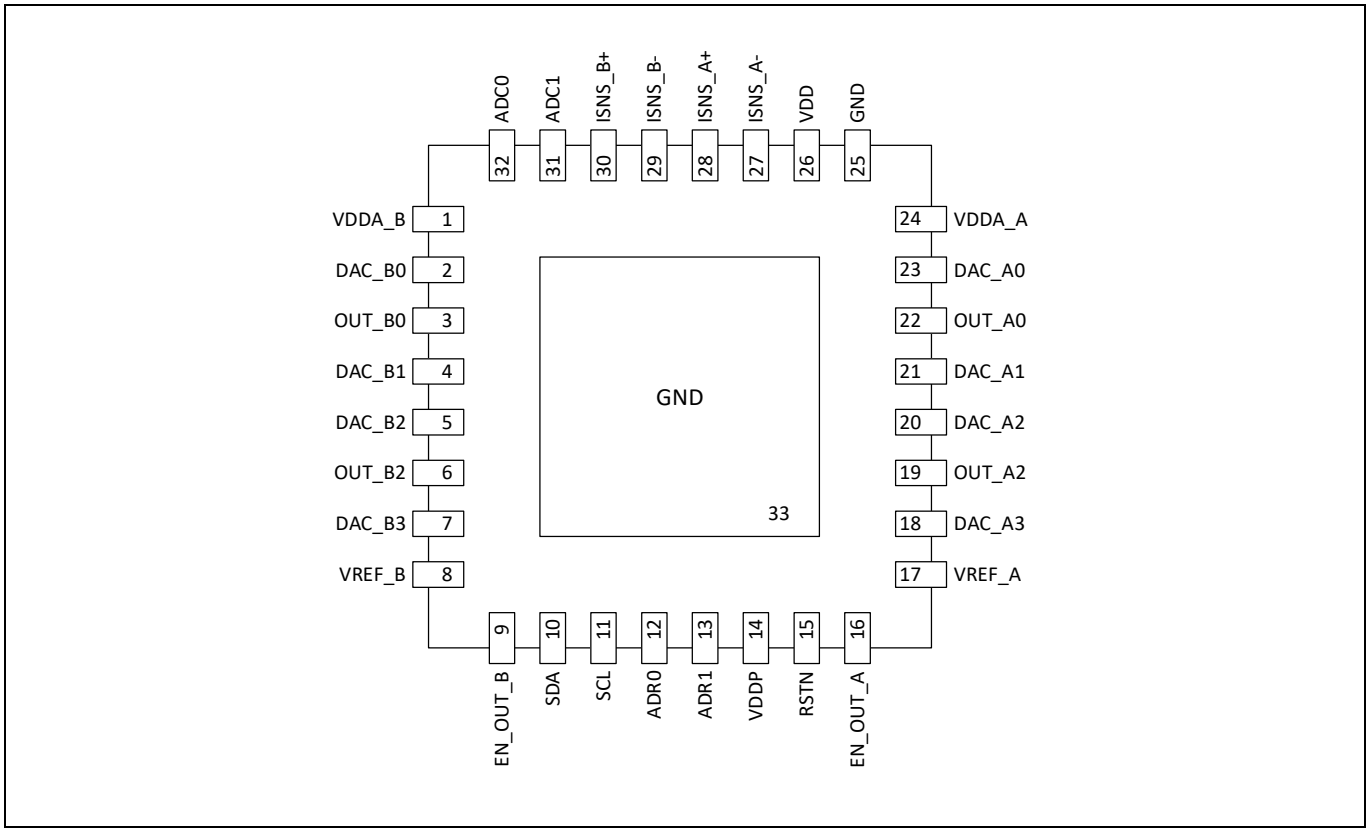


Figure 3 Pin number assignment of BGMC1210

Table 1 Pin definition and function

Pin #	Symbol	Function	Description
1	VDDA_B	SUP	Upper DAC supply voltage; depending on selected DAC output range, connects either to positive supply (positive gate voltages) or GND (negative gate voltages); side B
2	DAC_B0	DAC OUT	DAC out; side B
3	OUT_B0	OUT	Switched bias output; connects to DAC_B0 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_B, DAC_B1 or CLMP DAC based on register configuration; side B
4	DAC_B1	DAC OUT	DAC out; no switching; side B
5	DAC_B2	DAC OUT	DAC out; side B
6	OUT_B2	OUT	Switched bias output; connects to DAC_B2 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_B, DAC_B3 or CLMP DAC based on register configuration; side B
7	DAC_B3	DAC OUT	DAC out; no switching; side B
8	VREF_B	SUP	Lower DAC supply / reference voltage; depending on selected DAC output range, connects either to GND (positive gate voltages) or negative supply (negative gate voltages); side B
9	EN_OUT_B	IN	Switch the configured OUT_xy outputs between DAC_xy and corresponding VCLMP potential (x = [A, B]; y = [0, 2]); side B
10	SDA	IN/OUT	I3C/I²C data
11	SCL	IN	I3C/I²C clock

12	ADR0	IN	I3C/I²C Device ID, bit 0
13	ADR1	IN	I3C/I²C Device ID, bit 1
14	VDDP	SUP	Digital I/O pins supply rail
15	RSTN	IN	Asynchronous reset
16	EN_OUT_A	IN	Switch the configured OUT_xy outputs between DAC_xy and corresponding VCLMP potential (x = [A, B]; y = [0, 2]); side A
17	VREF_A	SUP	Lower DAC supply / reference voltage; depending on selected DAC output range, connects either to GND (positive gate voltages) or negative supply (negative gate voltages); side A
18	DAC_A3	DAC OUT	DAC out; no switching; side A
19	OUT_A2	OUT	Switched bias output; connects to DAC_A2 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_A, DAC_A3 or CLMP DAC based on register configuration; side A
20	DAC_A2	DAC OUT	DAC out; side A
21	DAC_A1	DAC OUT	DAC out; no switching; side A
22	OUT_A0	OUT	Switched bias output; connects to DAC_A0 or VCLMP potential based on the level at configured EN_OUT_x, (x = [A, B]); VCLMP can be defined by VREF_A, DAC_A1 or CLMP DAC based on register configuration; side A
23	DAC_A0	DAC OUT	DAC out; side A
24	VDDA_A	SUP	Upper DAC supply voltage; depending on selected DAC output range, connects either to positive supply (positive gate voltages) or GND (negative gate voltages); side A
25	GND	SUP	Ground connection
26	VDD	SUP	Main supply voltage
27	ISNS_A-	ADC IN	Differential current sensing ADC negative input; side A
28	ISNS_A+	ADC IN	Differential current sensing ADC positive input / Voltage ADC input; side A
29	ISNS_B-	ADC IN	Differential current sensing ADC negative input; side B
30	ISNS_B+	ADC IN	Differential current sensing ADC positive input / Voltage ADC input; side B
31	ADC1	ADC IN	Voltage ADC input 1
32	ADC0	ADC IN	Voltage ADC input 0
33	GND	SUP	Ground connection

2 Absolute Maximum Ratings

Table 2 Absolute Maximum Ratings [1,2]

Parameter	Symbol / Function	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Main supply	VDD	-0.3		5.5	V	
Pad supply	VDDP	-0.3		3.6	V	
Positive DAC supply [3]	VDDA_x	-0.3		8.0	V	
Negative DAC supply/reference [3]	VREF_x	-8.0		0.3	V	
DAC supply [3]	VDDA_x – VREF_x	-0.3		8.0	V	
Digital I/Os	IN/OUT	-0.3		VDDP+0.3	V	
DAC outputs [3]	DAC_xy	VREF_x-0.3		VDDA_x+0.3	V	
Switched outputs [3]	OUT_xy	VREF_x-0.3		VDDA_x+0.3	V	
Voltage ADC inputs	ADC0/1	-0.3		3.3	V	
Current sense inputs [3]	ISNS_x+/-	-0.3		60	V	
Differential current sense input voltage [3]	ISNS_x+ – ISNS_x-	-1		1	V	
Junction temperature	T_J	-40		150	°C	
Storage temperature	T_{STG}	-65		150	°C	

[1] Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[2] All voltages are with respect to GND=0V unless otherwise noted. Currents are positive into and negative out of the specified terminal.

[3] x = [A, B]; y = [0, 1, 2, 3].

3 Specifications

3.1 Operational Ratings

Table 3 Operational Ratings[2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Main supply	VDD	3.1	3.3	5.5	V	
Pad supply	VDDP	1.65	1.80	3.6	V	
Positive DAC supply [1]	VDDA_x	0		8	V	
Negative DAC supply/reference [1]	VREF_x	-8		0	V	
DAC supply [1]	VDDA_x – VREF_x	3.1		8.0	V	
ISNS inputs	ISNS_x+/-	0		60	V	
ISNS input current	$I_{ISNS\_x+/-}$	-120		120	mA	
Ramp rate supply, ISNS inputs	V_{ramp}			10	V/us	
Junction temperature	T_J	-40		150	°C	

[1] x = [A, B].

[2] All voltages are with respect to GND=0V unless otherwise noted.

3.2 ESD Ratings

Table 4 ESD Ratings[1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
ESD robustness on all pins, Human Body Model (HBM) sensitivity as per ANSI/ESDA/JEDEC JS-001	V_{HBM}	-2		+2	kV	
ESD robustness on all pins, Charged Device Model (CDM) sensitivity as per ANSI/ESDA/JEDEC JS-002	V_{CDM}	-0.5		+0.5	kV	

[1] All voltages are with respect to GND=0V unless otherwise noted.

3.3 External components

Table 5 External components

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DAC load capacitance [1]	C_{DAC_xy}	30 [2] / 100	1000	1200 [3]	nF	
VDD buffer capacitor	C_{VDD}		100		nF	
VDDP buffer capacitor	C_{VDDP}		100		nF	
VDDA_x-VREF_x buffer capacitance [1]	C_{VDDA_x}		1000		nF	Connected between VDDA_x and VREF_x

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
OUT load capacitance for VCLMP buffer usage [1]				5	nF	Maximum load capacitance for VCLMP buffer; VCLMP_x.SET_xy = 10_b or 11_b
VADC input buffer capacitance	$C_{ADC0/1}$		10		nF	Noise filter

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] Lower capacitance value is only valid if the load (DACCNF2.LD_xy) is configured to “low capacitance”.

[3] Maximum capacitance value can be exceeded (up to 15 µF), but a sequential turn-on or a slow DACCNF1.SLP setting of the DACs is recommended in this case to avoid overheating.

3.4 Thermal information

Table 6 Thermal resistance

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Thermal resistance between junction and bottom pad	Rth_B		2.64		K/W	
Thermal resistance between junction and package top	Rth_T		35.4		K/W	

3.5 Electrical characteristics

3.5.1 Gate biasing

Table 7 Electrical characteristics of gate biasing [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
GATE BIASING DAC						
DAC resolution	RES_{DAC}		12		bits	
DAC full-scale range “low”	FSR_{low}		3.5		V	Referred to VREF_x, RNG=’0’ [1]
DAC full-scale range “high”	FSR_{high}		7		V	Referred to VREF_x, RNG=’1’ [1]
DAC gain error	Eg_{DAC}	-3		+3	%FSR	
DAC differential non-linearity	DNL_{DAC}	-1.0		1.5	LSB	Monotonic
DAC temperature stability	dV_{DAC}/dT			0.3	mV/K	
DAC source current	I_{src}	10			mA	Current flowing out of pins, DAC_xy < VDDA_x – 0.2V [1]
DAC source current “high”	$I_{src,hi}$	50			mA	Current flowing out of pins, high current mode enabled, DAC_xy < VDDA_x – 1.0V [1]
DAC sink current	I_{snk}	8			mA	Current flowing into pins, DAC_xy > VREF_x + 0.7V [1]
DAC sink current “high”	$I_{snk,hi}$	20			mA	Current flowing into pins, high current mode enabled, DAC_xy > VREF_x + 1.0V [1]
DAC source current limitation	$I_{src,lim}$		20		mA	Current flowing out of pins, DAC_xy < VDDA_x – 0.2V [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DAC source current limitation, “high”	$I_{src,lim,hi}$		70		mA	Current flowing out of pins, high current mode enabled, DAC_xy < VDDA_x – 1.0V [1]
DAC sink current limitation	$I_{snk,lim}$		13		mA	Current flowing into pins, DAC_xy > VREF_x + 0.7V [1]
DAC sink current limitation, “high”	$I_{snk,lim,hi}$		30		mA	Current flowing into pins, high current mode enabled, DAC_xy > VREF_x + 1.0V [1]
DAC static load regulation	dV_{DAC}/dI_{DAC}	0.0	0.7	1.9	mV/ mA	VREF_x + 1V < V_{DAC} < VDDA_x - 1V [1]
BIAS SWITCHES						
OUT transmission resistance	R_{trans}		3.5	5	Ω	OUT_xy is connected to DAC_xy, DAC_xy > VREF_x + 1.5V, I_{DC} = 10mA [1]
OUT transmission resistance variation over Temperature	dR_{trans}/dT			12	mΩ/ K	OUT_xy is connected to DAC_xy, DAC_xy > VREF_x + 1.5V, I_{DC} = 10mA [1]
OUT clamping resistance	R_{clamp}			15	Ω	OUT_xy is connected to VREF_x, I_{DC} = 10mA [1]
OUT transient peak current	$I_{OUT,peak}$	-200		200	mA	for pulses shorter than 100 ns
CLAMP DAC (DAC enabled)						
CLAMP DAC resolution	RES_{CLMP}		6		bit	
CLAMP DAC full scale range	FSR_{CLMP}		1.42		V	referred to DAC_x0(2) [1]
CLAMP DAC LSB size	LSB_{CLMP}		22.5		mV	
CLAMP DAC gain error	Eg_{CLMP}	-5		5	%FSR	I_{OUT_xy} = 0mA [1]
CLAMP DAC sink current	$I_{CLMPsnk}$			30	mA	OUT_xy > VREF_x + 1.5V [1]
CLAMP DAC current limitation	$I_{CLMPsnk,lim}$		50		mA	
CLAMP DAC static load regulation	dV_{CLMP}/dI_{CLMP}			15	mV/ mA	EN_OUT_x = 0, $I_{OUT,snk}$=0…20mA, OUT_xy > VREF_x + 1.5V [1]
CLAMP DAC disabled/unsupplied						
CLMP DAC sink current	$I_{CLMPsnk\_dis}$	12	25		mA	OUT_xy > VREF_x + 2V [1]

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.2 Supply monitoring

Table 8 Electrical characteristics of supply monitoring [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VDD UVLO release	$UVLO_{VDD,rel}$	2.6	2.8	3	V	
VDD UVLO lock	$UVLO_{VDD,lck}$	2.5	2.7	2.9	V	
VDD UVLO hysteresis	$UVLO_{VDD,hys}$		100		mV	
VDDA_x-VREF_x UVLO release [1]	$UVLO_{VDDA-VREF,rel}$	2.6	2.8	3	V	
VDDA_x-VREF_x UVLO lock [1]	$UVLO_{VDDA-VREF,lck}$	2.5	2.7	2.9	V	
VDDA_x-VREF_x UVLO hysteresis [1]	$UVLO_{VDDA-VREF,hys}$		100		mV	
VDDP UVLO release	$UVLO_{VDDP,rel}$	1.50	1.55	1.60	V	
VDDP UVLO lock	$UVLO_{VDDP,lck}$	1.45	1.50	1.55	V	
VDDP UVLO hysteresis	$UVLO_{VDDP,hys}$	30	50	70	mV	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.3 Temperature sensor

Table 9 Electrical characteristics of temperature sensor [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
DTS resolution	RES_{DTS}		9		bits	
DTS measurement range	RNG_{DTS}	-40		160	°C	
DTS absolute error	E_{DTS}	-2.5		2.5	°C	

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.4 Voltage ADC

Table 10 Electrical characteristics of VADC [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VADC resolution	RES_{VADC}		11		bit	
VADC full-scale range ADC0/1	$FSR_{VADC,ADC}$		3.07		V	
VADC full-scale range ISNS_x+ [1]	$FSR_{VADC,ISNS}$		61.46		V	ISNS voltages must not exceed ISNS_x+/- = 60 V
VADC differential non-linearity	DNL_{VADC}	-1		2	LSB11	
VADC gain error ADC0/1	$Eg_{VADC,ADC}$	0		1.5	%	

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VADC gain error ISNS_x+[1]	$Eg_{VADC,ISNS}$	0		2.0	%	
VADC offset error	Eo_{VADC}	-3		3	LSB11	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.5 Current shunt ADC

Table 11 Electrical characteristics of CSA [2,3]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
CSA resolution	RES_{CSA}		12		bit	
CSA input range 0	$RNG_{CSA,rng0}$		15		mV	ADCEN.ISNS_x_RNG=000_b [1]
CSA LSB size range 0	$LSB_{CSA,rng0}$		9.4		µV	ADCEN.ISNS_x_RNG=000_b [1]
CSA input range 1	$RNG_{CSA,rng1}$		30		mV	ADCEN.ISNS_x_RNG=001_b [1]
CSA LSB size range 1	$LSB_{CSA,rng1}$		18.8		µV	ADCEN.ISNS_x_RNG=001_b [1]
CSA input range 2	$RNG_{CSA,rng2}$		60		mV	ADCEN.ISNS_x_RNG=010_b [1]
CSA LSB size range 2	$LSB_{CSA,rng2}$		37.6		µV	ADCEN.ISNS_x_RNG=010_b [1]
CSA input range 3	$RNG_{CSA,rng3}$		120		mV	ADCEN.ISNS_x_RNG=011_b [1]
CSA LSB size range 3	$LSB_{CSA,rng3}$		75.2		µV	ADCEN.ISNS_x_RNG=011_b [1]
CSA input range 4	$RNG_{CSA,rng4}$		240		mV	ADCEN.ISNS_x_RNG≥100_b [1]
CSA LSB size range 4	$LSB_{CSA,rng4}$		150.4		µV	ADCEN.ISNS_x_RNG≥100_b [1]
CSA sample rate	SR_{CSA}		20		kS/s	
CSA offset error side A	Eo_{CSA_A}	-250		100	uV	
CSA offset error side B	Eo_{CSA_B}	-100		250	uV	
CSA gain error	Eg_{CSA}	-1.5		1.5	%FSR	
SNDR input ranges 0 and 1	$SNDR_{0/1}$	50			dB	ADCEN.ISNS_x_RNG=000_b / ADCEN.ISNS_x_RNG=001_b [1]
SNDR input ranges 2 and 3	$SNDR_{2/3}$	56			dB	ADCEN.ISNS_x_RNG=010_b / ADCEN.ISNS_x_RNG=011_b [1]
SNDR input range 4	$SNDR_4$	62			dB	ADCEN.ISNS_x_RNG=100_b [1]

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] All voltages are with respect to GND=0V unless otherwise noted.

[3] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.6 Timing parameters

Table 12 Timing parameters [2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Reset pulse width	t_{reset}	80			ns	
Rampup time	t_{rampup}			180	µs	RSTN is tied to VDDP, VDD and VDDP are above UVLO threshold. Time until interface is ready to accept commands
Startup time	t_{start}			10	µs	RSTN transision from 0 to 1 until interface is ready to accept commands
BIAS SWITCHES						
OUT propagation delay clamping	t_{clamp}			300	ns	C_{OUT}=0nF, time measured from OUT_EN_x change until 10% of final value [1]
OUT propagation delay enable	$t_{prop,en}$			300	ns	C_{OUT}=0nF, time measured from OUT_EN_x change until 10% of final value [1]
ADC						
VADC startup time	$t_{VADC,start}$	35	47	59	µs	from VADC_EN=1 until first result (I_ISNS_A) is available
VADC round robin time	$t_{VADC,round}$	17	23	29	µs	Full conversion cycle of all 10 channels
CSA						
CSA startup time	$t_{CSA,start}$	43	57	71	µs	
CSA conversion time	$t_{CSA,conv}$	38.4	51.2	64.0	µs	
DTS						
DTS startup Time	$t_{DTS,start}$	3.15	4.2	5.25	ms	
DTS conversion Time	$t_{DTS,conv}$	3	4	5	ms	

[1] x = [A, B]; y = [0, 1, 2, 3].

[2] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.7 Current consumption

Table 13 Current consumption [1]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
VDD current consumption, in RESET	$I_{VDD,reset}$		200		µA	RSTN pin = '0'
VDD current consumption, in ACTIVE	$I_{VDD,active}$		4	7	mA	RSTN pin = '1', VADC and CSA enabled, all DACs enabled, no DC loads at DAC outputs
VDDA / VREF current consumption, in RESET	$I_{VDDA,reset}$		300		µA	RSTN pin = '0'; per one side
VDDA / VREF current consumption, in ACTIVE	$I_{VDDA,active}$		4.2		mA	RSTN pin = '1', VADC and CSA enabled, all DACs enabled, no DC loads at DAC outputs; per one side
VDDP current consumption	I_{VDDP}		1		mA	Depending on communication traffic

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

3.5.8 Digital Interface

Table 14 Electrical Characteristics Digital Logic [1,2]

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
High-level input voltage	V_{IH}			0.7·VDDP	V	
Low-level input voltage	V_{IL}	0.3·VDDP			V	
High-level output voltage	V_{OH}	VDDP – 0.1			V	VDDP = 1.65 V…3.6 V I = 1 mA
Low-level output voltage	V_{OL}			0.1	V	VDDP = 1.65 V…3.6 V I = 1 mA
xternal ADR0/1 pull resistor	ADR_{PULL}	0		100	Ohm	
Reset pulse duration	RST_{active}	80			ns	

[1] The minimum and maximum limits are valid over the full operational range and are ensured by characterization and statistical correlation. Typical values are tested at ambient temperature T_A = 25 °C.

[2] All voltages are with respect to GND=0V unless otherwise noted.

3.6 ESD Concept

The following figures show a simplified view of the main ESD protection building blocks:

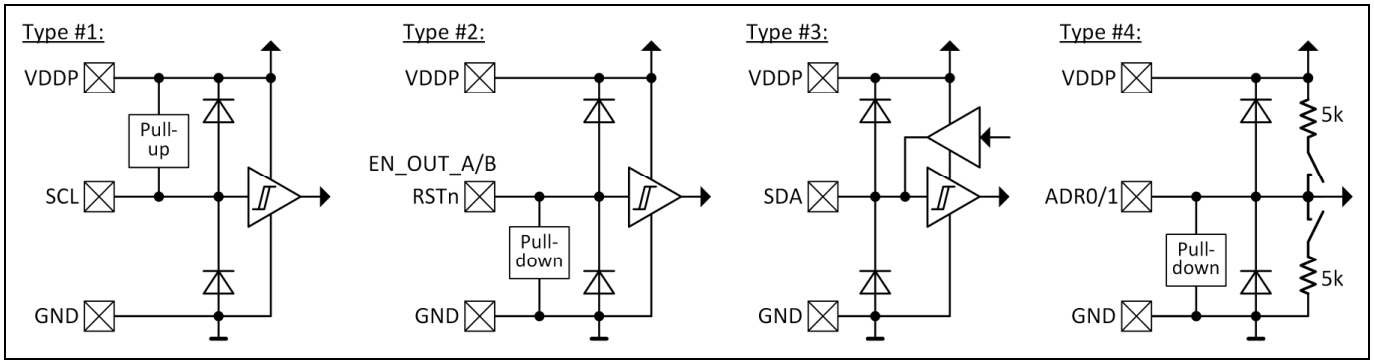


Figure 4 ESD protection for digital pins

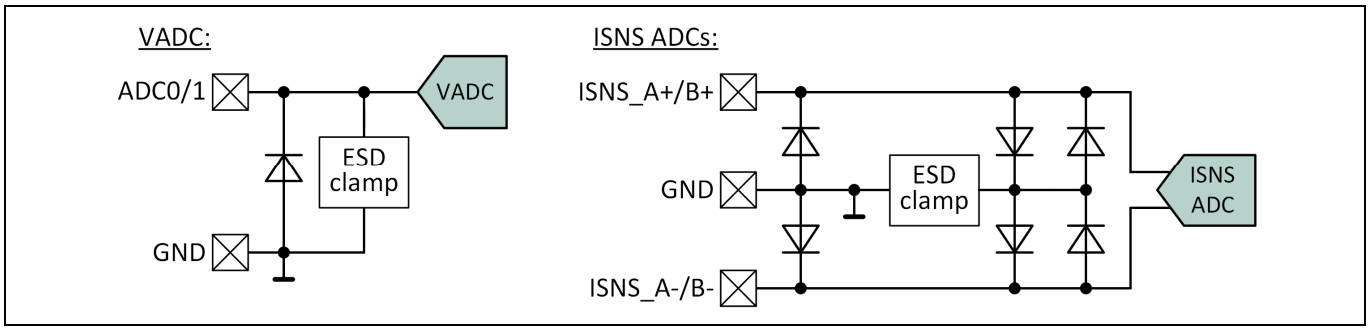


Figure 5 ESD protection for ADC pins

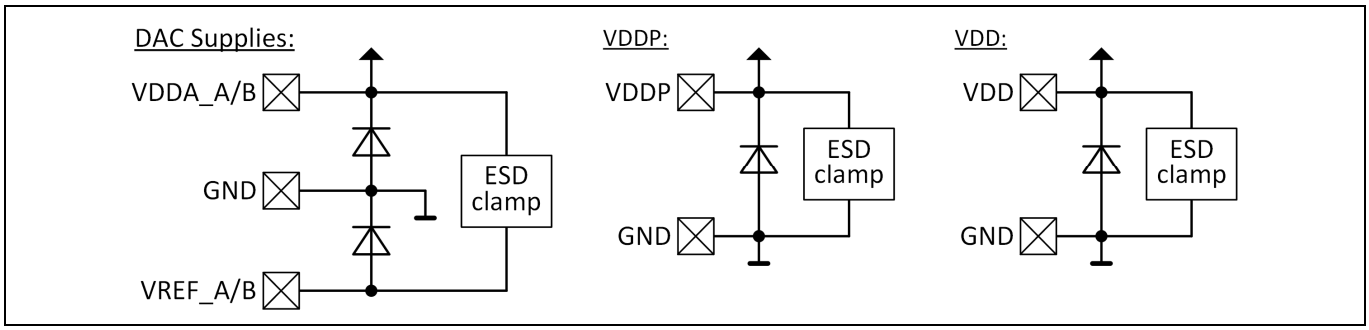


Figure 6 ESD protection for supply pins

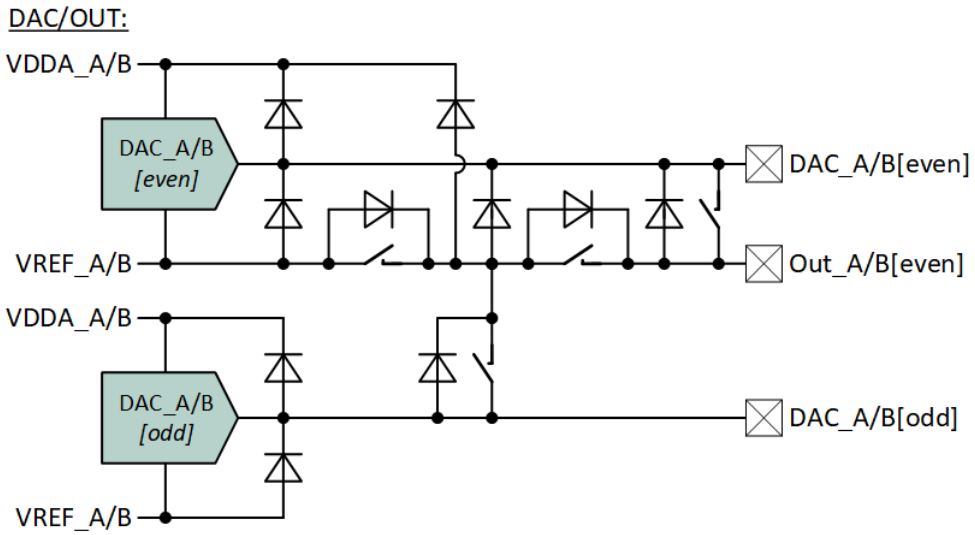


Figure 7 ESD protection for DAC pins

4 Functional Description

4.1 Overview

The BGMC1210 is an eight-channel analog monitoring and control IC with integrated switch control on four output channels, capable of voltage, current and temperature monitoring. The device supports dual polarity on two of its DAC groups A and B, each including four DACs. Two of the DACs in each group are equipped with switches to enable fast toggling between the DAC output and configured clamping voltage. Positive or negative polarity on a corresponding DAC group is defined by the voltages at its supply inputs. The device registers are configured through an I2C/I3C interface.

The main application of BGMC1210 is a bias voltage generation for RF transistor Power Amplifiers as a below simplified block diagram shows.

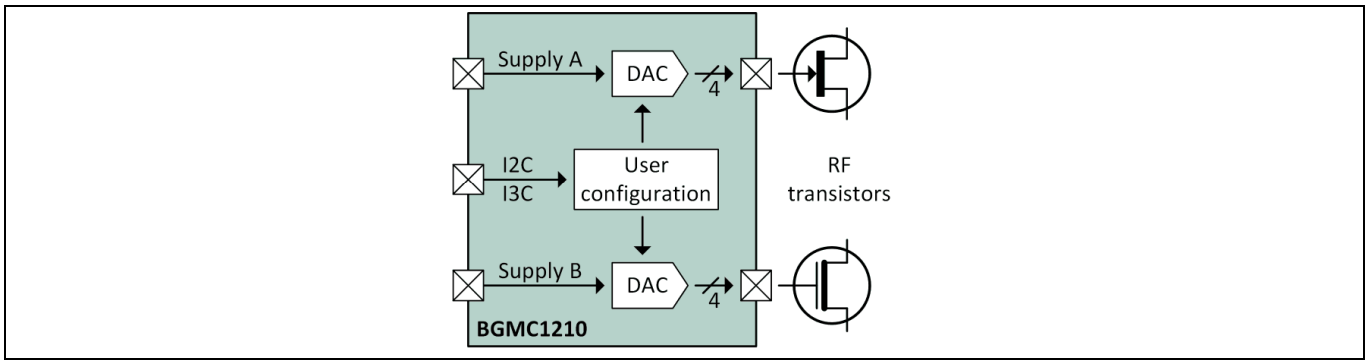


Figure 8 Simplified Device Block Diagram

4.2 Functional Block Diagram

The main building blocks of BGMC1210 are shown in the figure below. It also lists all the device pins.

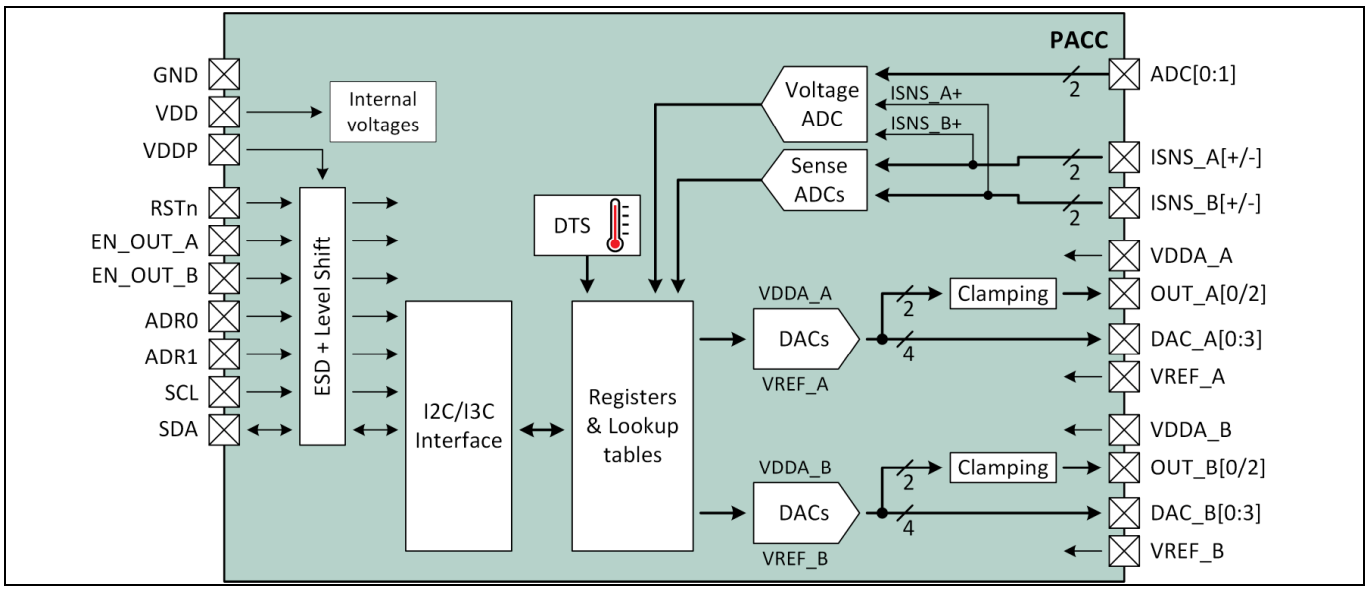


Figure 9 Detailed Device Block Diagram

4.3 Startup and Shutdown Procedure

4.3.1 Startup Procedure

The following startup procedure is recommended:

1. RSTN is connected to VDDP via pull-up resistor
2. Turn-on VREF_A, VREF_B, VDD, VDDP, VDDA_A, VDDA_B
3. Once VDDP and VDD are powered up wait t_{rampup} = 180 us to allow the I2C/I3C interface to unlock
4. Program registers:
   - programmed registers will have immediate effect on analog periphery
   - ADCs can be fetched (if enabled)
5. PA transistor gate voltages at OUT_A0(2), OUT_B0(2), DAC_A1(3), DAC_B1(3) can be enabled
6. PA transistors Vdd supply can be enabled

Power supplies can be ramped-up in any sequence. To make the digital interface available VDD and VDDP need to cross their undervoltage release threshold $UVLO_{VDD,rel}$ and $UVLO_{VDDP,rel}$. This is necessary as the device-internal logic is supplied by internal voltages derived from VDD (see Figure 10 time point #1) and the device pins are supplied by VDDP:

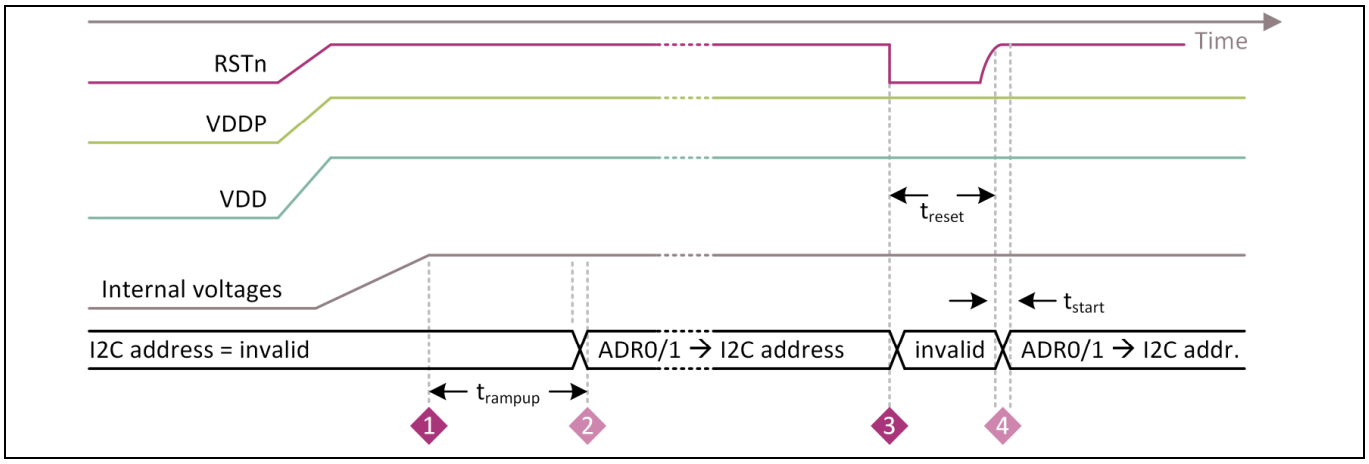


Figure 10 Power-Up and reset Timing

After the rampup time t_{rampup} the internal voltages are stable and the address pins ADR0/1 determine the I2C address (see time point #2). Digital communication (e.g. I2C accesses or I3C dynamic address assertion) can now take place. The address remains stable until the next VDD/VDDP power-down or reset via RSTN. Note that the voltages VDDA_A, VDDA_B, VREF_A and VREF_B will have no effect on the availability of the digital interface.

Once t_{rampup} elapsed and the internal voltages are available the temperature sensor (DTS), the voltage ADC (ADC) as well as the current sense ADC (CSA) can be used. To do so they need to be enabled and their startup time needs to elapse ($t_{VADC,start}$ / $t_{CSA,start}$ / $t_{DTS,start}$).

A hardware reset via RSTN (see time point #3) will block the digital interface. Once deasserted communiation can take place again after time t_{start} elapsed (see time point #4). For further details on the software reset please refer to section 4.3.3.

In cases where the RSTN is driven directly from a microcontroller/FPGA without being pulled to VDDP the rampup time t_{rampup} must elapse before using the I2C/I3C interface.

In general it is good practice to assert a hardware reset via RSTN after each power cycle.

4.3.2 Voltage Monitoring

All voltages provided externally to the device are monitored. Once a voltage falls below its undervoltage limit ($UVLO_{lck}$) it needs to rise beyond its undervoltage release limit ($UVLO_{rel}$). The voltage difference between the two is the hysteresis:

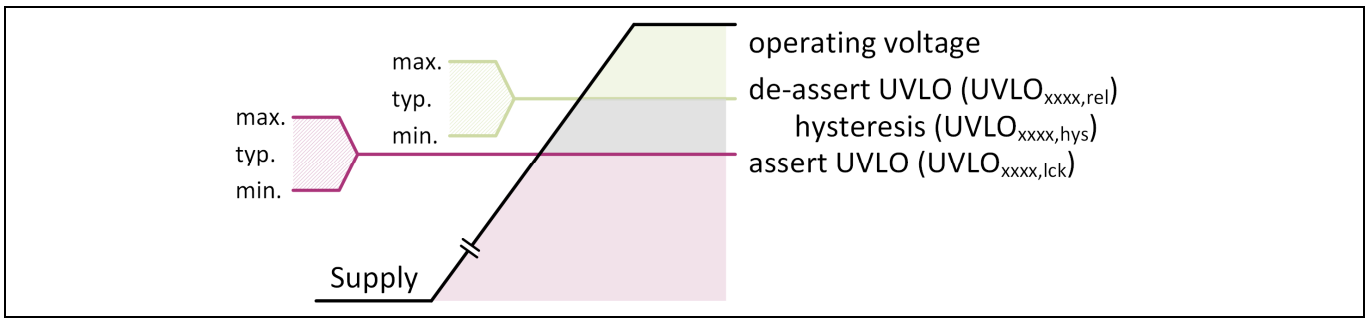


Figure 11 Voltage Monitoring

4.3.3 Software Reset

In case software needs to execute a reset by asserting RSTN low (see Figure 10 time point #3) the digital interface will be blocked during that time. The RSTN pin needs to be logic low for minimum time of 80ns (RST_{active}). After reset is released it takes maximum t_{start} to make the digital interface accessible again (see Figure 10 time point #4).

Note: *Reset events shorter than 50ns can cause undeterministic device behavior. In case such events are unavoidable (e.g. during power-on phase) a defined reset pulse is required.*

4.3.4 Shutdown Procedure

The following shutdown procedure is recommended:

1. Set gate voltages at DAC_A1(3), DAC_B1(3) to pinchoff or lower
2. Set transistor gate voltages at OUT_A0(2), OUT_B0(2) to clamping or lower
3. Disable PA transistor supply
4. Set RSTN low (RSTN=0)
5. Turn-off VREF_A, VREF_B, VDD, VDDP, VDDA_A, VDDA_B (no specific sequence required)

4.4 Operation Modes

4.4.1 Mode: RESET

At power-up, when RSTN input is low or in the event of VDD/VDDP supply getting out of range, the BGMC1210 state machine is placed in a RESET state:

- All registers are reset to their initial values (asynchronous)
- Analog infrastructure for DACs is powered up to ensure safe output voltages and fast startup
- DAC_xy outputs are set to VREF_x by default register settings and are pulled down to VREF_x with internal safety clamp
- OUT_xy outputs are switched to VREF_x (clamped)
- All ADCs are disabled
- No digital communication to the device is possible

4.4.2 Mode: ACTIVE

After RSTN becomes logic high and if main supplies (VDD, VDDP and internal supplies) are ready and within range, the BGMC1210 state machine finds itself in an ACTIVE state:

- Digital interface available
- All registers are transparent towards the analog part: a changed register content will have immediate effect on the output
- The ADCs are operating (if enabled) and results can be fetched from registers

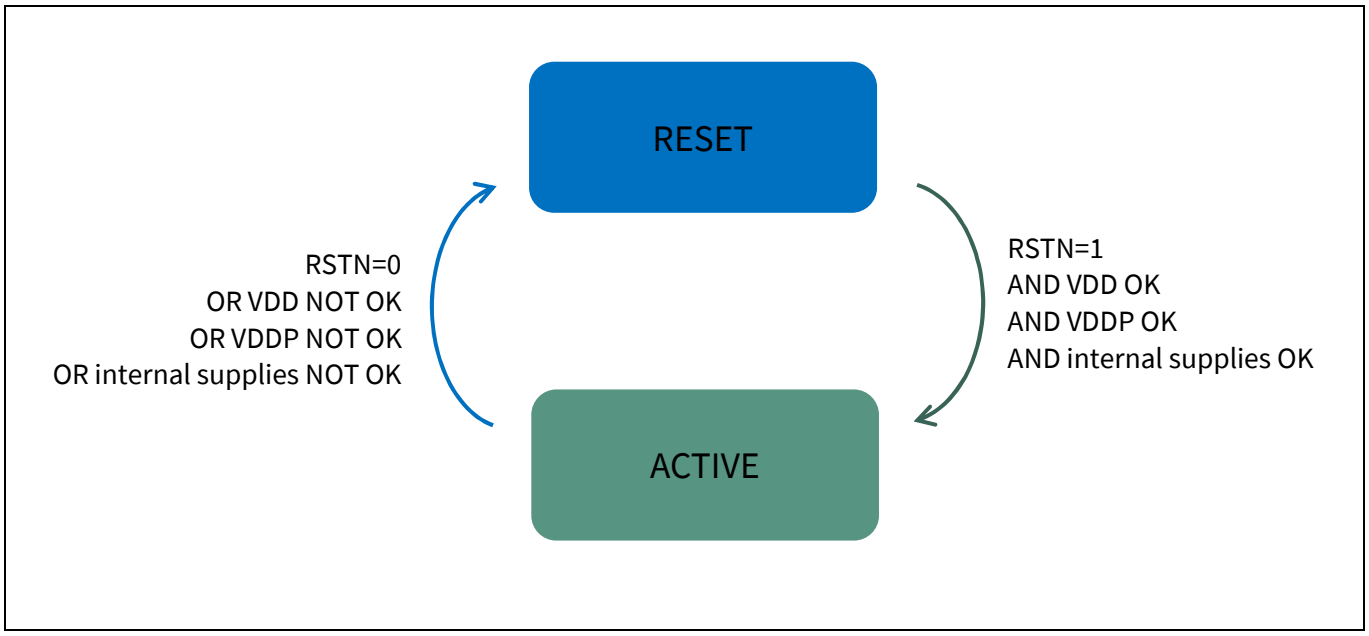


Figure 12 BGMC1210 state diagram

4.5 DAC Output Voltage Configuration

4.5.1 Overview

The analog control channels are built around eight DAC cores, each consisting of an R-2R DAC and an output voltage buffer. BGMC1210 offers two independent groups of outputs: A and B. Each group consists of four DACs with a separate supply domain per group.

Two of the DACs per group, the ones with even channel number (DAC_A0, DAC_A2, DAC_B0, DAC_B2), are connected via switched circuits to additional outputs: OUT_A0, OUT_A2, OUT_B0, OUT_B2. This enables clamping of the output voltage, which means that the voltage at these pins can be toggled between two levels to support PA operation in a time-division duplexing (TDD) radios. One voltage level, defined by the DAC with even channel number, is used to bring RF transistors into their active/conductive region. The other voltage level (clamping voltage) is used to bring the RF transistors into their pinch-off region. Two pins, EN_OUT_A and EN_OUT_B, allow toggling between two voltages at switched outputs of corresponding DAC group. A simplified block diagram is given in the following figure.

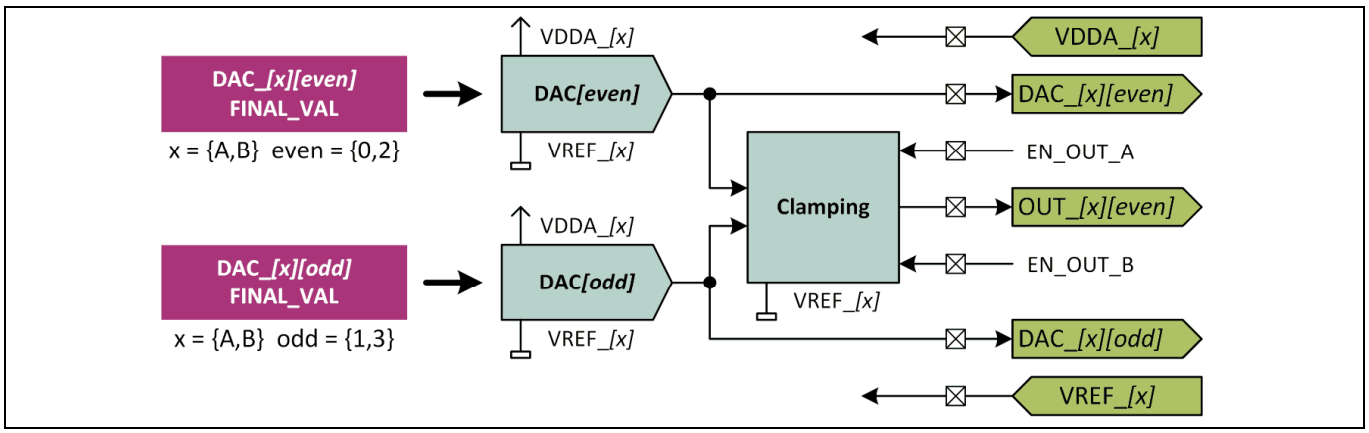


Figure 13 DAC Simplified Block Diagram

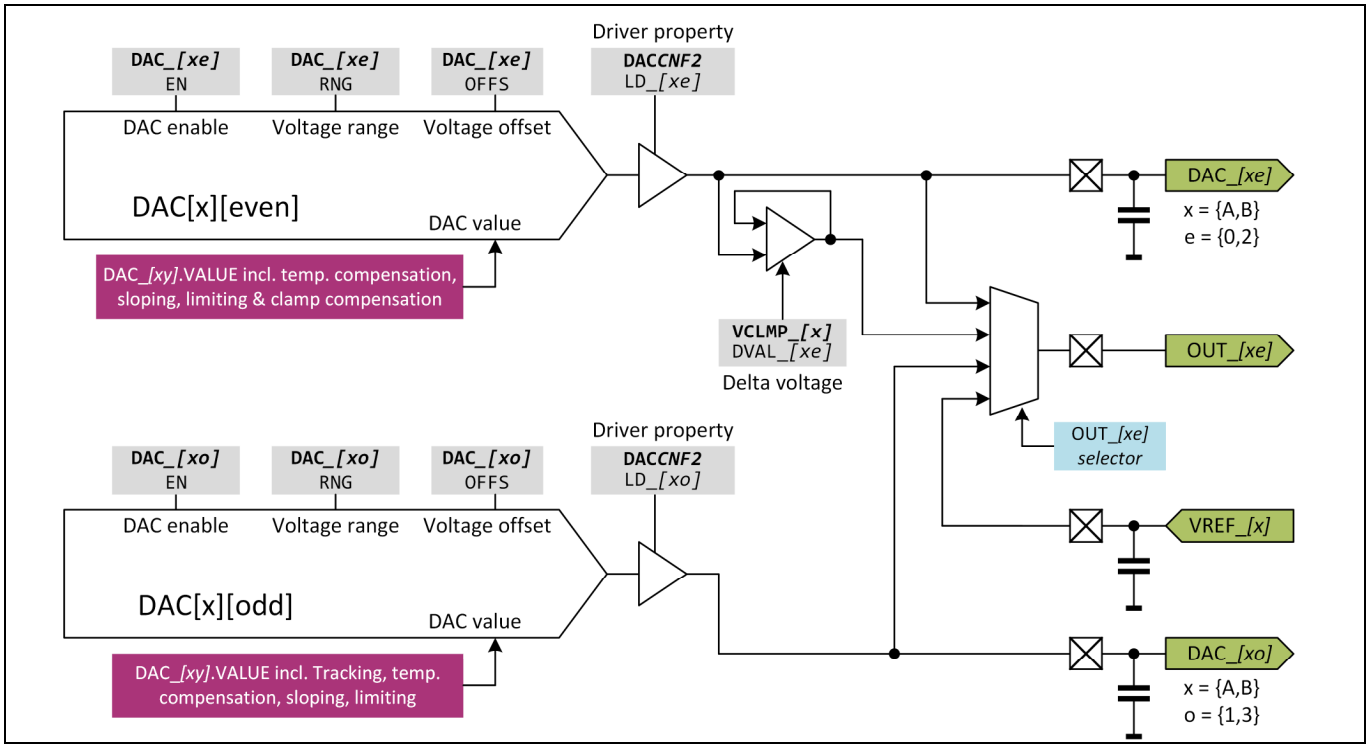


Figure 14 DACs And Their Registers

The generated voltages depend on various register settings. Figure 14 shows the entry point for each register setting.

Every DAC has a 12-bit resolution, internal reference voltage and can be adjusted in range and offset. Supply range per DAC group is defined by reference potential VREF_x and supply input VDDA_x: VDDA_x - VREF_x. Supply voltage can be selected down to -8V and up to +8V, so that enhancement type LDMOS transistors as well as depletion type GaN transistors are supported.
To reduce traffic on the digital control interface it is possible to enable temperature compensation via a look-up table and/or enable tracking of the DAC used for peak device to the DAC used for main device.
Additional features include DAC clamping compensation, a dedicated internal clamping buffer and a possibility to use neighboring DAC as a clamping potential.

4.5.2 DAC and OUT Voltages in Reset Mode

An external reset (RSTN logic low) and a power-on reset (VDD/VDDP) will cause all register settings to revert to their reset values. This also disables the DAC cores. In this state the BGMC1210 pulls DAC_[x][even], DAC_[x][odd] and OUT_[x][even] outputs to VREF_[x] levels by means of dedicated safety clamps to protect the gates of RF transistors from electrical damage. The following figure gives a simplified overview about the electrical behavior in reset mode:

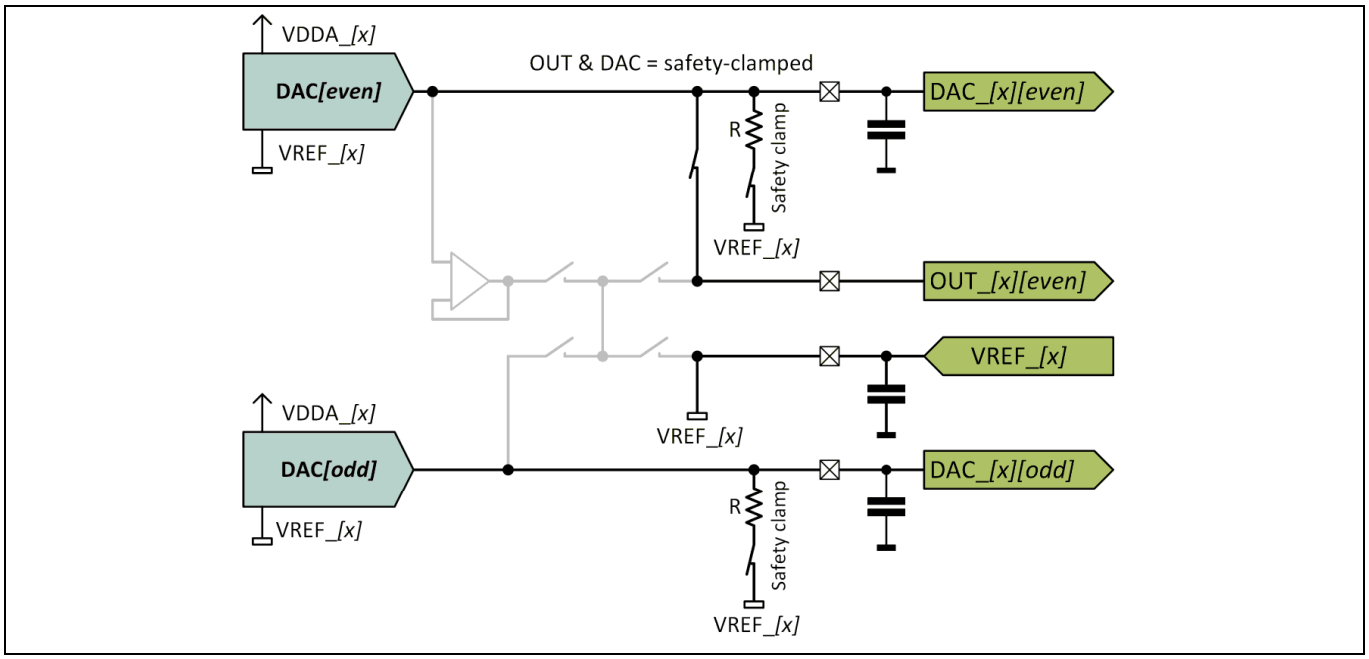


Figure 15 DAC Power-On / Reset Behavior

Please note that the OUT_[x][even] outputs will be clamped to VREF_[x] through a transistor which will cause a clamping voltage slightly higher than at the DAC_[x][even] or DAC_[x][odd] outputs.

4.6 DAC and OUT Voltages in Active Mode

In the simplest case (with compensations, slope control and limitation disabled) a DAC output voltage is determined by the value in the DAC_[xy].VALUE register (e.g. DAC_A3.VALUE):

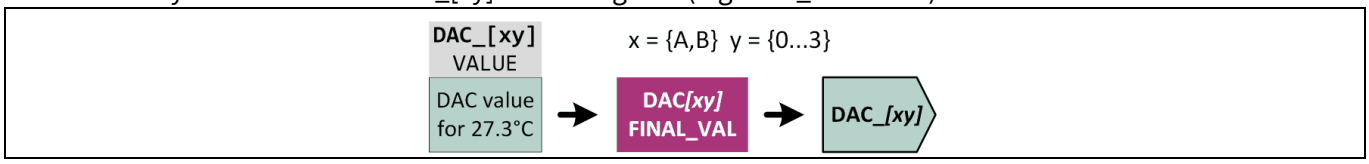


Figure 16 DAC Output Voltage Simple View

In Active Mode the DAC voltages are forwarded to the corresponding DAC and OUT pins according to the following simplified circuit diagram:

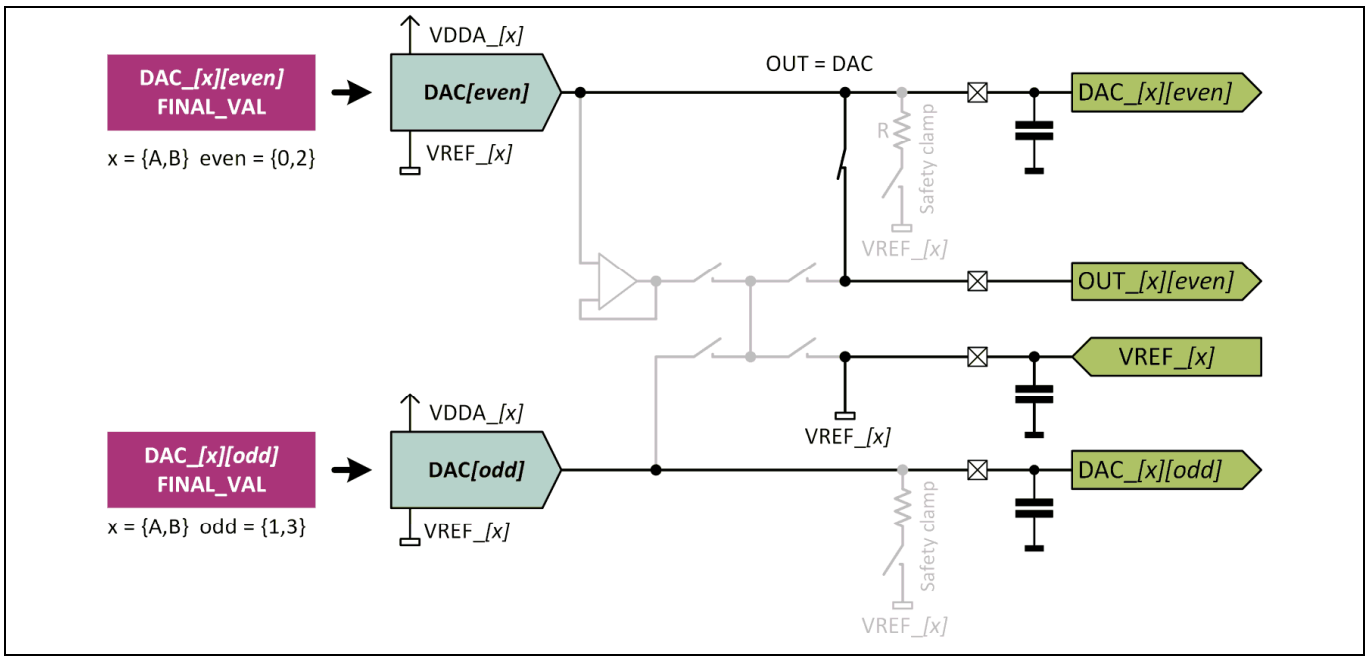


Figure 17 DAC and OUT Voltage in Active Mode

4.6.1 DAC Value Calculation Flow

To allow higher flexibility DAC output voltages depend on various register settings. These settings will be processed in several steps resulting in a final DAC value which will then be converted into a voltage. Note that even and odd DACs behave slightly different since their purpose is different.

The following figure lists individual steps of this processing flow. For the sake of readability DAC A3 and DAC A2 are shown as an odd and even DAC, respectively. The figure is also valid for other odd/even DAC pairs like {A1, A0}, {B1, B0} and {B3, B2} by simply replacing {A3, A2} accordingly:

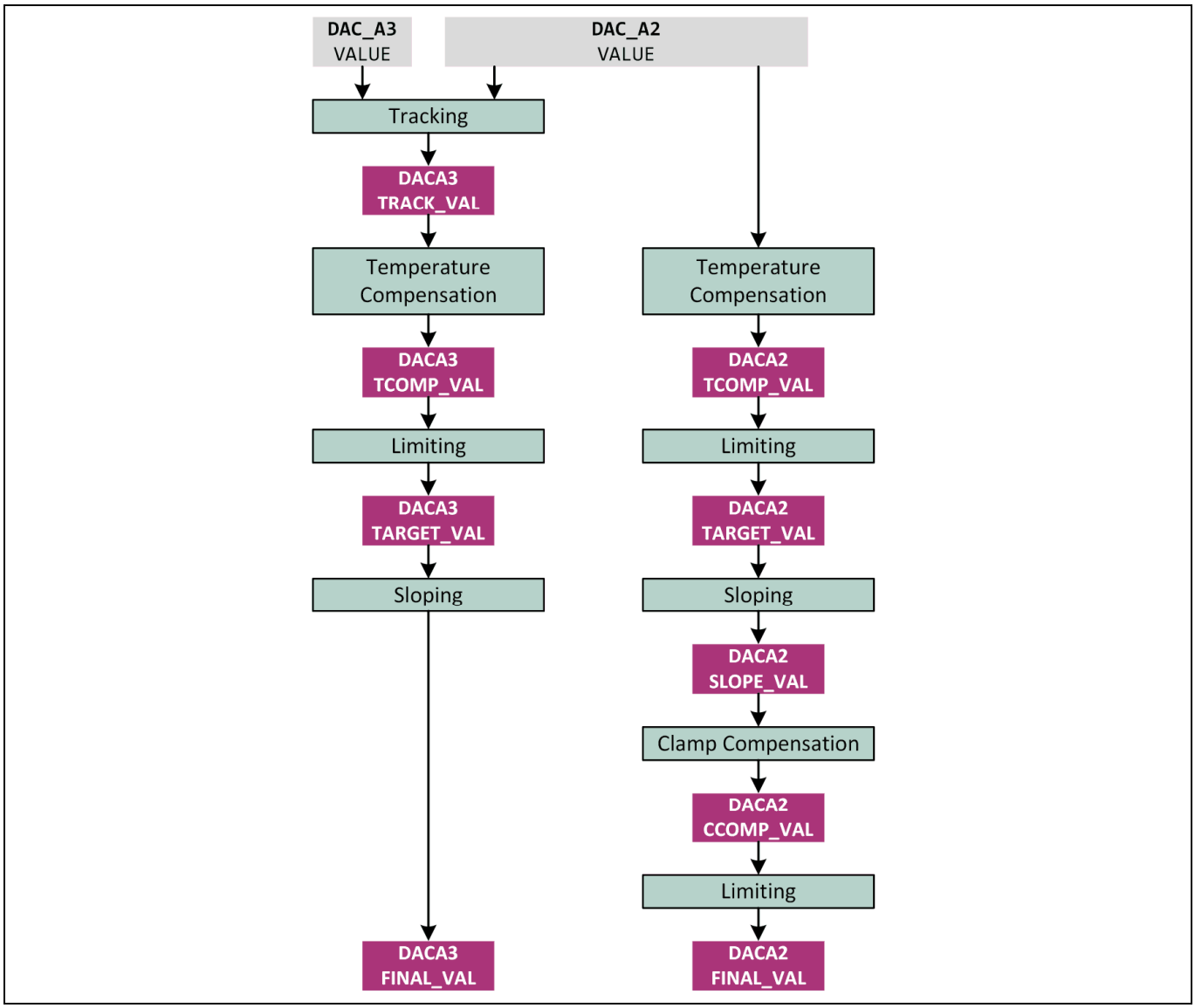


Figure 18 DAC Value Calculation Flow

- Tracking (step #1): An odd DAC channel can be set to track its neighboring even DAC channel (e.g. DAC_A3 tracks DAC_A2). In this case an offset between the channels needs to be defined.
- Temperature compensation (step #2): A device receiving a DAC voltage usually shows a performance drifting with temperature. To mitigate such effects a temperature compensation mechanism is provided.
- Sloping (step #3): To avoid excessive (peak) currents when charging capacitors connected to the DACs an output voltage step can be slowed down by turning the step into a ramp. This is done by the sloping feature.

- Limiting (step #4 and #6): To prevent a DAC voltage from rolling over when exceeding the maximum or minimum DAC value a limit is used. Under normal operating / configuration conditions the limits will never be reached.
- Clamp Compensation (step #5): Some RF transistors fed by the DACs show trapping effects causing them to underperform at the bias point set by the DAC. This happens when the transistor returns from the clamped (pinch-off) state to the conducting state. This effect usually disappears after a short time (microseconds). In such situations time-limited over-biasing may be required. This is provided by the clamp compensation mechanism for all even DACs.

The final calculated value is then fed to the DAC which will then generate the corresponding output voltage. During software implementation phase it can come in handy to check the calculated DAC value. This can be done by using the DAC_FB register.

All these steps are described in more details later during this chapter.

4.6.2 Initial DAC Value Calculation

To calculate DAC_[xy].VALUE for a desired DAC output voltage the following parameters must be known:

- DAC supply voltages VDDA_[x] and VREF_[x]
- Desired output voltage for DAC channel [xy] relative to VREF_[x]
- DAC range
- DAC offset

The figure below shows how those parameters define the DAC output voltage:

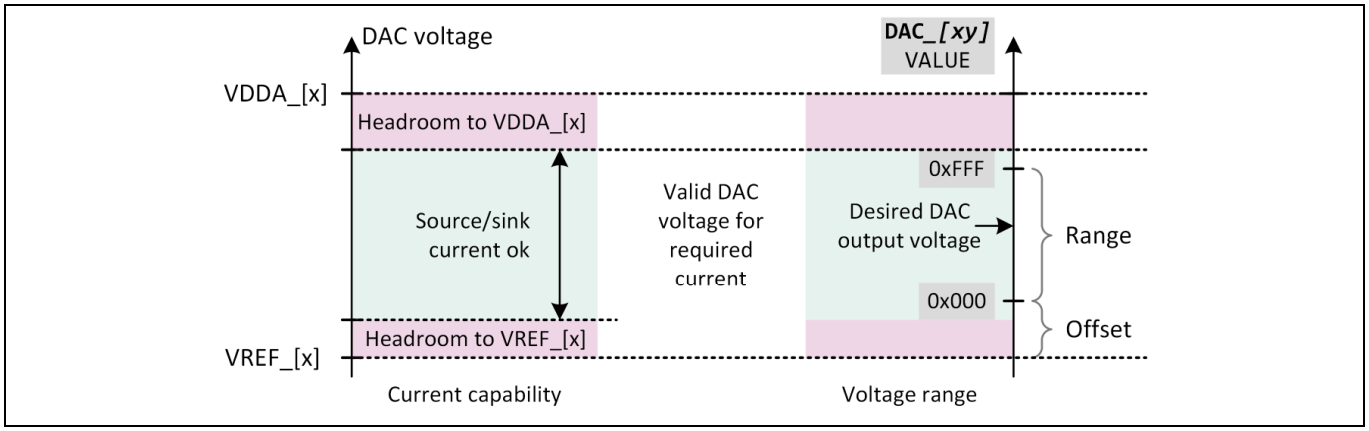


Figure 19 Parameters Relevant for DAC Value

The DAC output voltage should have a certain headroom to VDDA_[x] and VREF_[x] to allow normal operation of DAC buffers, ensure specified DAC accuracy and sink and source current capabilities. For details on the required voltage headrooms see the specifications for I_{src} and $I_{src,hi}$ as well as I_{snk} and $I_{snk,hi}$ in Table 7.

The following figure illustrates DAC buffer driving capabilities with respect to the buffer output voltage V_{DAC}:

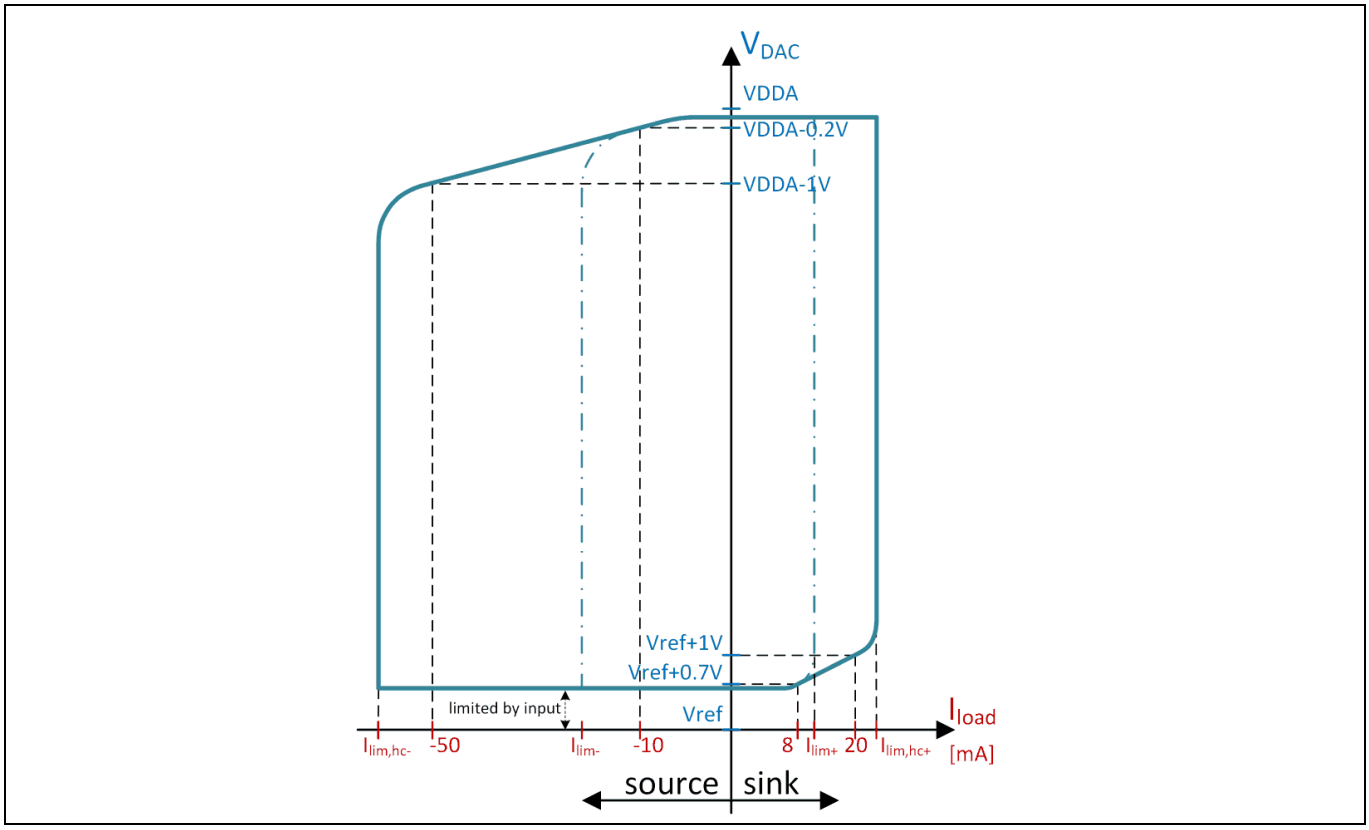


Figure 20 DAC Output Voltage Capability

To set a fixed voltage offset in relation to VREF_[x] a corresponding setting can be defined for each individual channel by DAC_[xy].OFFS. Preferrably the offset is selected such that the desired DAC voltage range resides within the boundaries of VDDA_[x] / VREF_[x] with respecting corresponding voltage headrooms. Available offsets are 0V (OFFS = 0), 0.5V (OFFS = 1), 1.5V (OFFS = 2) and 3.0V (OFFS = 3).

To maximize DAC granularity the 3.5V voltage range is used (DAC_[xy].RNG = 1). Otherwise the range will be 7V (DAC_[xy].RNG = 1).

As the final step the DAC value DAC_[xy].VALUE can be calculated as the voltage difference relative to the offset voltage set by DAC_[xy].OFFS (=ΔV). The following equation can be used to calculate the DAC value (refer to an example in section 5.2 for more details):

$$\text{DAC\_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V \qquad \Delta V = \text{DAC\_Voltage - Offset - VREF\_[x]}$$

Figure 21 DAC Value Equation

4.6.3 DAC Value Step #1: Tracking

An odd DAC channel can be set to track its neighboring even DAC channel (e.g. DAC_A3 tracks DAC_A2). This is typically done when an odd DAC is used as a clamping voltage for the neighboring even DAC. Often clamping voltage can/should have a fixed voltage offset to bias point voltage. In this case an offset between the two channels is defined as shown on Figure 22.

If an odd DAC is configured to track an even DAC, the range and offset settings will be taken from the even DAC registers. This is needed for linear tracking and proper limitation.

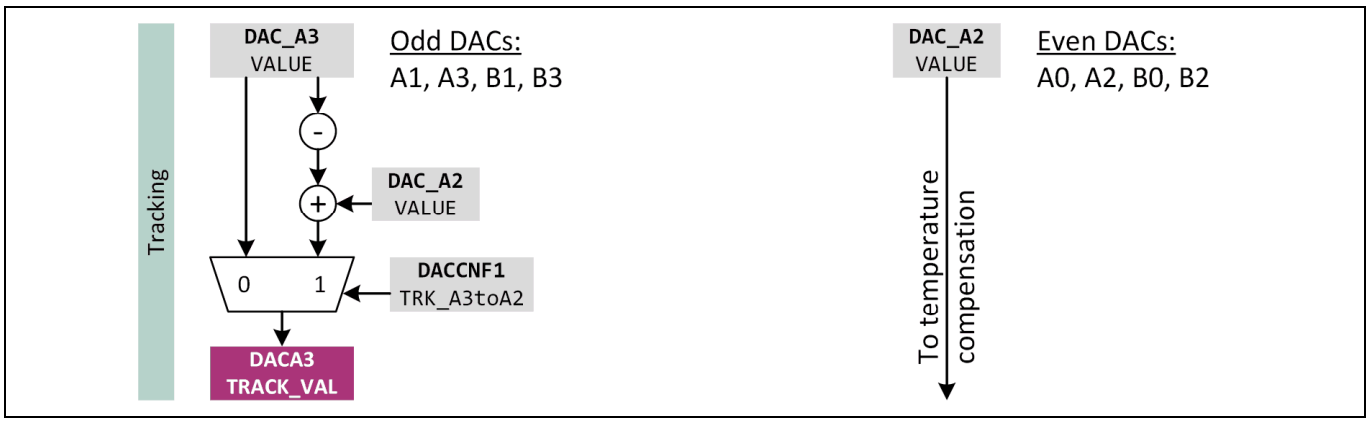


Figure 22 DAC Value Calculation: Tracking

4.6.4 DAC Value Step #2: Temperature Compensation

The BGMC1210 provides built-in thermal compensation as a convenient solution to minimize temperature drifts of both internal DACs (minor drift) and RF transistors (major drift) connected to them. In case user application requires temperature compensation it is advised to read through the following sections.

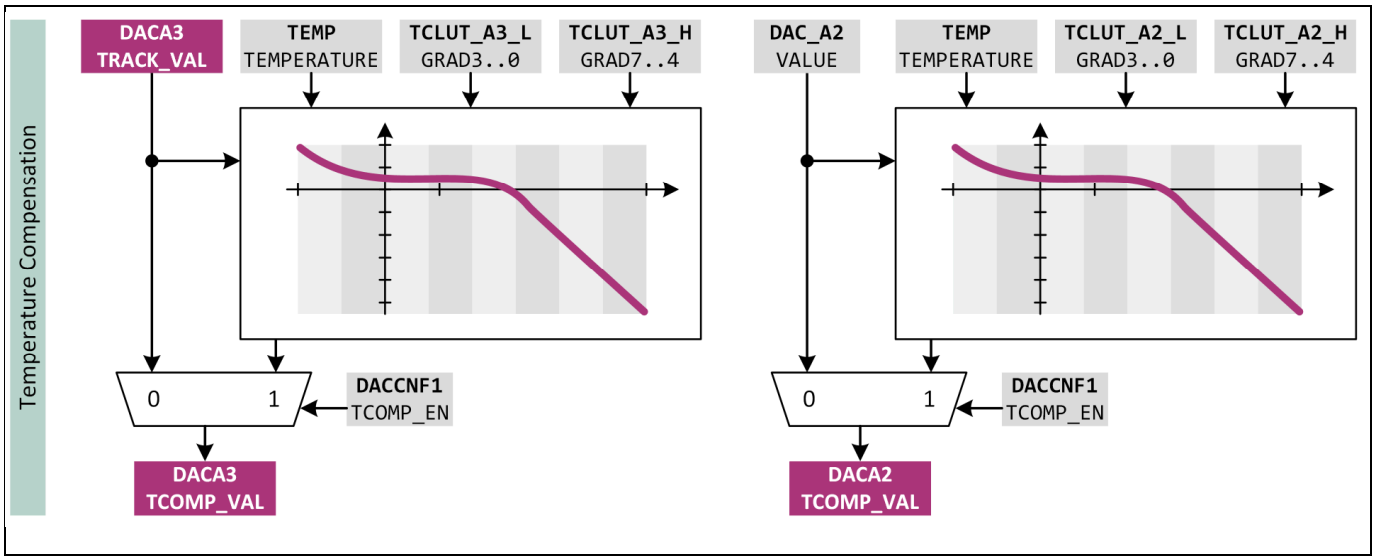


Figure 23 DAC Value Calculation: Temperature Compensation

Compensation is implemented with a Look-Up Table (LUT), in which eight temperature coefficients (gradients) for each individual DAC can be configured (e.g. TCLUT_A3_L and TCLUT_A3_H). Depending on the temperature measured by the Die Temperature Sensor (DTS), a delta to the reference DAC value of 27.3°C is calculated and provided to the DAC via DAC_[xy]_VAL (if temperature compensation is enabled via DACCNF1.TCOMP_EN).

In total nine equidistant interpolation points at fixed temperatures are needed to calculate the eight gradients (see Figure 24). The gradients need to be defined in such a way that the piecewise interpolated values approximate the Delta DAC curve (see Figure 25) best.

The following example is a real-world example where the DACs are used in a GaN-based power amplifier. It describes the process how to find the best gradients. The starting point is always a measurement over temperature to determine the DAC values required to achieve the desired DAC (here DAC_A3) output voltage. Figure 24 shows an example of such measurement.

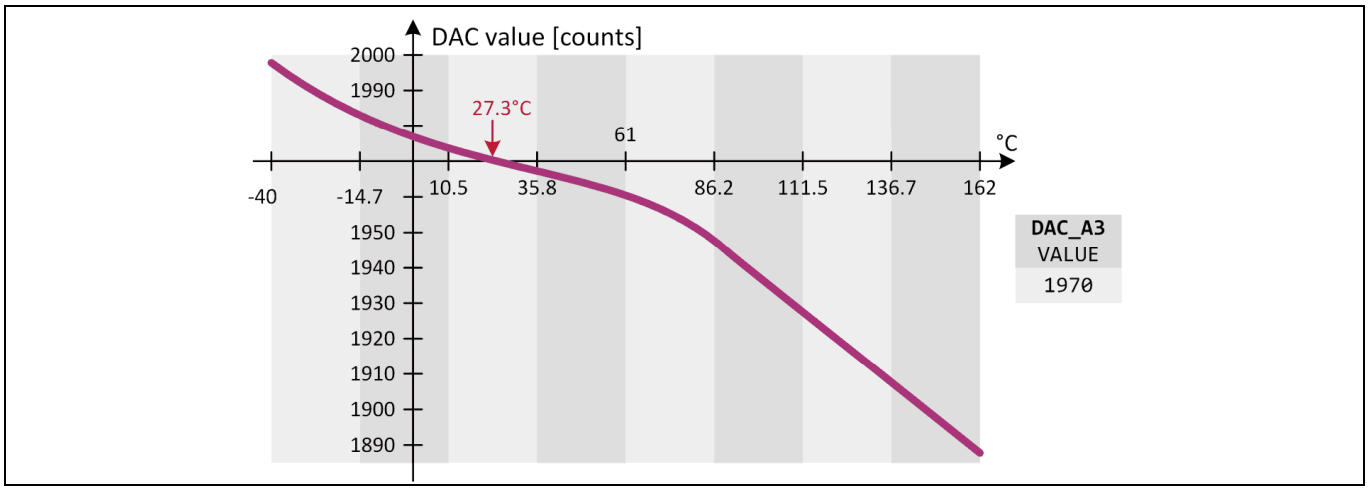


Figure 24 DAC Value Over Temperature

In this example a DAC value of 1970 is required to achieve the desired output voltage at the reference temperature of 27.3°C measured by the DTS. This value is used for the DAC_A3.VALUE register. It will also be the reference point for the gradient fitting.

The temperature points shown on the X-axis match the temperatures at which one gradient starts/ends. Gradient #0 starts at -40°C while gradient #1 starts at -14.7°C and so on. Therefore it makes sense to measure the DAC value at least for these temperatures. For a better fitting more measurements are advised. Figure 24 shows such a graph measured using multiple points.

The graph in Figure 25 can then be plotted relative to the DAC value at 27.3°C:

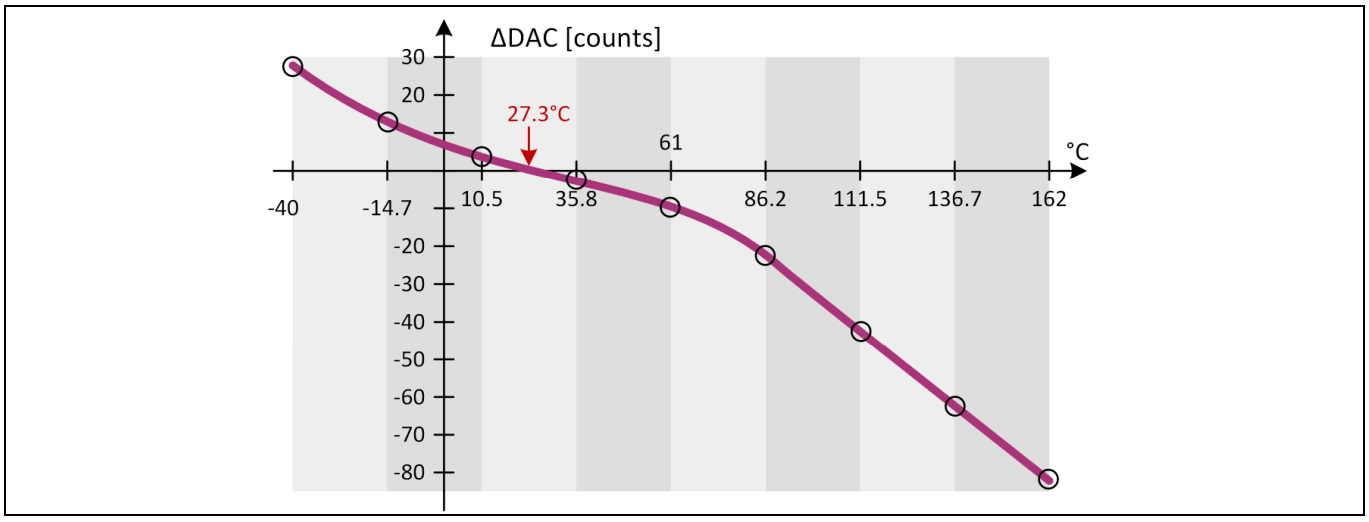


Figure 25 Delta DAC Over Temperature

The delta values can now be used to calculate the gradients such that they best-fit the previously shown curve. Each gradient is valid for a temperature range of 24.5K. This odd number is calculated like this: (32 counts in the TEMP.TEMPERATURE register) * (0.7648K per count).

Gradient #0 for example is used only for temperatures between -40°C … -15.5°C. Gradient #1 starts at -14.7°C (-15.5°C + 0.7648K) and ends at +9.7°C (10.5°C – 0.7648K) and so on.

A gradient describes the delta between two DAC values measured at two temperatures 8 Kelvin apart from each other. The gradients reach from -8…+7 in steps of 1 and are programmed using the two's complement (Figure 26).

$$\text{grad[n]} = \frac{\text{DAC deviation [counts]}}{\text{per 8 Kelvin}}$$

Decimal	Binary	Hex	Decimal	Binary	Hex
7	0111	7	-1	1111	F
6	0110	6	-2	1110	E
5	0101	5	-3	1101	D
4	0100	4	-4	1100	C
3	0011	3	-5	1011	B
2	0010	2	-6	1010	A
1	0001	1	-7	1001	9
0	0000	0	-8	1000	8

Figure 26 Gradient Two's Complement

For example if the DAC value for -40°C is 2000 counts and for -15.5°C it is 1985 counts the DAC-Delta is 15 counts. Since the temperature delta is 24.5K the gradient is calculated as:

(1985 counts - 2000 counts) / [-15.5°C – (-40.0°C)] = -15 counts / 24.5K = -4.9 counts / 8K

The nearest suitable gradient is -5 which stands for -5 counts / 8K. This procedure is repeated for each gradient.

Some gradient examples are shown in the following figure.

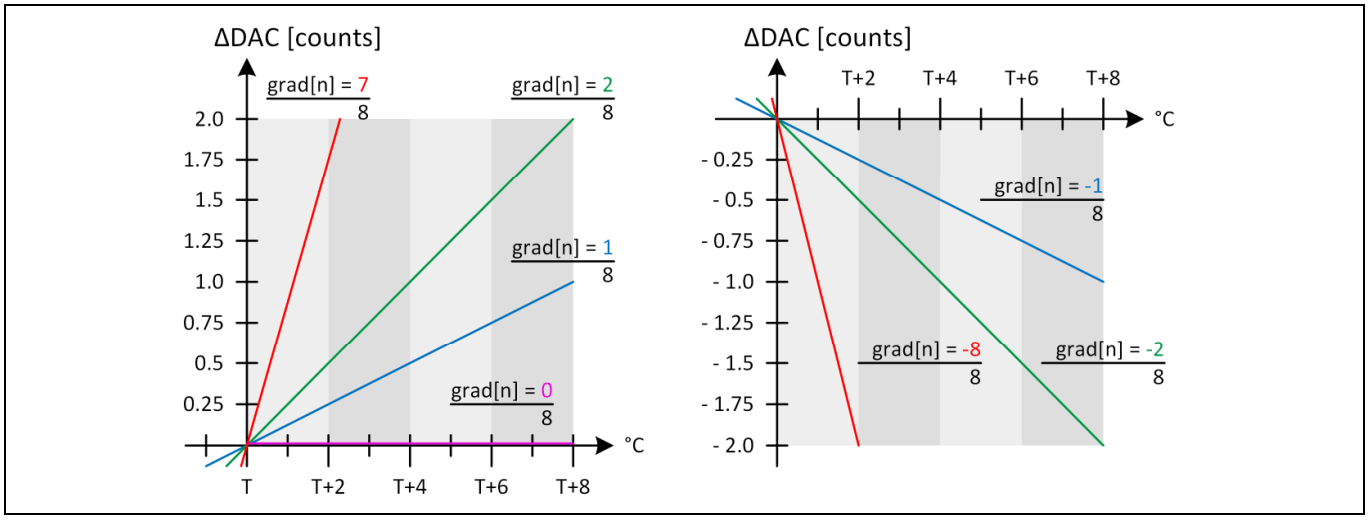


Figure 27 Gradient Examples

An example for a gradient fitted curve can be found in Figure 28. The curve from Figure 25 is shown as a white envelope.

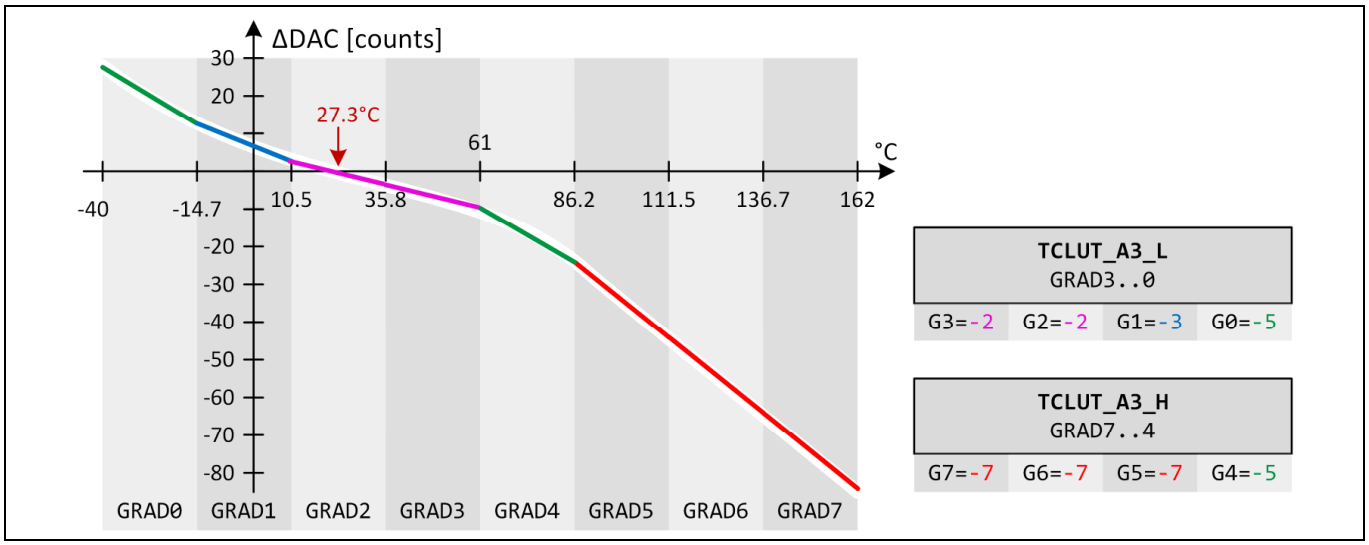


Figure 28 Gradient Example

Please note that the gradients in the registers TCLUT_A3_H and TCLUT_A3_L are shown with MSB on the left (gradient #0) and LSB on the right (gradient #7) while in Figure 28 they appear the other way around.

4.6.5 DAC Value Step #3: Limit

The DAC values coming from the temperature compensation (DAC[xy] TCOMP_VAL) are limited to 0xFFF at the upper end and 0x000 at the lower end. Temperature compensation may leed to values outside this range and therefore limits need to be applied. For the majority of usecases it is unlikely that the limits will ever be reached as the DACs are usually operated with enough headroom from the upper and lower limit.

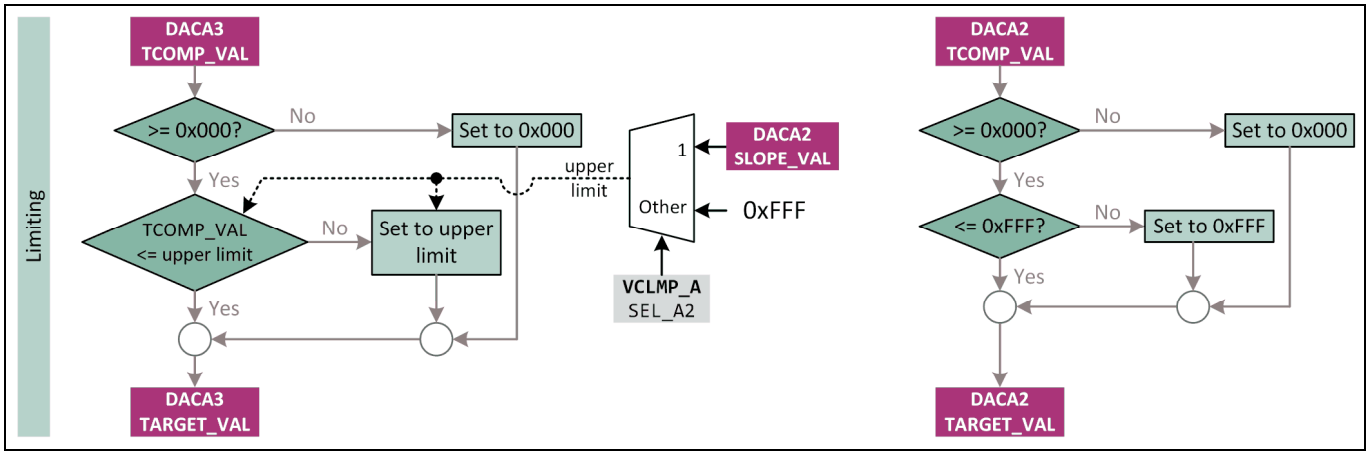


Figure 29 DAC Limiting After Temperature Compensation

For an odd DAC the upper limit 0xFFF will be decreased when its neighboring even DAC uses the odd DAC as its clamping voltage. This is done to ensure that the clamping voltage (used for transistor pinch-off mode) never exceeds the voltage used for transistor conducting mode.
This feature is available purely for safety reasons. Note that when the even DAC SLOPE_VAL is used as the upper limit the transistor will still be in conducting mode. It is the user's responsibility to ensure that the clamping voltage generated by the odd DACs is low enough to ensure transistor pinch-off mode.

4.6.6 DAC Value Step #4: Slope

To reduce inrush currents especially after enabling a DAC it is possible to define an update rate with which the DAC will adjust its output voltage to the programmed value. To do so the DAC input value (DAC[xy] FINAL_VAL) is updated step-wise. During normal operation this feature is no loger needed.

Each time DAC_[xy] TARGET_VAL changes DAC_[xy] SLOPE_VAL value will be updated count by count with an update rate defined by DACCTRL.SLP: 0 = 50ns, 1 = 1us, 2 = 5us, 3 = 10us, 4 = 100us, 5 = 250us, 6 = 1ms, 7 = 4 ms. The slope configured in DACCTRL.SLP is the same for all DACs.

The (analog) offset is not affected by sloping. In other words: when a DAC is enabled its output voltage will rapidly change from VREF_[x] to the offset voltage. But from the offset to the final DAC voltage the sloping will take effect:

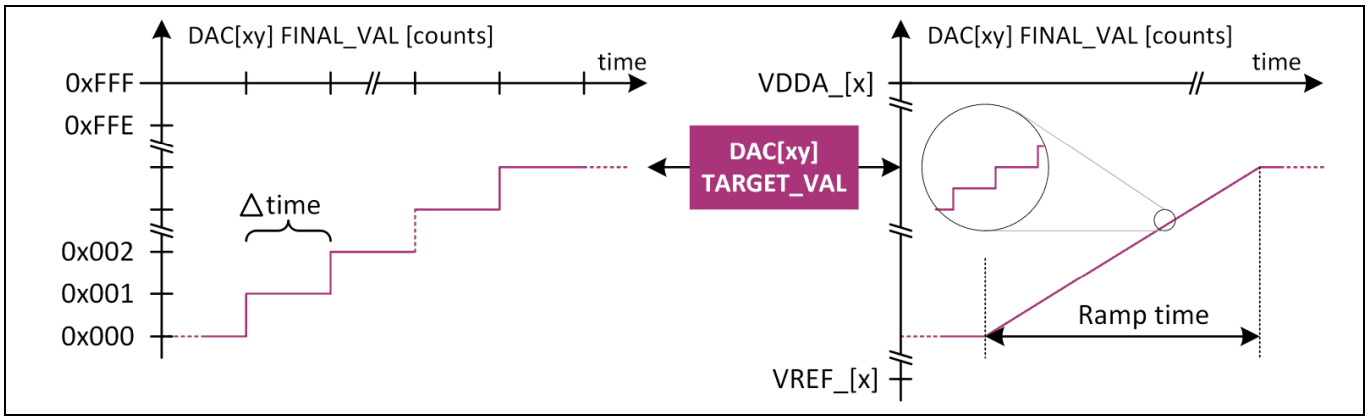


Figure 30 DAC Sloping

If e.g. the software set DACCTRL.SLP = 1 = 1us per DAC count and the DAC_[xy].VALUE was programmed to 1900 (=0x76C) it will take 1900us to update DAC_[xy].VALUE to its final value.

4.6.7 DAC Value Step #5: Clamp Compensation + Limit

The DAC outputs connected to bias switches (DAC_x0 and DAC_x2) can be configured to compensate for unwanted transitional effects at RF transistor turn-on event, which could be potentially caused by:

- too small capacitor at DAC_xy;
- too high load at OUT_xy;
- thermal settling effects;
- trapping effects in GaN devices;
- etc.

As countermeasure the device can temporarily increase the output voltage at the DAC_xy pins, depending on the state of EN_OUT_x (to enable this feature CCOMP_xy.EN =1, where x=[A;B], y=[0;2]):

• While EN_OUT_x is low, the output voltage at DAC_xy is incremented with a fast transition (1 step per 50ns) up to an amplitude defined in CCOMP.AMP (delta value to DAC_xy.VALUE).
• After detecting a rising edge at EN_OUT_x, the output DAC_xy is decremented again down to its initial value (delta value = 0) with a transition defined in CCOMP.SLP (1 step per CCOMP.SLP * 1us).
• In case CCOMP.SLP = 00h, there will be just a minimum delay (50ns) between the steps counting down.
• In case the decrement is interrupted by another falling event at EN_OUT_x, the DAC_xy output is immediately incremented to the desired AMP.

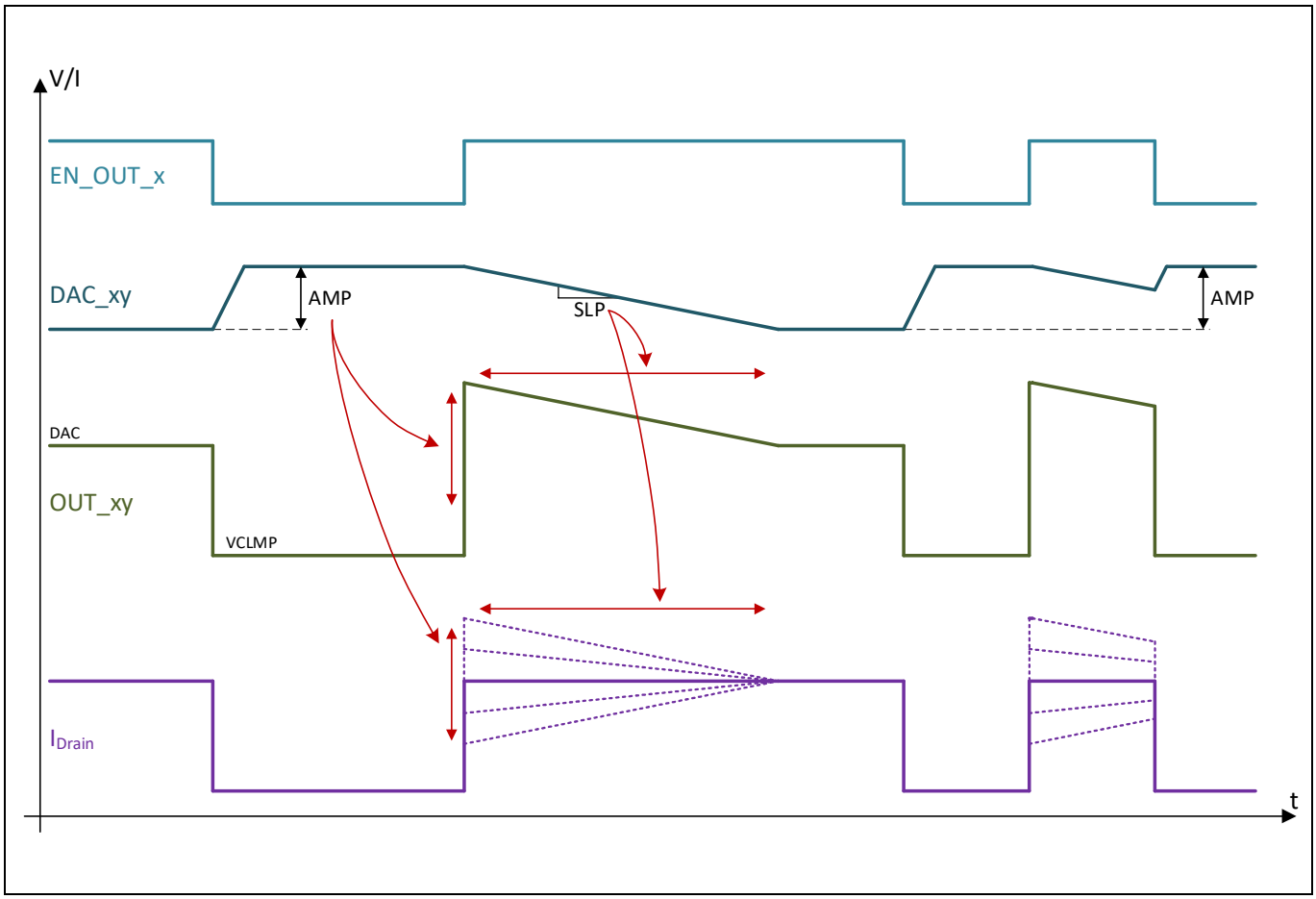


Figure 31 DAC clamping compensation

4.6.8 DAC Value: Read Back Calculated Value

To verify the actual calculated value DAC[xy] FINAL_VAL applied to a DAC, it can be read via the digital interface. The register DAC_FB is used for this purpose. First, the register is used to tell the device from which channel the DAC_[xy] FINAL_VAL is requested. To do so one of the following values needs to be written to it:

Side	Channel	Bit 14 DAC_SIDE	Bits 13:12 DAC_CH	DAC_FB
A	0	0	00	0x0000
A	1	0	01	0x1000
A	2	0	10	0x2000
A	3	0	11	0x3000
B	0	1	00	0x4000
B	1	1	01	0x5000
B	2	1	10	0x6000
B	3	1	11	0x7000

Figure 32 DAC_FB Channel Selection

If e.g. the DAC_B2 FINAL_VAL is of interest then DAC_FB needs to be written with 0x6000 first. After the write access the same register can be read. DAC_FB.VALUE will now contain the value for DAC_B2 FINAL_VAL. Masking the bits 15:12 by e.g. by doing DAC_FB.VALUE & 0x0FFF returns purely the DAC value. Reading the register another time will always return the most recent value for DAC_B2 FINAL_VAL.

4.7 Clamping

In reset mode and during startup the clamping potential is connected to VREF_[x] input. In active mode clamping voltage can be selected from:

- neighboring odd DAC (e.g. for DAC_A0 neighboring DAC is DAC_A1 etc.);
- 6-bit offset DAC (clamp buffer) adding a delta voltage up to 1.41V to an even channel;
- reference potential VREF_[x].

When clamping is engaged (triggered by EN_OUT_[x] input or forced by OUT_CTRL_[xy] setting), a configured clamping voltage is presented at OUT_[xy] output. This is used to quickly close the RF transistor into its pinch-off region. When clamping is disengaged, the OUT_[xy] presents corresponding DAC_[xy] voltage, which sets RF transistor bias point. The following figure gives an overview about the register bits and their influence on clamping.

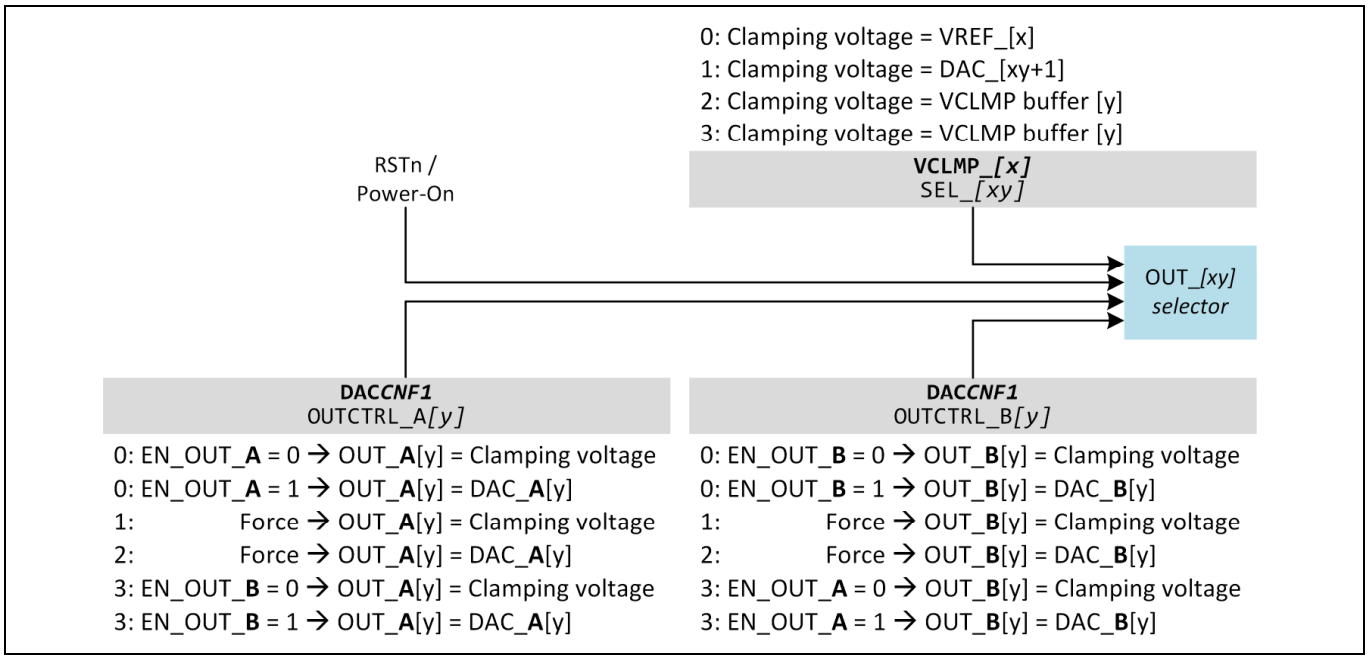


Figure 33 OUT_[xy] Selection

4.7.1 Clamping Using VREF

When setting VCLMP_[x].SEL_[xy] = 0 then VREF_[x] defines clamping potential for the corresponding OUT_[x][even] output:

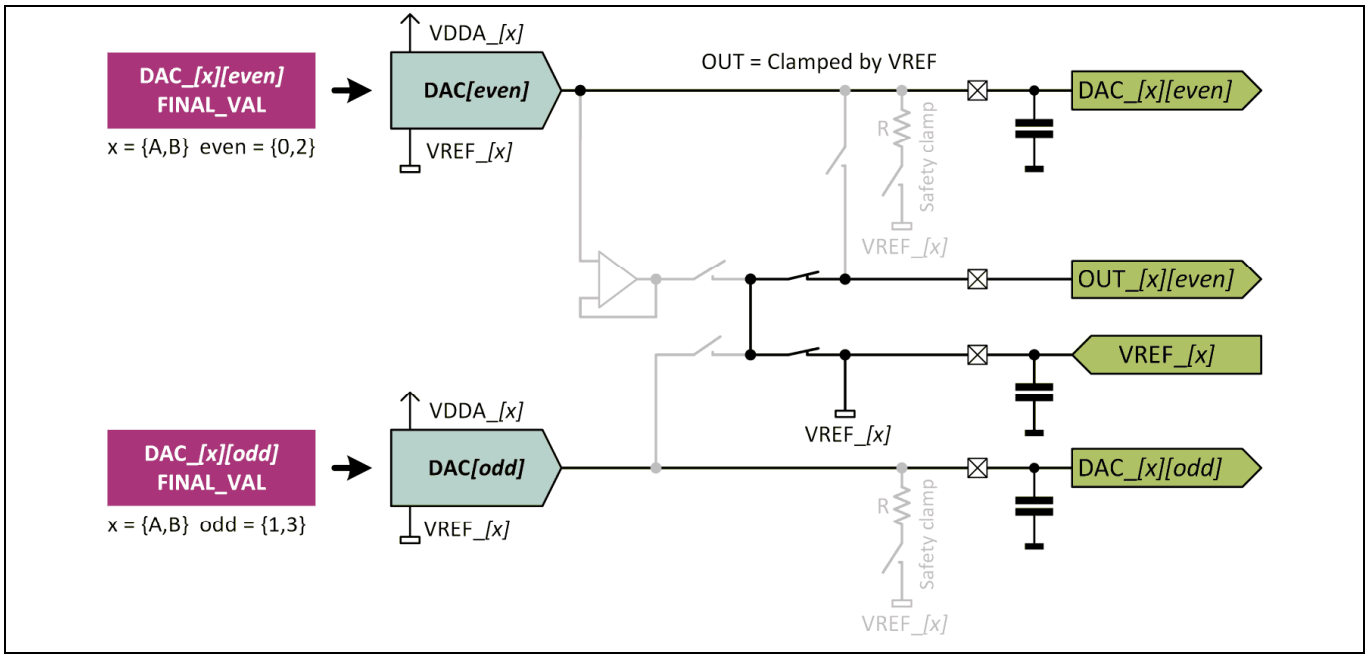


Figure 34 Clamping Using VREF

4.7.2 Clamping Using Neighboring Odd DAC

When setting VCLMP_[x].SEL_[xy] = 1 the neighboring DAC defines the clamping potential. E.g. for DAC_A0 the neighboring DAC is DAC_A1 etc.

Range and offset settings for the odd DACs are ignored but the corresponding even DAC settings are used. When e.g. DAC_A1 is used as a clamping DAC the settings DAC_A0.EN, DAC_A0.RNG and DAC_A0.OFF are used for DAC_A1:

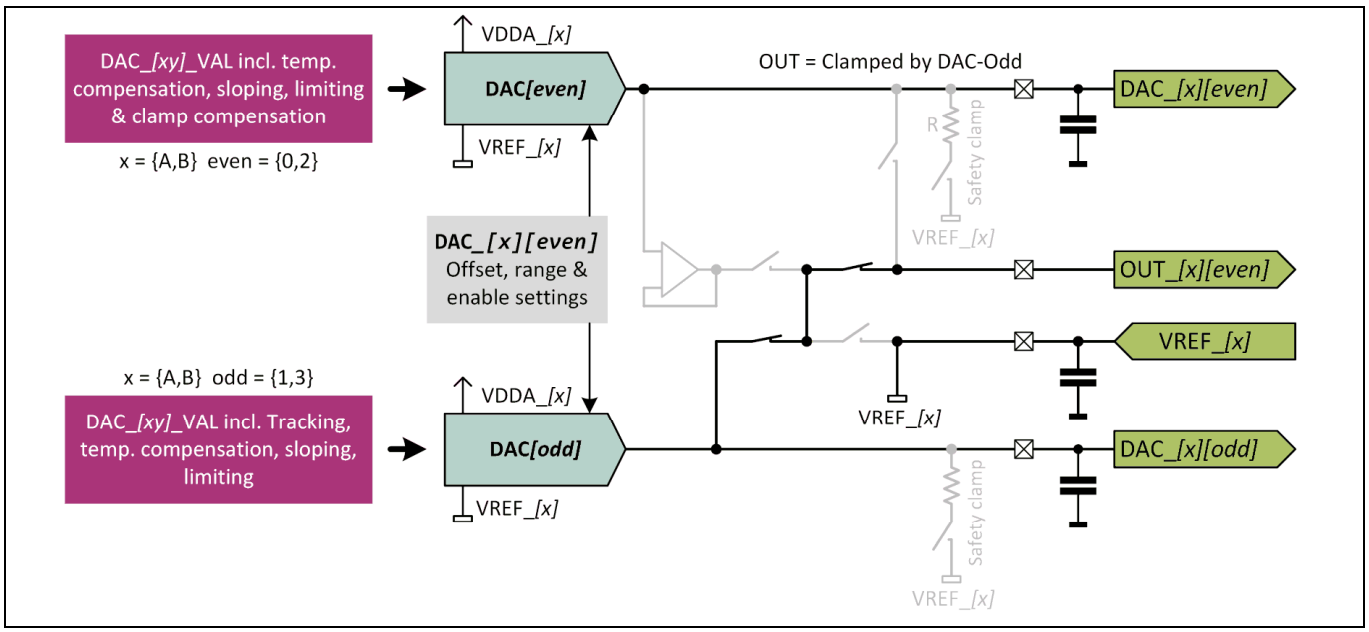


Figure 35 Clamping with Neighboring DAC

4.7.3 Clamping Using Clamp Buffer

When VCLMP_[x].SEL_[xy] = 2 or 3 an internal clamping buffer generates the clamping voltage for low current loads. The buffer tracks its corresponding DAC_[x][even] channel. This option offers a clamping voltage without sacrificing a neighboring DAC.

The voltage difference between the DAC and the clamping buffer is set with a granularity of 64 voltage steps by the 6-bit value in VCLMP.DVAL_[xy]. Each voltage step is 22.5mV (LSB_{CLMP}). In total the clamping voltage ($V_{CLMP\_[xy]}$) can be (64-1) · 22.5mV = 1.4175V lower than the DAC_x[even] voltage ($V_{DAC\_[xy]}$) which feeds the clamping buffer:

$$V_{delta\_[xy]} = V_{DAC\_[xy]} - V_{CLMP\_[xy]}$$

The following value needs to be written to VCLMP_x.DVAL_xy register entry:

$$VCLMP.DVAL\_[xy] = V_{delta\_[xy]} / LSB_{CLMP} = V_{delta\_[xy]} / 25mV$$

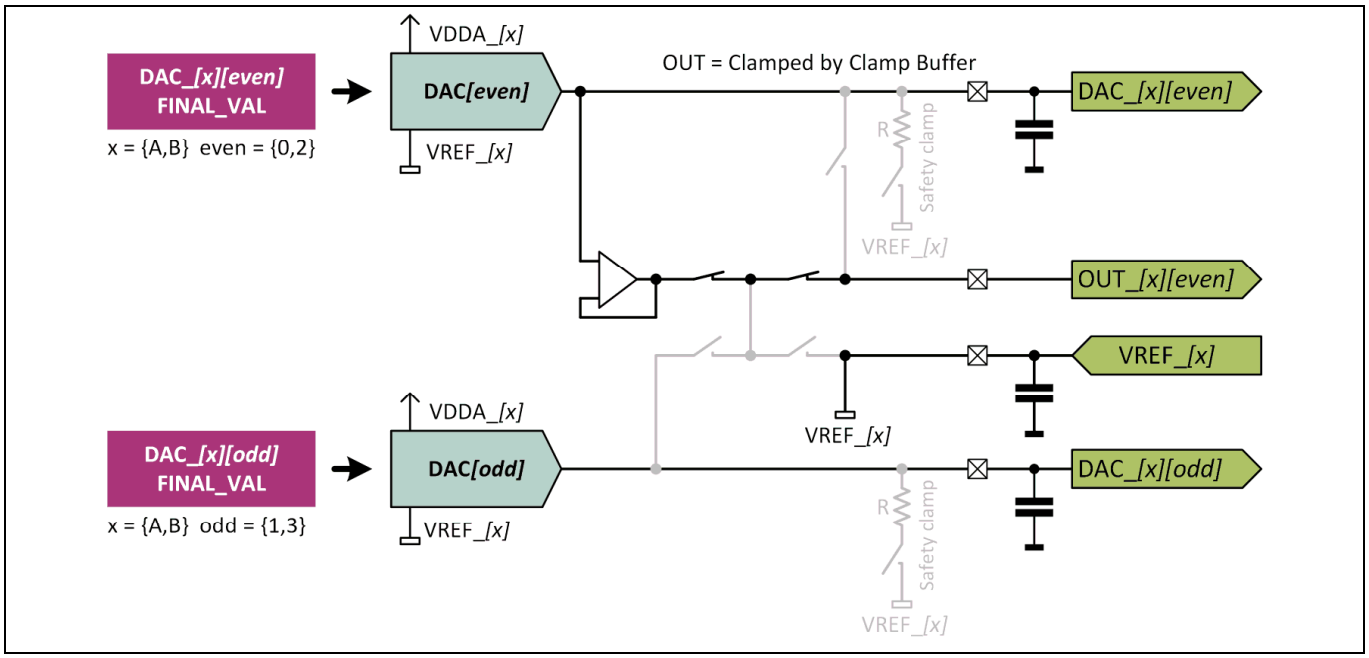


Figure 36 Clamping with Clamp Buffer

4.8 Voltage ADC

The Voltage ADC (VADC) is an 11-bit SAR ADC with several multiplexed inputs. VADC is using an internal reference voltage. Inputs are referred to GND:

- ADC0 / ADC1
- ISNS_A+ / ISNS_B+
- Supply inputs VDD / VDDP / VDDA_A / VDDA_B / VREF_A / VREF_B

The ADC is operated in round-robin scheme: once it's enabled, inputs are sampled and converted sequentially. The results are stored in corresponding separate registers:

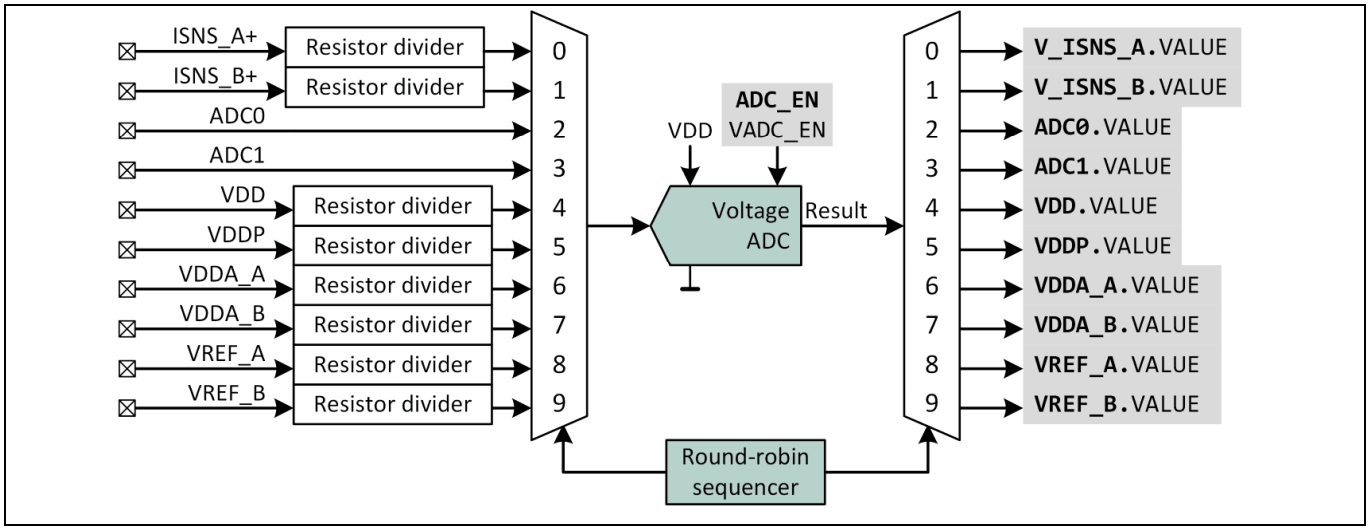


Figure 37 Voltage ADC

To translate the results into voltages the transfer functions in Table 15 can be used. Use the contents of the corresponding register (e.g. ADC0.VALUE) for VALUE and $V_{ref} = 1.213$ V to calculate the result. When using VALUE = 1 an LSB can be calculated:

Table 15 VADC Parameters

Pin	ADC Channel	Full-Scale	LSB size	Register VALUE	Transfer Function (for ADC result)
ISNS_A+	Ch 0	61.46 V	30.02 mV	V_ISNS_A	$20 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
ISNS_B+	Ch 1	61.46 V	30.02 mV	V_ISNS_B	$20 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
ADC0	Ch 2	3.073 V	1.50 mV	ADC0	$1 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
ADC1	Ch 3	3.073 V	1.50 mV	ADC1	$1 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
VDD	Ch 4	5.745 V	2.81 mV	VDD	$430 \div 230 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
VDDP	Ch 5	3.73 V	1.82 mV	VDDP	$340 \div 280 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
VDDA_A	Ch 6	8.561 V	4.18 mV	VDDA_A	$390 \div 140 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
VDDA_B	Ch 7	8.561 V	4.18 mV	VDDA_B	$390 \div 140 \cdot 512 \div 202 \cdot V_{ref} \div 2^{11} \cdot VALUE$
VREF_A	Ch 8	-8.4 V	-4.15 mV	VREF_A	$7 \cdot (-1.2 + V_{ref} \div 2^{11} \cdot VALUE)$
VREF_B	Ch 9	-8.4 V	-4.15 mV	VREF_B	$7 \cdot (-1.2 + V_{ref} \div 2^{11} \cdot VALUE)$

The voltage at ADC0 and ADC1 can be used to monitor device-external voltages. The maximum voltage is $FSR_{VADC,ADC}$ which is typically 3.07 V. In case a higher voltage needs to be monitored a resistor divider (green dashed line) is required. Additionally an RC-filter (blue dashed line) can be added if required:

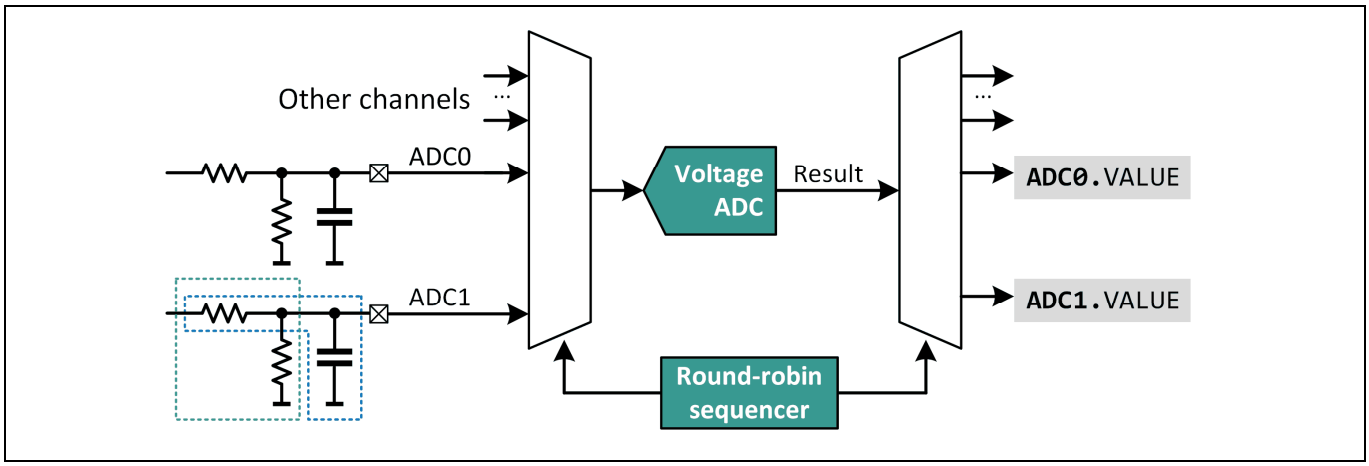


Figure 38 Reference Design Voltage ADC

4.9 Current Shunt ADC

The Current Shunt ADC (CSA) is capable of sampling the voltage across an external shunt directly, without the need of a shunt amplifier. The floating input stage enables a fully-differential measurement across the entire common mode input range ($I_{SNS\_[x]+}$ – $I_{SNS\_[x]-}$) from 0 V up/down to +/-60 V.

The differential voltage across the I_{SNS} pins (V_{SNS}) is limited to +/-1 V. In applications where a higher differential voltage can occur (e.g. during error conditions) an optional resistor (R_{opt_a}) can be added to limit the I_{SNS-} current (maximum 120 mA) into an I_{SNS_A}/ I_{SNS_B} pin:

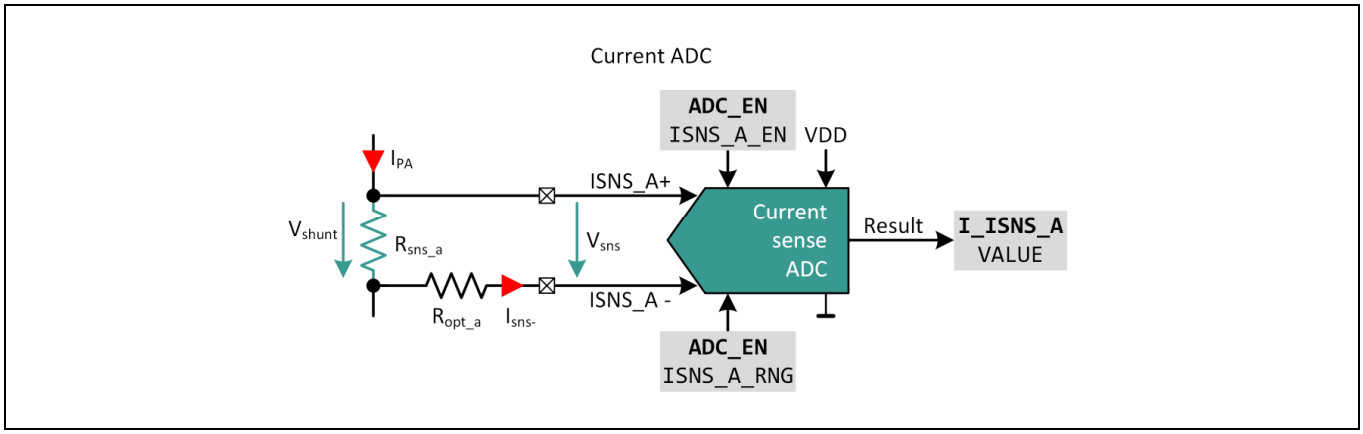


Figure 39 Current Shunt ADC

For optimal matching to the external shunt different full scales can be programmed. Please be aware that due to the architecture of the ADC the theoretical full-scale can only be used considering a non-linear distortion:

Table 16 CSA ranges and LSB

Range	-3dB full scale	Theoretical full scale	LSB_{range}
15 mV	±13.6 mV	±19.25 mV	9.4 µV
30 mV	±27.2 mV	±38.5 mV	18.8 µV
60 mV	±54.4 mV	±77 mV	37.6 µV
120 mV	±108.8 mV	±154 mV	75.2 µV
240 mV	±217.6 mV	±308 mV	150.4 µV

The CSA transfer function is:

$$V_{SNS} = VALUE \cdot LSB_{range}$$

where:

- VALUE is the content of the corresponding register I_ISNS_A.VALUE or I_ISNS_B.VALUE
- LSB_{range} is defined by Table 16

It's important to note that V_{SNS} result is fully differential. Depending on the voltage presented to I_{SNS_A} / I_{SNS_B} pins the CSA will return a positive or negative result. The result is provided as a signed integer in two's complement format as shown in Figure 40:

	11	10	9	8	7	6	5	4	3	2	1	0
	Value											
+FS - 1	0	1	1	1	1	1	1	1	1	1	1	1
+FS - 2	0	1	1	1	1	1	1	1	1	1	1	0
…	…	…	…	…	…	…	…	…	…	…	…	…
1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1	1
-2	1	1	1	1	1	1	1	1	1	1	1	0
…	…	…	…	…	…	…	…	…	…	…	…	…
-FS	1	0	0	0	0	0	0	0	0	0	0	0

Figure 40 I_ISNS_A.VALUE / I_ISNS_B.VALUE result mapping

4.10 DTS: Die Temperature Sensor

This device offers a die temperature sensor (DTS). Once enabled via the ADC_EN.DTS_EN bit the DTS measures the temperature continuously and stores the result in the TEMP.TEMPERATURE register. The update occurs after $t_{DTS,conv}$ (max. 5ms). The following equation can be used to determine the actual temperature in °C:

$$T\,[°C] = 0.7648°C \cdot TEMP.TEMPERATURE - 80.497°C$$

Some example values are given in the table below:

Decimal	Hex	Bin	Temperature	Decimal	Hex	Bin	Temperature	Decimal	Hex	Bin	Temperature
53	035	000110101	-40.0	141	08D	010001101	27.3	218	0DA	011011010	86.2
85	055	001010101	-15.5	151	097	010010111	35.0	250	0FA	011111010	110.7
86	056	001010110	-14.7	152	098	010011000	35.8	251	0FB	011111011	111.5
118	076	001110110	9.7	184	0B8	010111000	60.2	283	11B	100011011	135.9
119	077	001110111	10.5	185	0B9	010111001	61.0	284	11C	100011100	136.7
130	082	010000010	18.9	217	0D9	011011001	85.5	316	13C	100111100	161.2

Figure 41 DTS Temperature Value Examples

Since the DTS is also used by the temperature compensation mechanism it is possible to manually overwrite the temperature value. This allows to verify the temperature compensation. To overwrite the temperature value DTS needs to be disabled via the ADC_EN.DTS_EN bit:

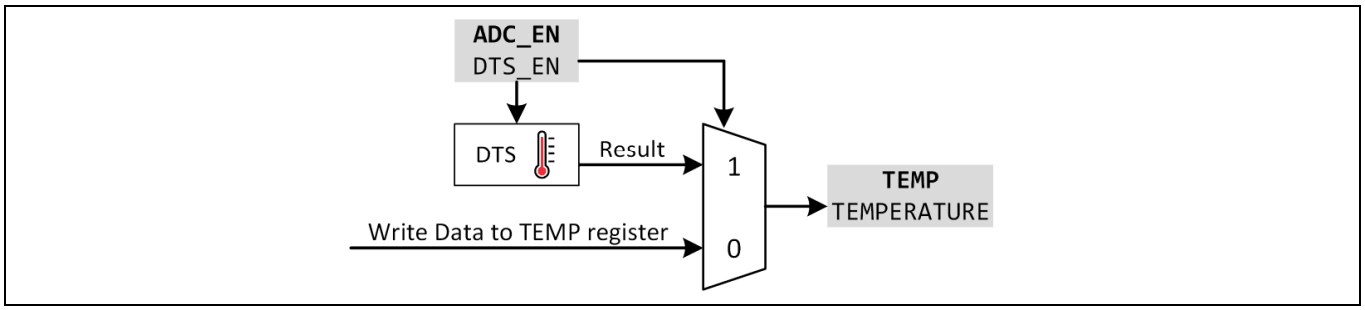


Figure 42 DTS Temperature Overwrite

5 Application and Implementation

For the sake of simplicity this chapter assumes application cases which require DAC output voltages of +3.6V and -3.6V at 27.3°C. Over temperature the DAC voltage must range only a few tens of millivolt to ensure a stable bias point for the RF transistor. The DAC voltages for biased and pinch-off mode differ by ≤1V. Under all conditions approximately 20mA need to be sourced and sinked.

5.1 DAC Basic Settings Overview

It is recommended to program the DAC related registers in the following order:

- DAC_[xy].RNG: Output voltage range either 3.5V or 7.0V. The DAC resolution (12-bit) divides this range into 2^12 – 1 = 4095 voltage steps (0.855mV for 3.5V and 1.71mV for 7V)
- DAC_[xy].OFFS: Offset voltage with respect to VREF_[X]. It can be either [0V; 0.5V; 1.5V; 2.5V] for 3.5V range or [0V; 1V] for 7V range
- DAC_[xy].VALUE: Offset plus DAC value results in the desired output voltage (temperature compensation not considered)
- DACCNF2.LD[xy]: DAC current drive capability and stability

Some DAC channels allow toggling between two voltages in order to clamp RF transistors. In the actual application mainly the signals EN_OUT_A and EN_OUT_B are used for this purpose. Furthermore during software debugging phase it may be necessary to force DACs to fixed values independent of EN_OUT_A or EN_OUT_B.

Below is a list of registers to be configured when using the clamping/forcing feature for the OUT_[xy] channels:

- DACCNF1.OUT_CTRL_[xy]: Clamp enabled by either EN_OUT_A = 0, EN_OUT_B = 0, never or always
- VCLM_[x].SEL_[xy]: Clamping voltage can be chosen from VREF_[x], DAC_[xy] or internal clamping buffer
- VCLMP_[x].DVAL_[xy]: Defines 6-bit offset voltage when using VCLMP buffer as clamping voltage

It is also possible to have DAC channels track other DAC channels. This can become useful when one RF-transistor bias point requires a fixed offset to another transistor. Then the following registers can be programmed:

- DACCNF1.TRK_A1toA0 … DACCNF1.TRK_B3toB2: Odd DAC channels track their neighboring even channels

5.2 DAC Value, Offset and Range

The following sections show the bit settings required for the example scenario defined earlier in this chapter. The settings are explained for only one DAC channel A and B:

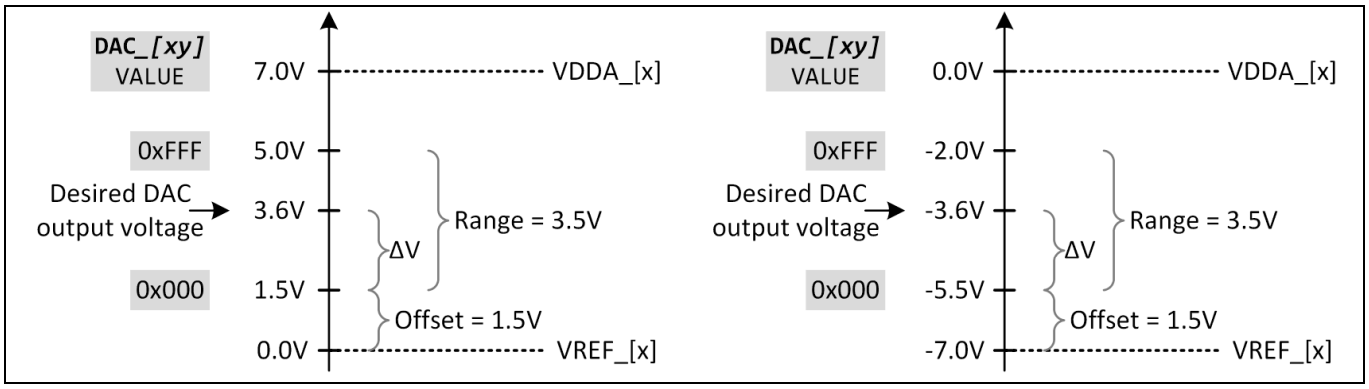


Figure 43 Parameters and their Influence on DAC Output Voltage

The DACs offer either 3.5V (DAC_[xy].RNG = 0) or 7.0V (DAC_[xy].RNG = 1) voltage range. Therefore DAC_[xy].RNG should be 0 to select 3.5V.

The required source current of 20mA allows DAC output voltages up to 1V lower than VDDA_[x] (see $I_{src, hi}$).
The required sink current of 20mA allows DAC output voltages up to 1V higher than VREF_[x].

For this application a voltage offset of >=1V will ensure proper functionality. The following voltage offsets can be selected by DAC_[xy].OFFS although the value 2 is recommended for this example:

- 0 = 0V offset: DAC voltage range is 0V…3.5V which is not sufficient for the desired DAC voltage of 3.6V
- 1 = 0.5V offset: DAC voltage range is 0.5V…4.0V which is just sufficient for the desired DAC voltage of 3.6V
- 2 = 1.5V offset: DAC voltage range is 1.5V…5.0V which is perfect for the desired DAC voltage of 3.6V
- 3 = 3.0V offset: DAC voltage range is 3.0V…6.5V which is just sufficient for the desired DAC voltage of 3.6V

The DAC value is used to generate a DAC voltage relative to VREF_[x] and the offset voltage set by DAC_[xy].OFFS (=ΔV). The following equation can be used to calculate the DAC value:

$$\text{DAC\_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V \qquad \Delta V = \text{DAC\_Voltage} - \text{Offset} - \text{VREF\_[x]}$$

Figure 44 DAC Value Calculation Equation

In this example the DAC voltage should be 3.6V. The desired DAC range is 3.5V and the offset 1.5V. Therefore, the DAC_[xy].VALUE register needs to have the value 2457 = 0x999:

$$\text{DAC\_[xy].VALUE} = \frac{4095}{\text{Range}} \cdot \Delta V = \frac{4095}{3.5V} \cdot 2.1V = \underline{\underline{2457}} \qquad \Delta V = 3.6V - 1.5V - 0V = 2.1V$$

Figure 45 DAC Value Positive Calculation Example

The same example but with negative values: DAC output voltage needs to be -3.6V. The desired DAC range is 3.5V and the offset 1.5V. The DAC_[xy].VALUE register needs to have the value 2223 = 0x8AF:

$$DAC\_[xy].VALUE = \frac{4095}{Range} \cdot \Delta V = \frac{4095}{3.5V} \cdot 1.9V = \underline{\underline{2223}} \qquad \Delta V = -3.6V - 1.5V - (-7V) = 1.9V$$

Figure 46 DAC Value Negative Calculation Example

5.3 DAC Source/Sink Current Setting

Depending on the capacitors connected to the DACs as well as the currents to be sourced/sinked the DACCNF2.LD_[xy] need to be set accordingly. When the current exceeds $I_{src, hi}$ or $I_{snk, hi}$ then DACCNF2.LD_[xy] needs to be set to 1 to support high current mode. Here 20mA for source/sink current are required. Therefore high current mode is selected.

For lower currents DACCNF2.LD_[xy] needs to be set to 0 to support normal mode. Only when capacitors smaller than 100nF (low cap mode) are used DACCNF2.LD_[xy] needs to be set to 2.

5.4 DAC Enable

After all DAC settings have been programmed the DACs can be enabled by setting the corresponding DAC_[xy].EN bit.

When capacitor values higher than $C_{DAC\_[xy]}$ are used a sequential turn-on or a slow DACCNF1.SLP setting for the DACs is recommended in this case to avoid overheating. Ideally one DAC is enabled at a time and the next one is enabled after the previous reached its target voltage.

6 I2C/I3C Serial Digital Interface

This device supports I3C communication and is backwards compatible to I2C. The pads of the digital interface use VDDP and connect to the digital core logic. This logic runs on a voltage derived from VDD using a voltage regulator (VREG). Therefore an undervoltage of any of the two voltages makes the interface unavailable.

VDDP is typically chosen to be 1.8V but it can also handle 3.3V. All digital I/Os (ADR0, ADR1, SCL, SDA, RSTN, EN_OUT_A, EN_OUT_B) need to use the same voltage as VDDP.

The I3C-interface of the Bias and Control IC is configured as slave device supporting all modes up to HDR-DDR, ternary symbol modes (HDR-TSL or HDR-TSP) are not supported. This leads to specified data rates up to 25MBit/s. The implementation was done according to MIPI Standard v1.0. Details on the protocol can be found on the MIPI webpage: https://www.mipi.org/specifications/i3c-sensor-specification. In all available modes, the slave interprets the first two bytes of data written to it by the master as the register address. This feature is called 'sub-addressing', and it is not explicitly defined by the MIPI I3C specification. The interface provides backward compatibility with the I2C protocol.

After RSTN release the digital interface will be in I2C mode until the first I3C message is recognized (Dynamic Address assignment). Once the digital interface has switched to I3C mode it will remain in this until it gets reset.

6.1 I2C Address Selection

Each I2C-device requires a unique address at which it can be reached. Each communication to a slave with an invalid address will remain unacknowledged.

This device offers address selection pins ADR0 and ADR1 to choose between addresses ranging from 0x40 to 0x47. The three logic levels are defined as follows:

- low: short to GND
- high: short to VDDP
- open: floating (VDDP/2)

To avoid external components for VDDP/2 internal pull-resistors are connected to the ADR0/1 pins. They will be active during power-on conditions plus additional 8µs. After that time the slave address is fix during normal operation (no power-on reset or reset). Therefore the pull-resistors are disconnected to avoid extra current between VDDP and GND. In case external pull resistors shall be used their value shall be <=100 Ohm (ADR_{PULL}). The three input states for each pin allow the following addresses to be selected:

Table 17 I2C Device Address truth table

ADR1	ADR0	I2C address ($+40_h$)
low	low	0
low	open	0
low	high	1
open	low	2
open	open	3
open	high	4
high	low	5
high	open	6
high	high	7

In Figure 47 the functional building blocks for the address selection are shown:

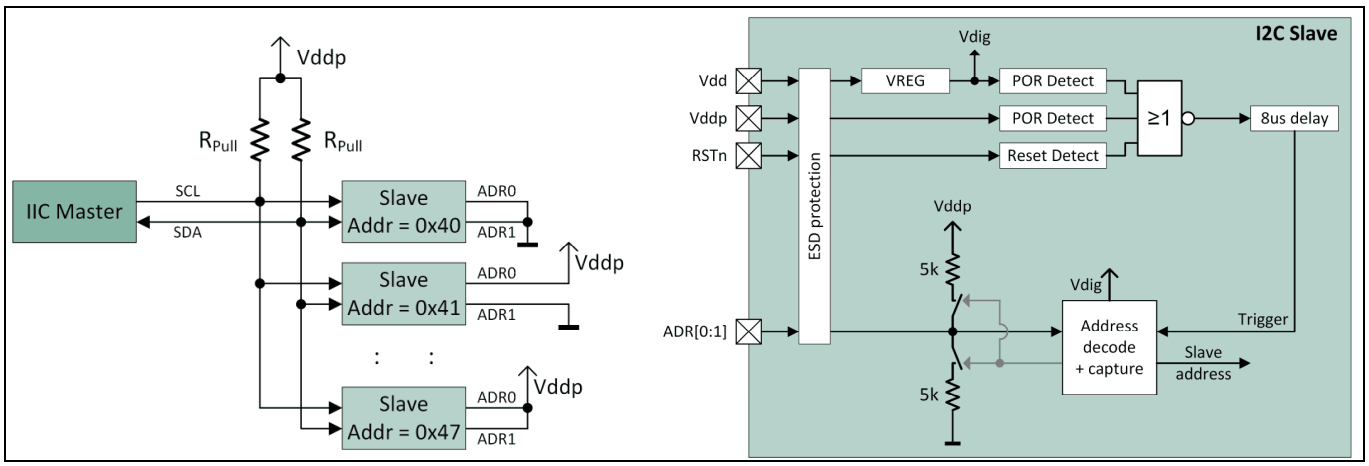


Figure 47 I2C Address Selection

6.2 I2C Design Considerations

For a proper communication it is important that Master and Slave can both drive data reliably. The SCL will only be driven by the Master as this Slave does not support clock stretching etc. Therefore it is possible that the Master drives SCL by a push-pull digital pin (GPO). In case an Open-Drain pin is used a pull-up is required (shown in grey). In the latter case pull-up and the capacity connected to it will be the only design factor to consider. This is described for the SDA pin in greater details.

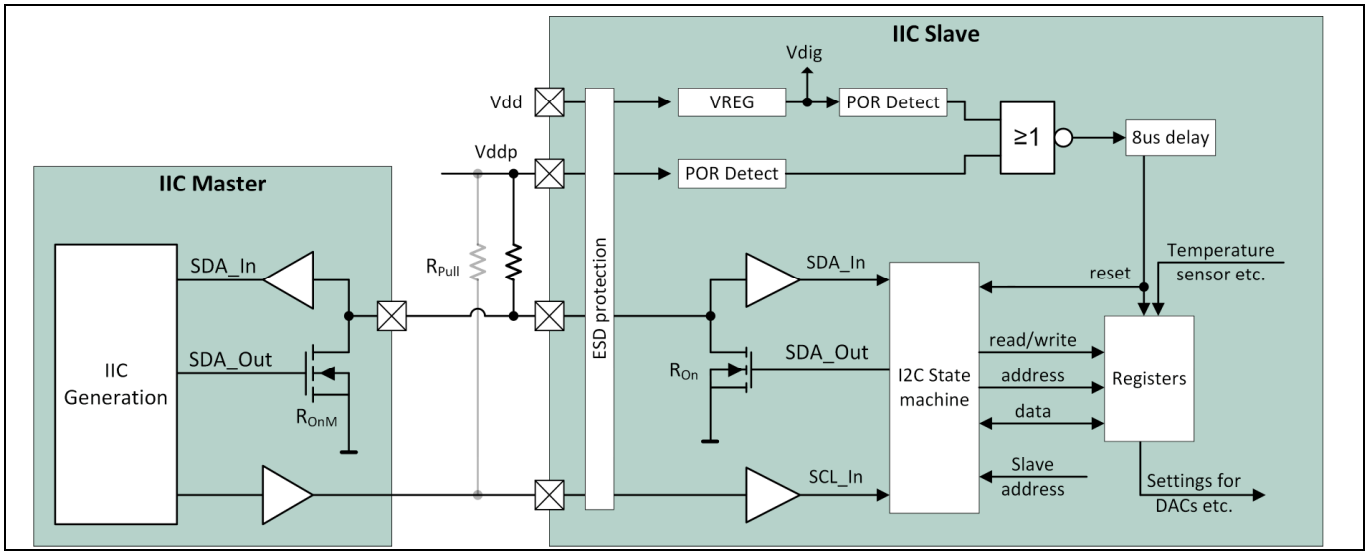


Figure 48 I2C Structure

The SDA pin is bi-directional which means it can be driven either by the Master or by the Slave. When handing over the driving authority from one to the other spikes and dips may occur on the SDA line. Such a handover happens when e.g. a Slave needs to acknowledge a byte sent by the Master. The SDA line is expected to change during the SCL low phase and remain stable during SCL high phase (see Figure 49 green area). Additionally there is a spike filter that swallows pulses (high or low) smaller than 60ns. Still care should be taken to avoid excessive crosstalk between SCL and SDA.

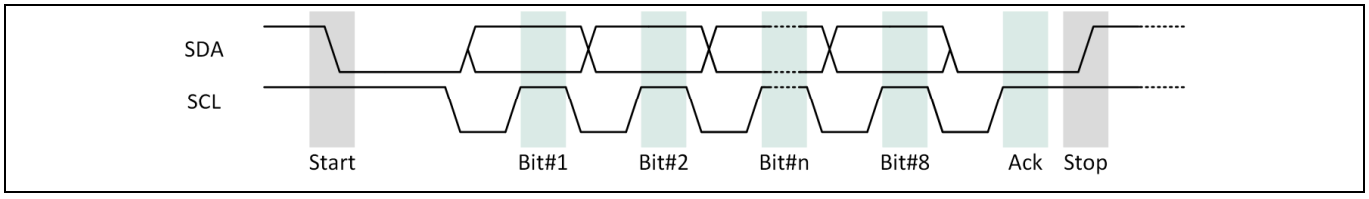


Figure 49 I2C Sample Phase

When data is sent on the SDA line the driver must be strong enough to drive a valid low as well as releasing the line in time to allow the external pull-up resistor to pull high. All capacitance connected to the line, the inner driver strength as well as the pull-up resistor need to be considered:

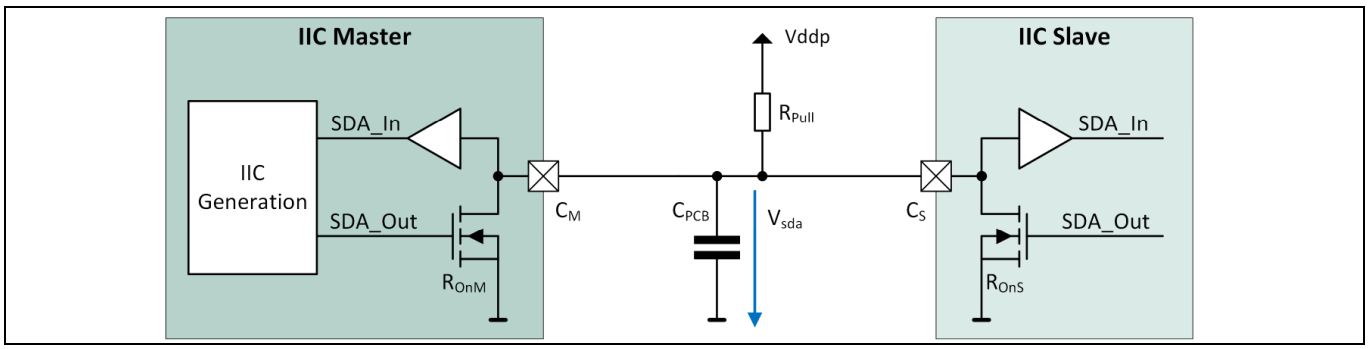


Figure 50 I2C SDA Driver Considerations

The required equations to calculate pull-up resistors, voltage levels and ramp times are given in the following overview:

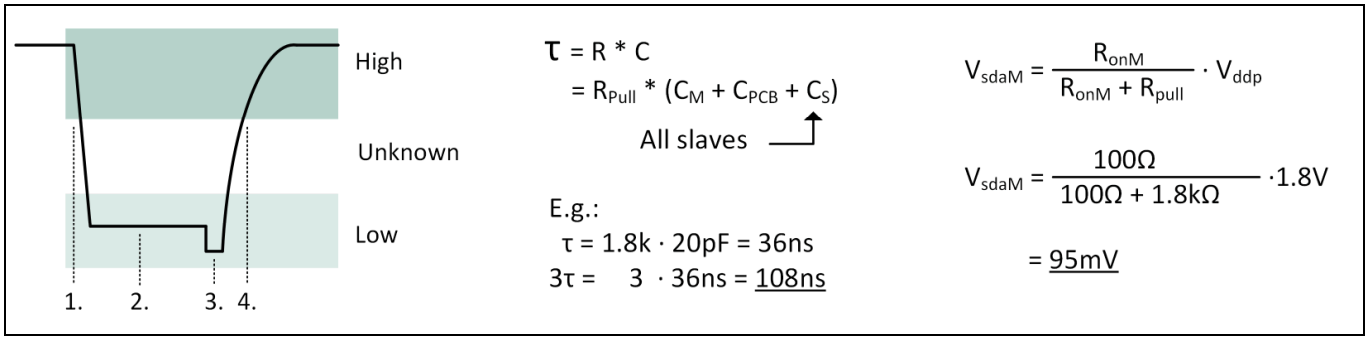


Figure 51 I2C Timing Equations

In this example the pull-up resistor is 1.8kOhm and the transistor which pulls low has 100Ohm on-resistance (R_{onM} and R_{onS}).

When e.g. the Master drives low (phase #2 in Figure 51 on the left) it drives against the pull-up resistor. This creates a voltage divider as described by the equations shown in Figure 51 on the right. The actual voltage on the SDA line for the Low level is approximately 95mV. Even for lower pull-up resistor values this is typically no problem. The fall-times are usually <=50ns.

When e.g. the Master drives a High after a Low it shuts off the transistor that pulls low. Now the pull-up resistor takes over and will charge the line and all the capacity attached to it. The total capacity consists of the pin capacities of the Master, the Slave(s) and the PCB trace. The charging looks like an RC-charging curve (phase #4 in Figure 51 on the left). The time constant is given by the equation in Figure 51 in the middle. One time constant τ reflects 63% VDDP, 2τ 86% and 3τ 95%. While 1τ may still be marginal 2τ or even 3τ are sufficient to be detected as a solid logic high. In this example τ = 36ns and therefore 2τ = 72ns and 3τ = 108ns. The charge times may appear slow but they are still far away from becoming an issue. Even for communication speeds of 1MHz there is enough time to ensure a proper High. At 1MHz one SCL clock cycle lasts 1us and therefore half a clock cycle lasts 500ns. This is the time during which the data on SDA needs to settle. When planning for a decent guard band of e.g. 100ns there are still 400ns left for the high to settle.

When one driver hands over the SDA line to the other, e.g. Master hands over to Slave while waiting for the Slave to acknowledge, it is possible to see spikes and glitches during this time (phase #4 in Figure 51 on the left). Whether these will be spikes or dips and also their duration very much depends on the timing and driving capability between Master and Slave(s) as well as on the SDA data itself.

6.3 I2C Communication

6.3.1 I2C Dummy access

During and after a power-on of VDD or VDDP the I2C interface remains in a state which blocks all I2C communication and therefore no data can be acknowledged. Depending on the I2C implementation in the Master such a non-acknowledge may cause the Master to get stuck while waiting for the slave to acknowledge.

To leave this blocked state at least the following options exist:

- Send two or more clock pulses with SDA = '1'
- Send bus clear command where the master sends 9 clock pulses with SDA = '1'
- Make I2C read/write to a slave address that does not require such a dummy access
- Ping slave with one byte

After the blocked state is left the I2C operates according to the I2C specification[1]. The following figure shows an example for 'bus clear' and 'ping':

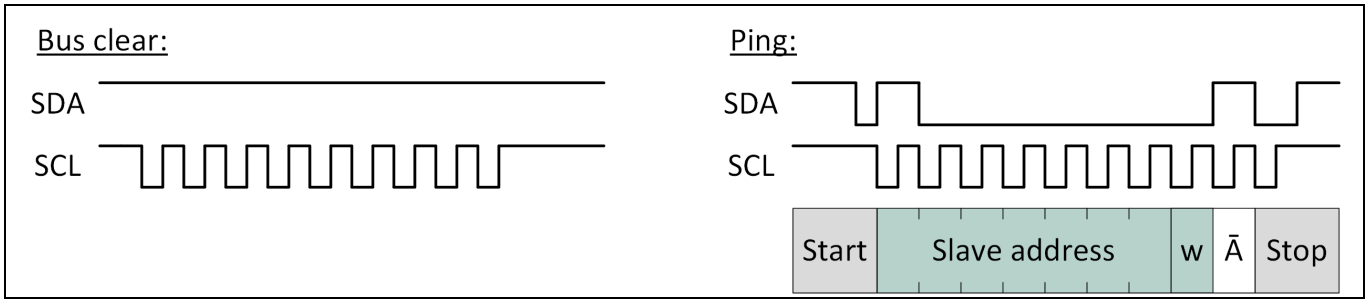


Figure 52 I2C Bus Clear & Ping

[1] https://www.nxp.com/docs/en/user-guide/UM10204.pdf

6.3.2 I2C Write access

There is the possibility of a single write access and block write access. A single write-access will allow writing to one 16-bit address while a block access allows multiple 16-bit accesses in a sequence:

Single Write Access:

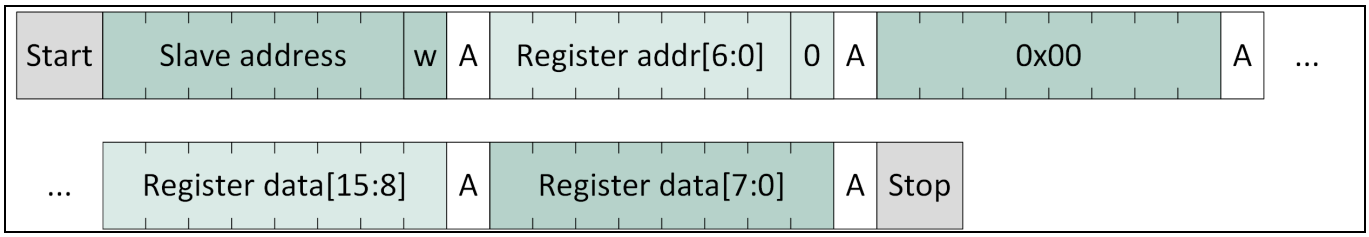


Figure 53 I2C Single Write Access

An example write access to register address 0x02 for I2C Slave address 0x40 with data 0x83A1 is shown in the figure below:

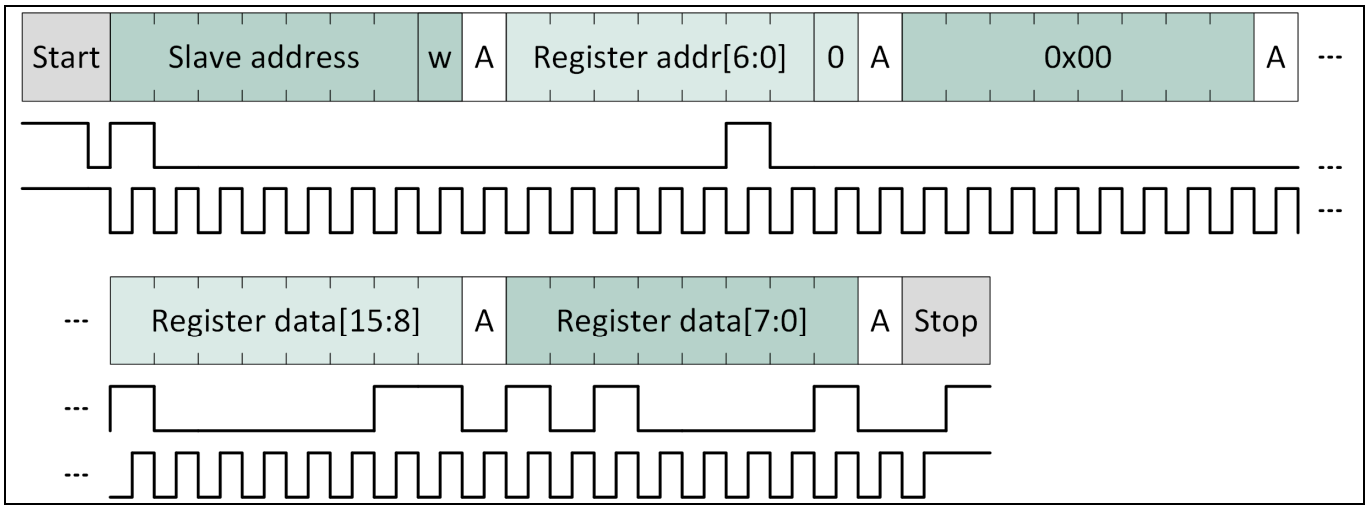


Figure 54 Single Write Access Example

A block write access is simply a single write access with additional bytes before the Stop condition:

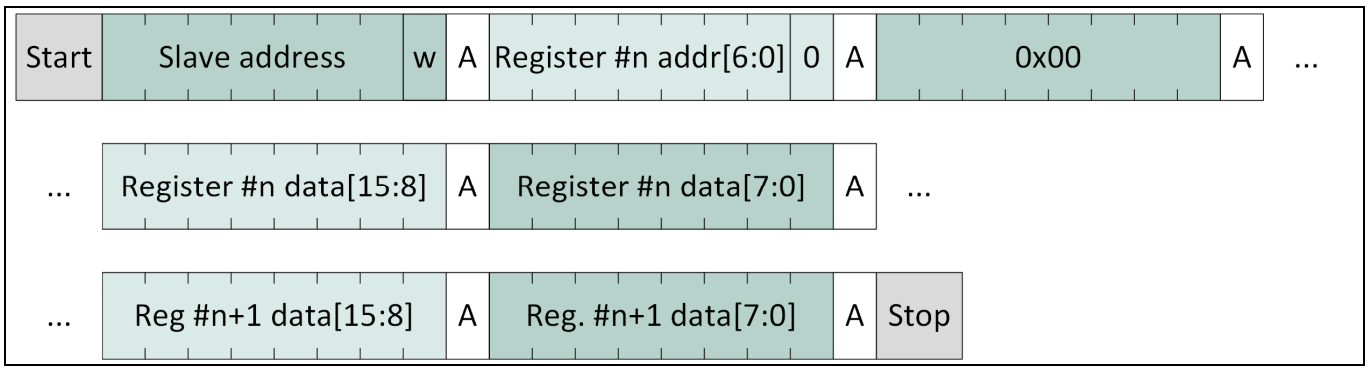


Figure 55 Block Write Access Example

6.3.3 I2C Read access

There is the possibility of a single read access and block read access. A single read-access will allow reading of one 16-bit address while a block access allows multiple 16-bit reads in a row:

Single Read Access:

Figure 56 I2C Single Read Access

An example read access from register address 0x02 for I2C Slave address 0x40 with read data 0x83A1 is shown in the figure below:

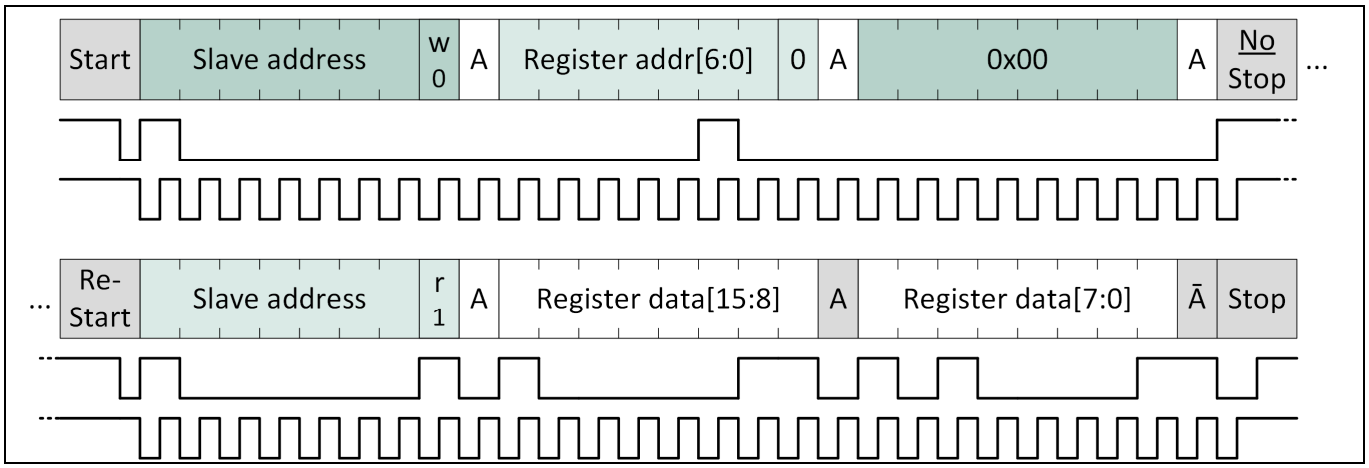


Figure 57 Single Read Access Example

A block read access is simply a single read access with additional read bytes before the NACK and Stop condition:

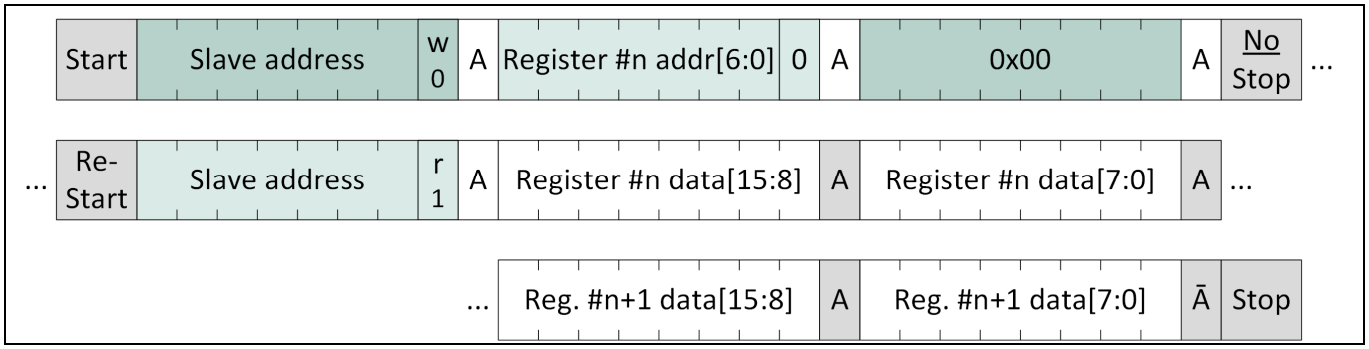


Figure 58 I2C Block Read Access

6.4 I3C Communication

This device is an I3C capable target and acts as an I2C device (with all the I2C limitations) before it gets its I3C Dynamic Address assigned. It fulfills the I3C Basic[SM] Specification version 1.0 from 19/JUL/2018. The following Dynamic Addressing modes are supported:

- ENTDAA
- SETDASA (assign target dynamic address) with limitations
- SETAASA

To communicate with the target using I3C the Primary Controller (Master) needs to execute the following steps:

- Set Dynamic Address for each target
- Read and/or write registers

These steps are described in the following chapters.

6.4.1 I3C Target Information

Some I3C commands require/deliver additional information about the target and its capabilities. At least the following commands do so:

- PID: Provisioned ID (used e.g. for ENTDAA or GETPID)
- BCR: Bus Characteristics Register (used e.g. for GETBCR)
- DCR: Device Characteristics Register (used e.g. for GETDCR)

The Provisioned ID (PID) looks like this:

- Bits[47:33]: 15-bit MIPI Manufacturer ID = 0x011A (Infineon)
- Bit [32] : Provisioned ID Type Selector = Vendor Fixed Value = 0x0
- Bits[31:16]: 16-bit Part ID = 0x0000
- Bits[15:12]: Instance ID = I2C address – 0x40 according to the ADR0 and ADR1 pins = 0x0 .. 0x7
- Bits[11:0]: 12-bit = 0x000

For an Instance ID = 0x**1** the PID is 0x0234_0000_**1**000 and for an Instance ID = 0x**5** the PID is 0x0234_0000_**5**000.

The 8-bit BCR register has the value 0x22 and looks like this:

- 7:6 = 0x0 = device is an I3C target
- 5 = 0x1 = device supports Advanced Capabilities
- 4 = 0x0 = device is not a virtual target
- 3 = 0x0 = device does not have low-power modes
- 2..1 = 0x1 = device supports in-band interrupts
- 0 = 0x0 = no data speed limitation

- The 8-bit DCR register has the value 0x00.

6.4.2 I3C Dynamic Address assertion using ENTDAA

One way to assign Dynamic Addresses to all targets can be done by using the ENTDAA command. The targets will answer one after the other. An answer includes PID, BCR and DCR. After those the Controller will provide the Target Dynamic Address with the next byte:

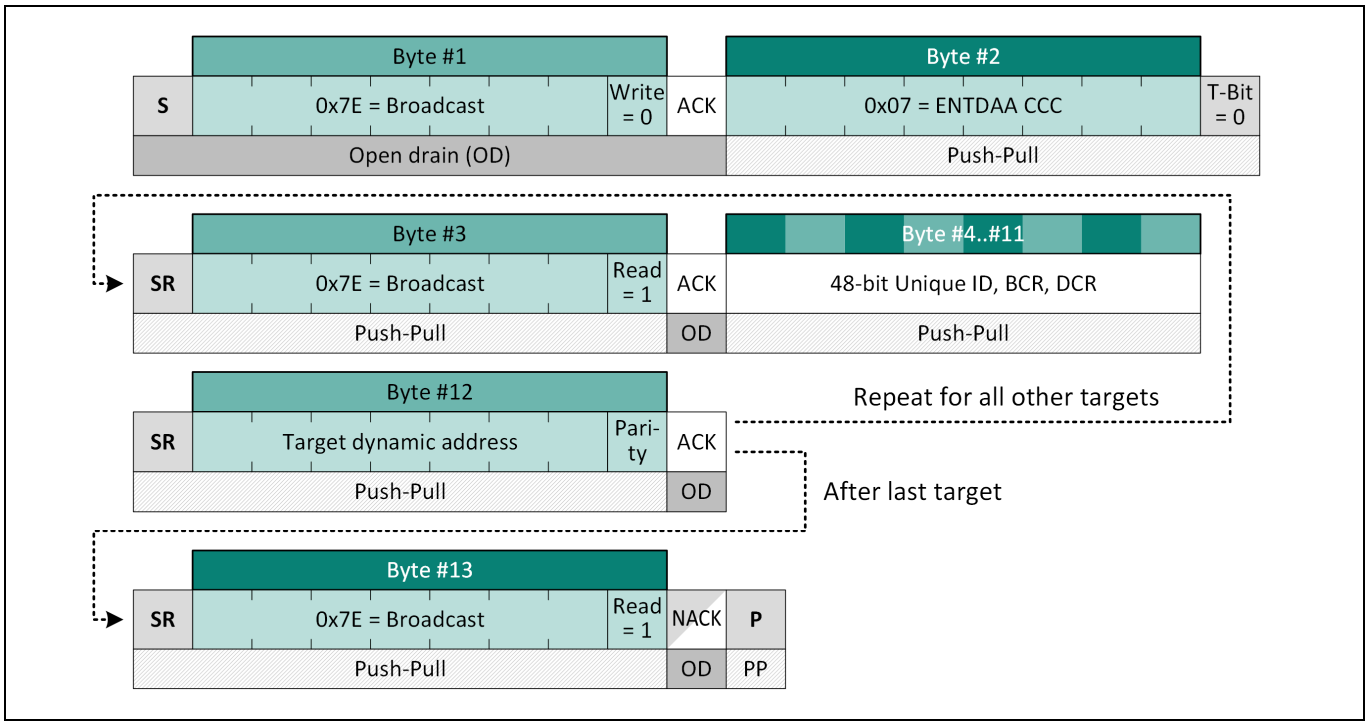


Figure 59 ENTDAA Command Structure

For a configuration with two targets (e.g. one target has I2C address 0x1 and one 0x5) the answer will be:

- Target 0x1: PID = 0x0234_0000_**1**000, BCR = 0x22, DCR = 0x00, Dynamic Address = 0x08
- Target 0x5: PID = 0x0234_0000_**5**000, BCR = 0x22, DCR = 0x00, Dynamic Address = 0x09

For two targets byte #3 to byte #10 (as shown in Figure 59) shall be repeated as byte #11 to byte #18 with the dynamic address for the second target. The last byte is another ‘0x7E + Read’ broadcast command. Since both targets will have received their dynamic addresses at this point no more target can acknowledge the broadcast. Therefore the Master will send “Stop”.

Please note that the Dynamic Address depends on the I3C Controller implementation.

6.4.3 I3C Dynamic Address assertion using SETDASA

With this command the Dynamic Address in a target can be set by addressing the Targets via their static I2C address:

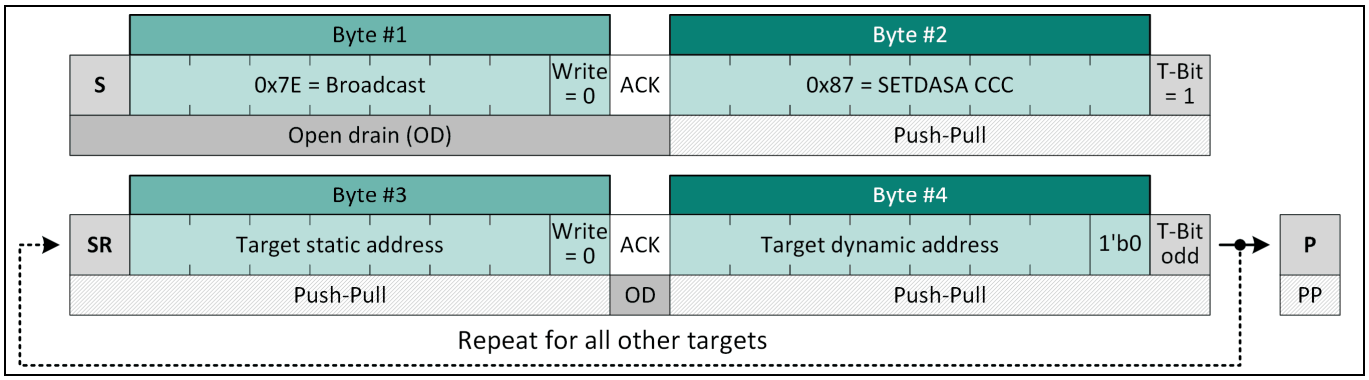


Figure 60 SETDASA Command Structure

Please note that the Static Address is the address set by the ADR0 and ADR1 pins. For this device it can range from 0x40 until 0x47.

Note: *This device version requires sending one SETDASA command (byte #1 to #4 + Stop) for each I3C target individually (see Figure 60).*
This device version does not support setting the dynamic address for more than one I3C device via one SETDASA command (byte #3 and byte #4 target specific), although I3C specification allows this.

6.4.4 I3C Dynamic Address assertion using SETAASA

This command is the fastest way to set the Dynamic Address for all Targets. The static address will become the dynamic address. Master can also identify the dynamic address of each target via the PID (GETPID).

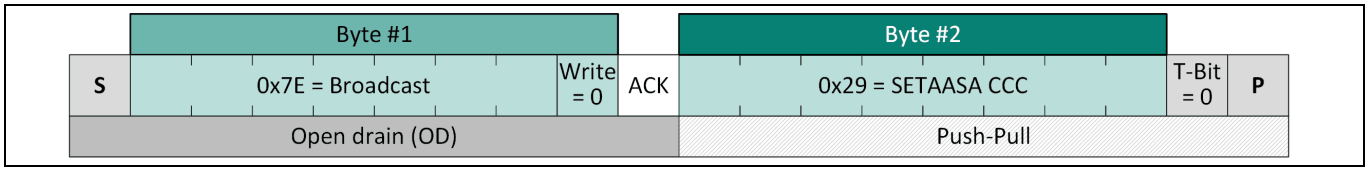


Figure 61 SETAASA Command Structure

6.4.5 I3C SDR read access

A read from a single register address (specified by byte #2) looks like this:

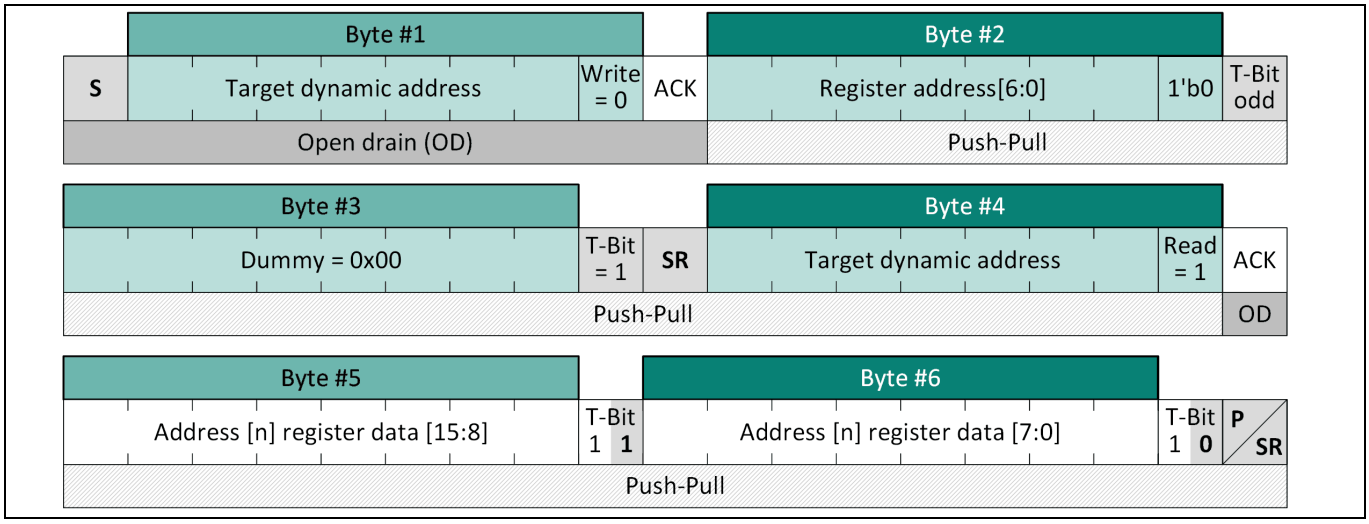


Figure 62 I3C SDR single read

Note: *This device version requires the Master sending a Re-Start (Sr) after byte#3 before the actual read is initiated via byte #4.*
This device version does not support sending a Stop (P)-Start (S) before the actual read is initiated via byte #4, although the I3C specification allows this. The same is also valid for the I3C SDR block read.

Reading multiple consecutive registers can be done using a block read. The only difference to the single read is the T-Bit in byte #6. Note that the address is auto incremented:

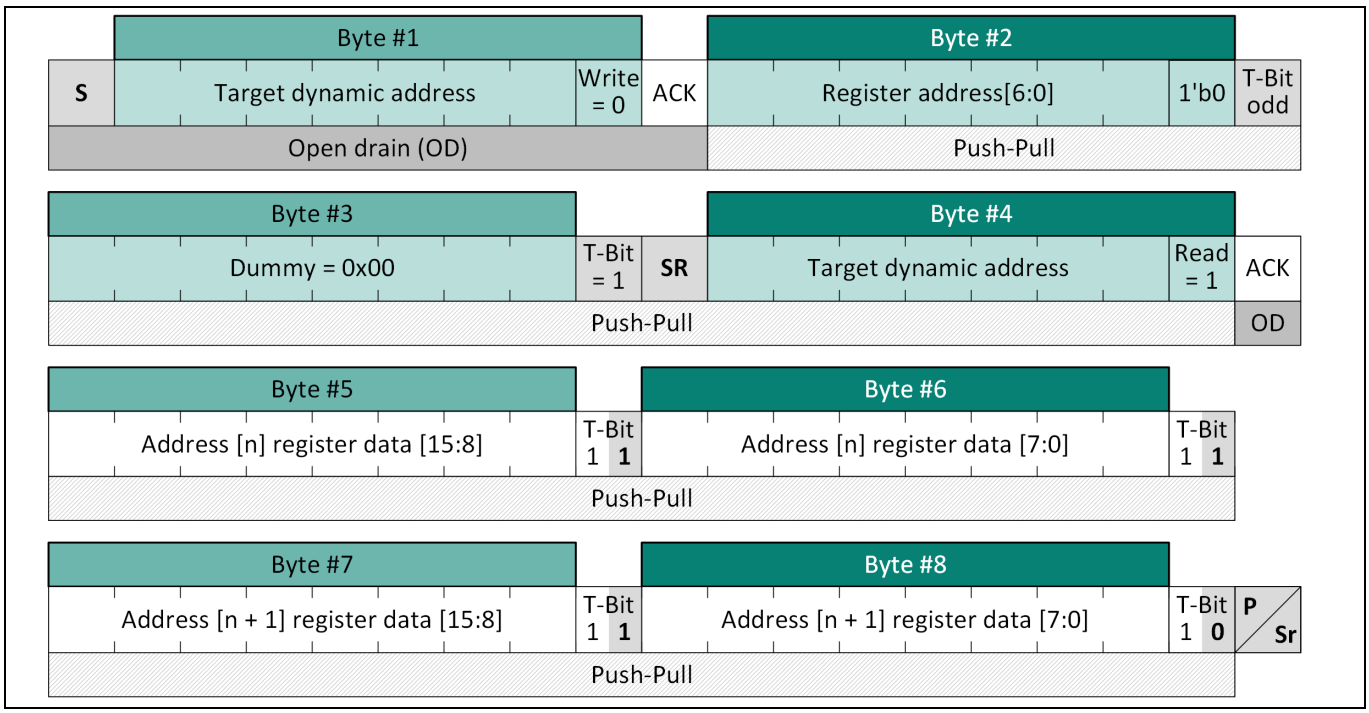


Figure 63 I3C SDR block read

The single register read can be simplified by omitting the register address. This will read the data from the current register address set by the autoincrement from the previous I3C access:

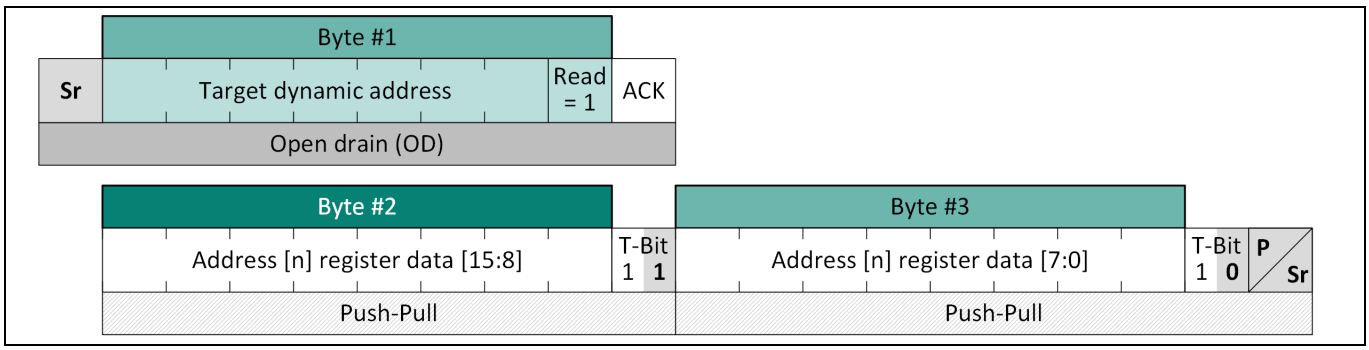


Figure 64 I3C SDR single read from current address

Note: *This device version requires the Master sending a Re-Start before a read is initiated via byte #1. This device version does not support using a Start (S) bit to initiate a read of the register address set via the autoincrement from the previous I3C access, although I3C specification allows this.*

6.4.6 I3C SDR write access

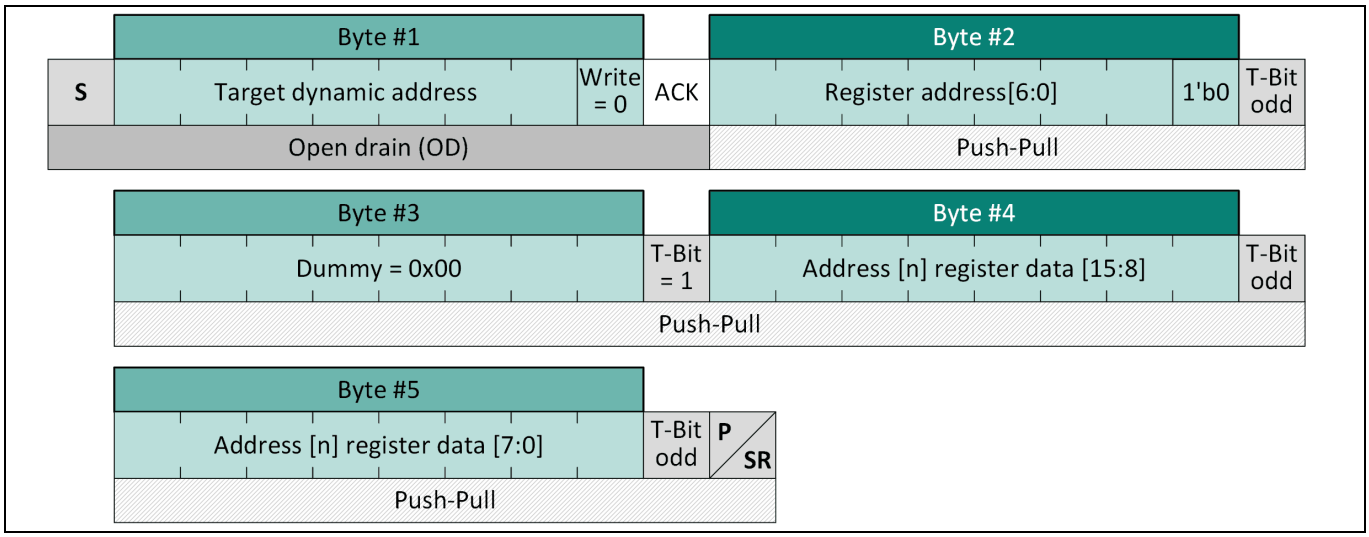


Figure 65 I3C SDR single write

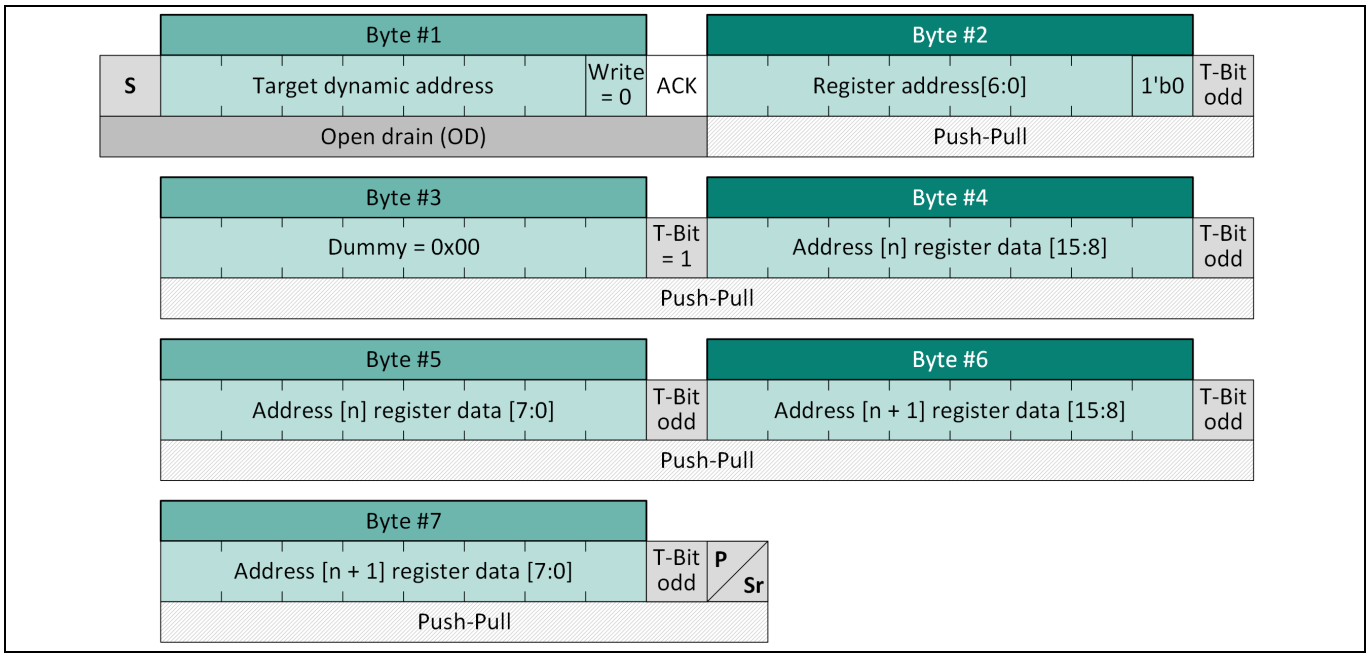


Figure 66 I3C SDR block write

Note: *This device version requires the Master sending a Re-Start (Sr) in case the Master wants to continue an SDR write with an SDR read from an autoincremented address.*
This device version does not support the Master sending a Stop (P) then Start (S) in case the Master wants to continue an SDR write with an SDR read from an autoincremented address.

6.4.7 I3C HDR DDR

Both single and block transfers are supported for HDR-DDR mode in the read and write directions. HDR-DDR transfers are terminated by a CRC word, transmitted by the device which sent the data (in the write direction this is the master, and in the read direction this is the slave). In the write direction, the master simply transmits the CRC word after it has finished transmitting data to the bus. In the read direction, the master must send the requested length of the transfer in advance, as part of its command word (see HDR-DDR read transfers). There are some important considerations for HDR-DDR communications:

- The HDR-DDR command codes 'Reserved for I3C Definition' in the MIPI I3C specification should not be used. This is achieved by starting all HDR-DDR command codes with 11_b.
- In an HDR-DDR read transaction, the command code in the write command word is taken as the number of words expected. The command code in the read command word is ignored.
- HDR-DDR bus turnaround occurs in a write transaction during preamble of first data word returned by slave, and during setup bits of CRC word returned by slave. Please see the MIPI I3C specification for detail on HDR-DDR bus turnaround, as it is not shown in detail here.

The following figures show the timing diagrams of both single and block read and write processes.

6.4.8 I3C HDR DDR read access

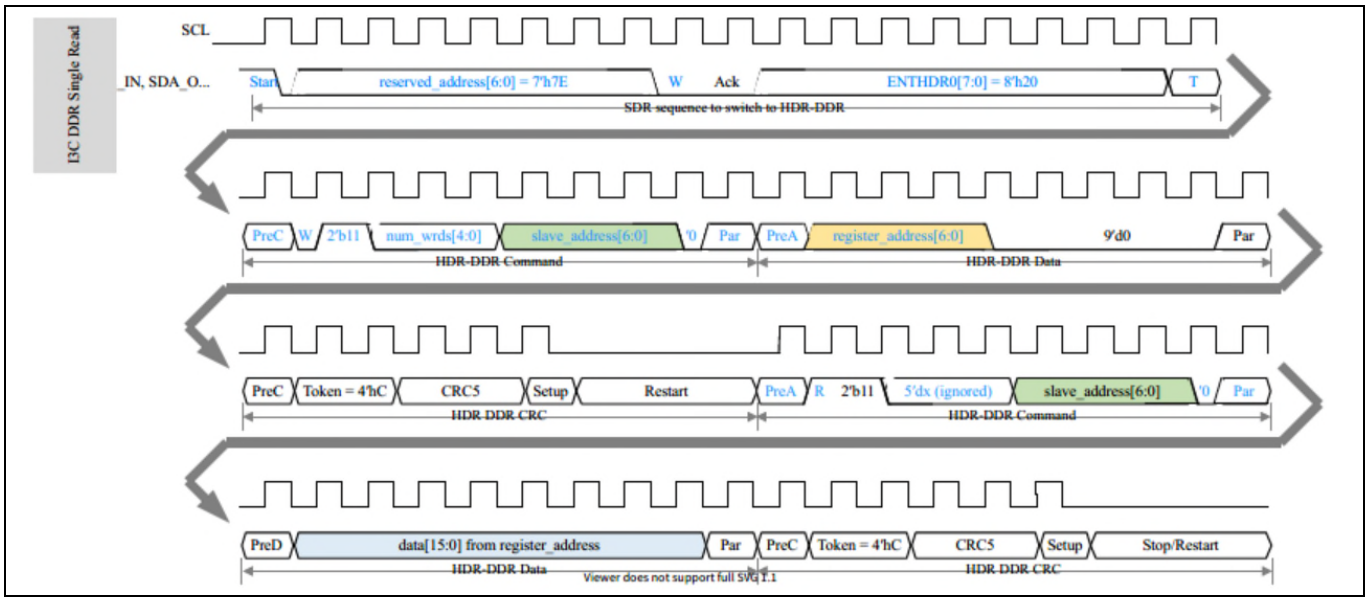


Figure 67 I3C HDR-DDR single read

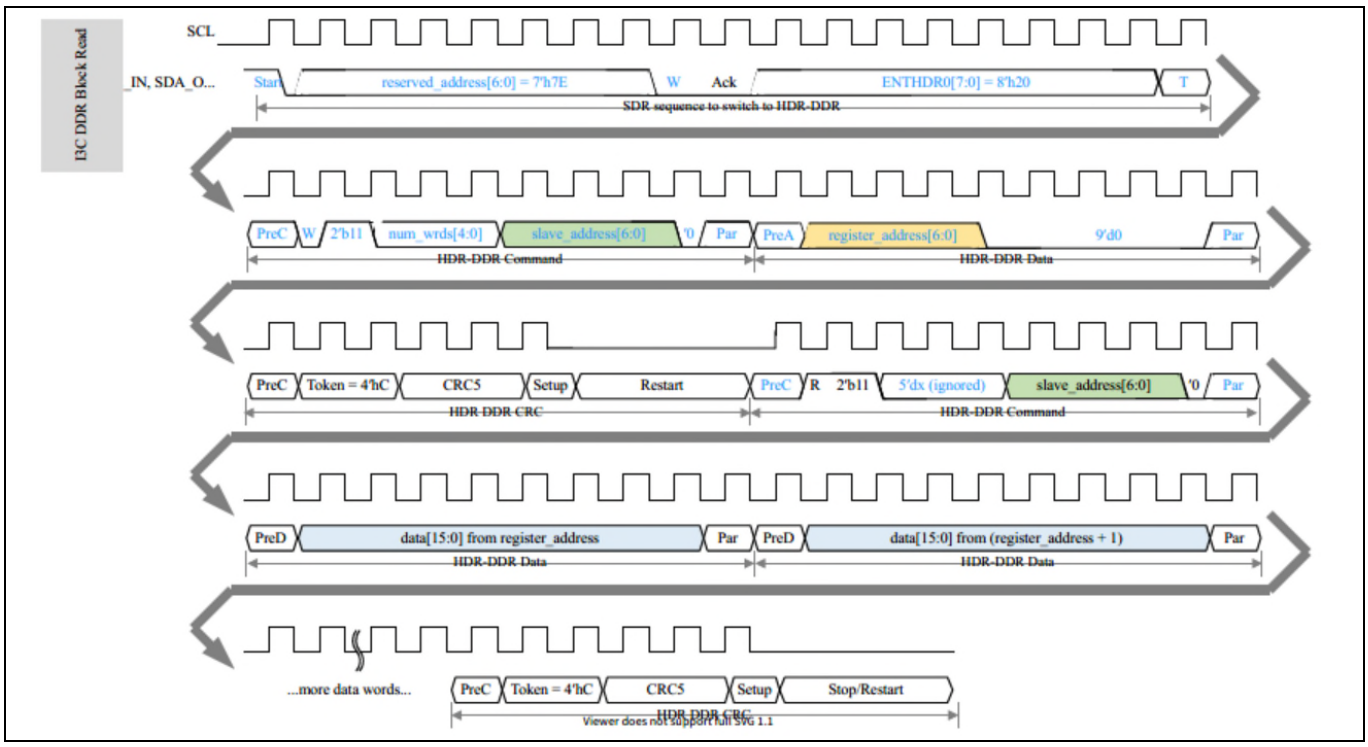


Figure 68 I3C HDR-DDR block read

6.4.9 I3C HDR DDR write access

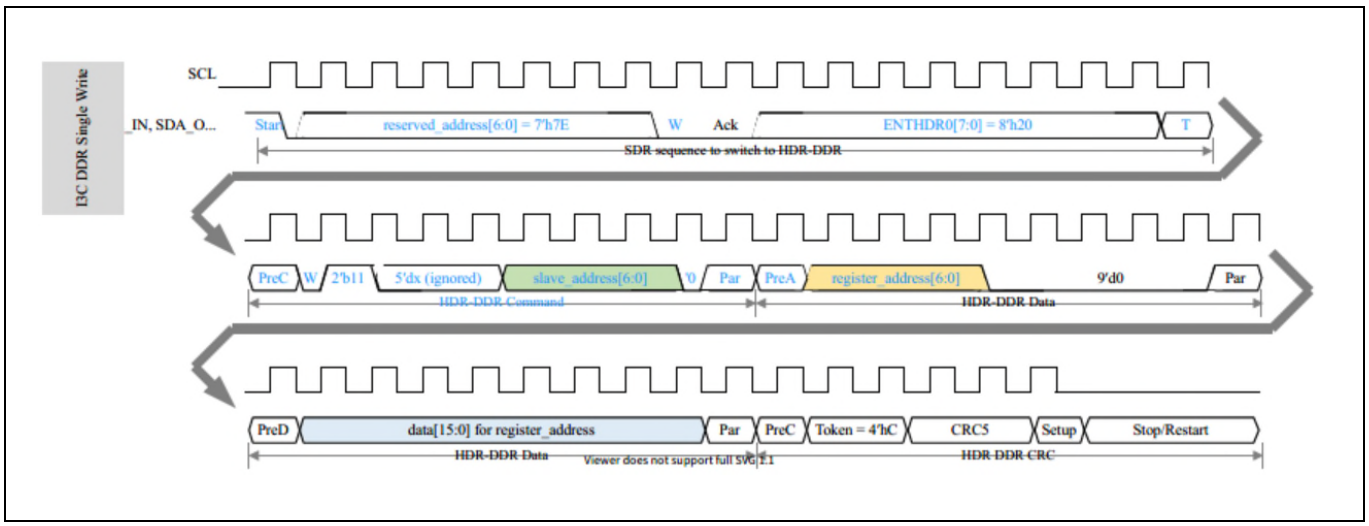


Figure 69 I3C HDR-DDR single write

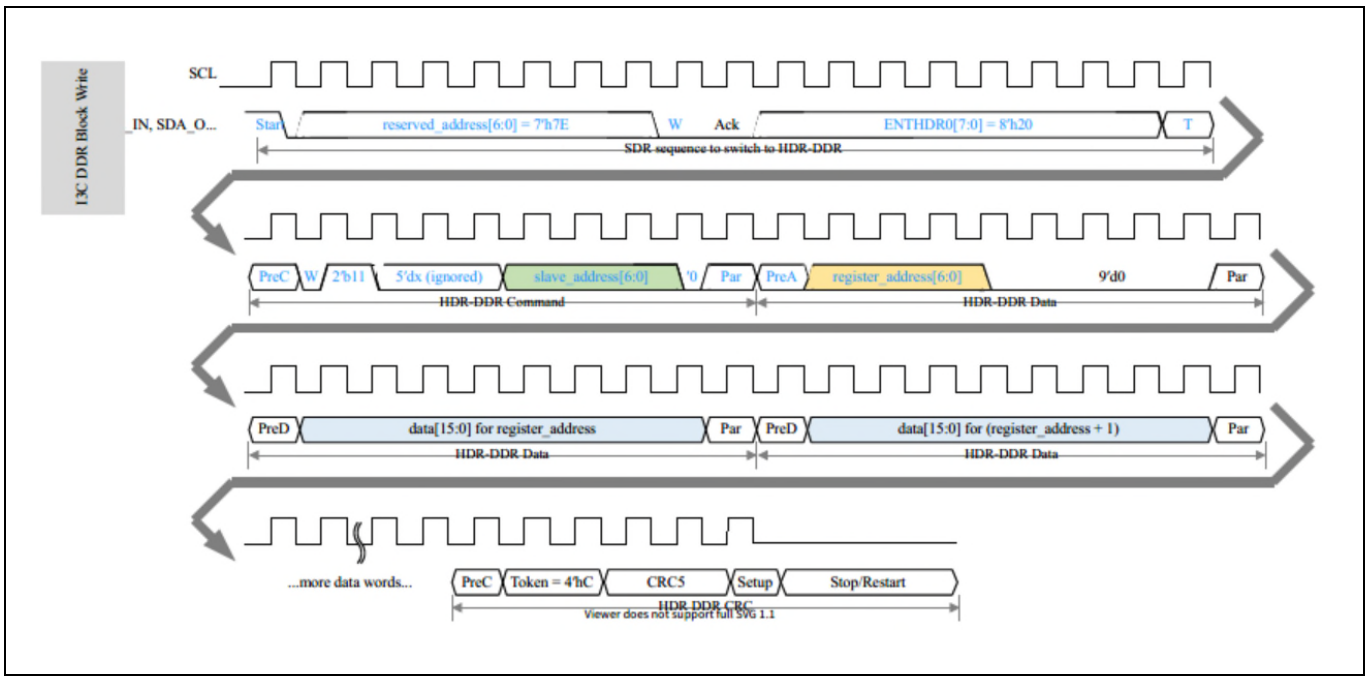


Figure 70 I3C HDR-DDR block write

7 Reference Design

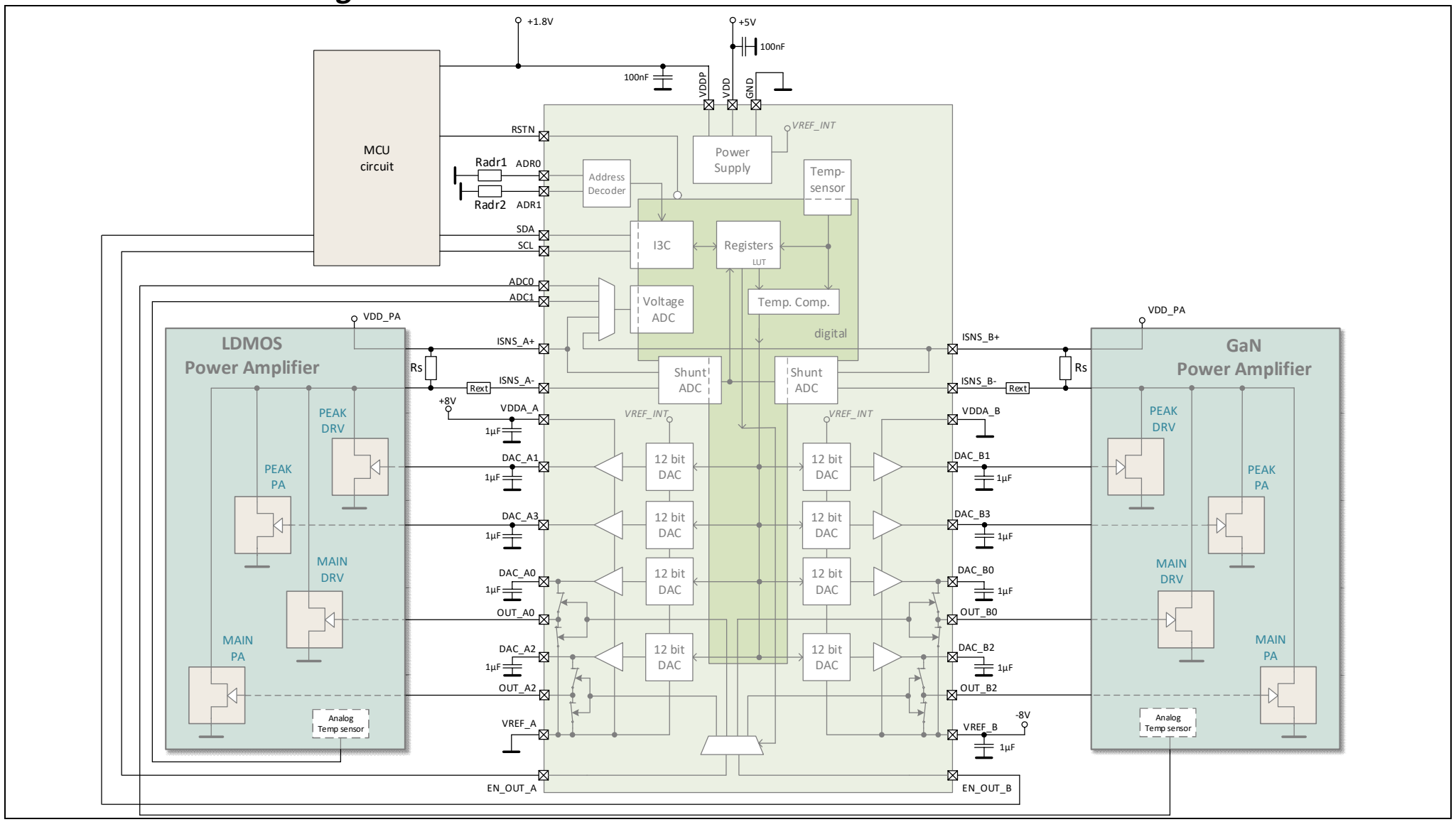


Figure 71 Typical application schematic circuit: biasing LDMOS and GaN Power Amplifiers

7.1 Current Sense ADC

The Current Sense ADC can be used to sense a differential voltage of up to +/-1V. This voltage is generated across a shunt resistor and depends on the current through the shunt. Since the ADC can operate at very low differential voltages (<=15mV) it is possible to use very low-ohmic shunts. For shunts smaller than 100mOhm 4-pin devices are recommended. This allows to compensate errors introduced through the soldering process as the actual shunt voltage is tapped at the top (resistive) side of the shunt. For applications with lower accuracy requirements standard two-pin devices can be used.

When selecting a shunt the thermal stress on the shunt needs to be considered. The thermal power generated in the shunt can be calculated unsing the following equation $P_{SNS\_A} = I^2_{PA} \cdot R_{SNS\_A}$:

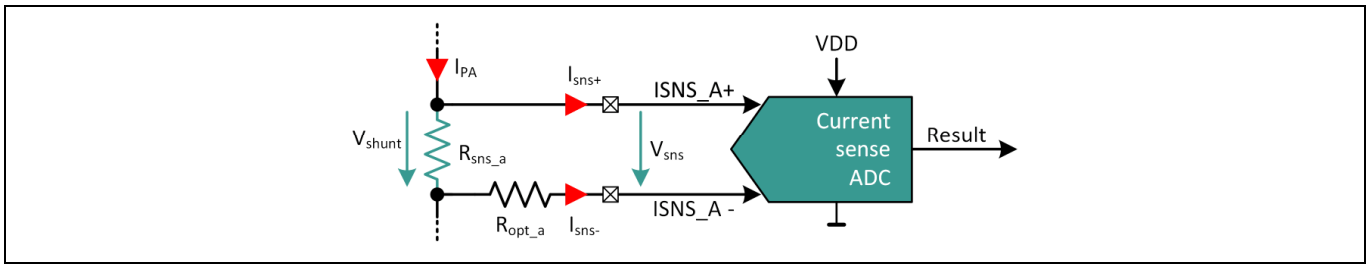


Figure 72 Reference Schematic Current Sense ADC

For e.g. a current of I_{PA} = 1A and R_{SNS_A} = 100mOhm the thermal power is $P_{SNS\_A} = (1A)^2 \cdot 100mOhm = 0.1W$. This can easily be tolerated by a 1206 shunt. In this example the Current Sense ADC can be set to a voltage range of 120mV or 240mV.

For e.g. a current of I_{PA} = 10A and a shunt of R_{SNS_A} = 10mOhm this shunt needs to withstand $P_{SNS\_A} = (10A)^2 \cdot 10mOhm = 1W$ which can still be tolerated by a 1206 shunt. In this example the Current Sense ADC voltage range can be set to 120mV or 240mV.

The maximum voltage across the shunt determines which voltage range to select for the Current Sense ADC. Ranges from 15mV to 240mV are possible. The ADC can tolerate maximum sense voltages up to 1V without any damage although the ADC results will be clipped at the full-scale value. Higher voltages cause an alternative current path through the ESD diodes. This is desired during an ESD event but it is not during normal application as the device may suffer from electrical overstress. To protect the device from overstress a current limiting resistor R_{opt_a} can be added to the ISNS_A-/ISNS_B- pins.

Note: *Sense voltages higher than 1V can degrade the semiconductor structure or cause permanent damage of the device. Current into the ISNS_A- and ISNS_B- pins needs to be limited via a resistor. The resistor may be damaged during such an event depending on the event duration. This can be intentional to protect the device.*

To calculate the optional resistor R_{opt_a} use the maximum input voltage at the ISNS_A- or ISNS_B- pin together with I_{sns-} of maximum 120mA into the ADC. For e.g. a system with a maximum of 60V at ISNS_A- during an error condition and a maximum allowed current of 0.12A the resistor R_{opt_a} must have a value of R_{opt_a} = 60V / 0.12A = 500Ohm. From the E96 series e.g. 499Ohm or 511Ohm can be chosen.

The following figure shows an example layout for the configuration with and without the optional resistor:

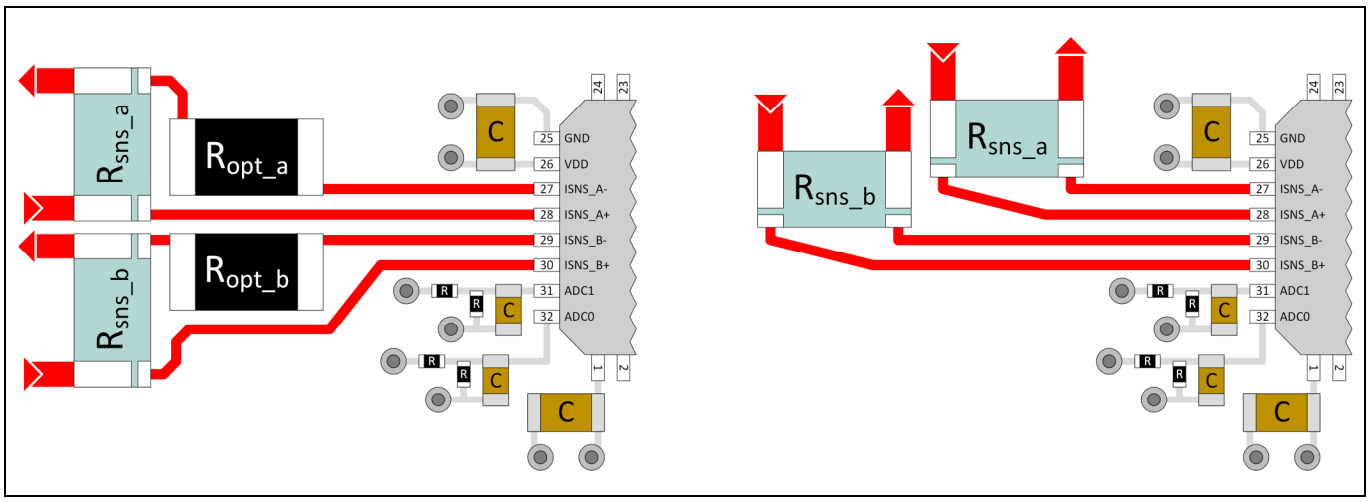


Figure 73 Reference Design Current Sense ADC

7.2 Voltage ADC

The VADC can be connected to an (optional) RC filter and voltage divider circuit. These circuits follow universal layout rules and therefore do not need any special attention:

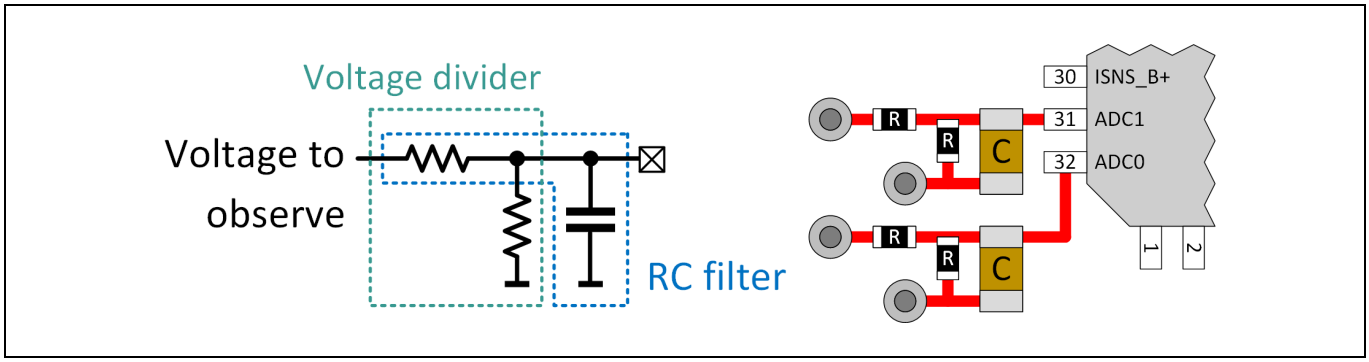


Figure 74 VADC reference circuit and layout

7.3 Digital Pins

This section explains more details about the usage of the digital pins during the following conditions:

- Pin is not used in application (e.g. EN_OUT_A/_B)
- Pins using external pulls (e.g. RSTN)

7.3.1 RSTN Pin

The RSTN pin has a device-internal pull-down circuit. This will assert reset while the device-external world is not driving the pin to high. To ensure a valid high level input signal the driver must be able to drive 800uA or more.

7.3.2 Address Pins ADR0/1

The address pins are used to set the I2C/I3C address. A pin can be left unconnected, tied to GND or tied to VDDP.

When an address pin is left unconnected a weak internal pull-down will ensure a stable pin value. For systems with high energy radiation in the device vicinity it may be necessary to not use unconnected pins but pull the pins to either VDDP or GND to ensure a proper address recognition. To do so it is allowed to have direct connections or use pull resistors. When using resistors their value must be <= 100Ohm.

7.3.3 SCL/SDA Pins

Please refer to section 6.2 I2C Design Considerations for more details.

7.3.4 EN_OUT_A/B Pins

The pins have a device-internal pull-down circuit. To ensure a valid high level the driver must be able to drive 800uA or more.

8 Register Map

8.1 Register summary

The registers of the Bias and Control IC provide information on actual status and measurements, and configure its hardware blocks.
The complete Register map is listed in Table 18.

Table 18 BGMC1210 Register Summary

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	r/w
0x00	VENDOR	VERSION								VENDOR								r
0x01	TEMP	RES								TEMPERATURE								r/(w)
0x02	V_ISNS_A	RES								VALUE								r
0x03	V_ISNS_B	RES								VALUE								r
0x04	ADC0	RES								VALUE								r
0x05	ADC1	RES								VALUE								r
0x06	VDD	RES								VALUE								r
0x07	VDDP	RES								VALUE								r
0x08	VDDA_A	RES								VALUE								r
0x09	VDDA_B	RES								VALUE								r
0x0A	Vref_A	RES								VALUE								r
0x0B	Vref_B	RES								VALUE								r
0x0C	I_ISNS_A	RES					VALUE											r
0x0D	I_ISNS_B	RES					VALUE											r
0x0F	DAC_FB	RES	DAC_ SIDE	DAC_CH			VALUE (read only)											r/w
0x10	ADC_EN	RES			DTS_EN	RES			VADC _EN	ISNS_B_RNG			ISNS _B_EN	ISNS_A_RNG			ISNS _A_EN	r/w
0x11	DACCNF1	TCOMP _EN	SLP			TRK_B3 toB2	TRK_B1 toB0	TRK_A3 toA2	TRK_A1 toA0	OUT_CTRL_B2		OUT_CTRL_B0		OUT_CTRL_A2		OUT_CTRL_A0		r/w
0x12	DACCNF2	LD_B3		LD_B2		LD_B1		LD_B0		LD_A3		LD_A2		LD_A1		LD_A0		r/w
0x13	VCLMP_A	DVAL_A2						SEL_A2		DVAL_A0						SEL_A0		r/w
0x14	VCLMP_B	DVAL_B2						SEL_B2		DVAL_B0						SEL_B0		r/w
0x15	DAC_A0	EN	RNG	OFFS		VALUE												r/w
0x16	DAC_A1	EN	RNG	OFFS		VALUE												r/w

Register Map

Addr	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	r/w
0x17	DAC_A2	EN	RNG	OFFS		VALUE												r/w
0x18	DAC_A3	EN	RNG	OFFS		VALUE												r/w
0x19	DAC_B0	EN	RNG	OFFS		VALUE												r/w
0x1A	DAC_B1	EN	RNG	OFFS		VALUE												r/w
0x1B	DAC_B2	EN	RNG	OFFS		VALUE												r/w
0x1C	DAC_B3	EN	RNG	OFFS		VALUE												r/w
0x1D	TCLUT_A0_L	grad3				grad2				grad1				grad0				r/w
0x1E	TCLUT_A0_H	grad7				grad6				grad5				grad4				r/w
0x1F	TCLUT_A1_L	grad3				grad2				grad1				grad0				r/w
0x20	TCLUT_A1_H	grad7				grad6				grad5				grad4				r/w
0x21	TCLUT_A2_L	grad3				grad2				grad1				grad0				r/w
0x22	TCLUT_A2_H	grad7				grad6				grad5				grad4				r/w
0x23	TCLUT_A3_L	grad3				grad2				grad1				grad0				r/w
0x24	TCLUT_A3_H	grad7				grad6				grad5				grad4				r/w
0x25	TCLUT_B0_L	grad3				grad2				grad1				grad0				r/w
0x26	TCLUT_B0_H	grad7				grad6				grad5				grad4				r/w
0x27	TCLUT_B1_L	grad3				grad2				grad1				grad0				r/w
0x28	TCLUT_B1_H	grad7				grad6				grad5				grad4				r/w
0x29	TCLUT_B2_L	grad3				grad2				grad1				grad0				r/w
0x2A	TCLUT_B2_H	grad7				grad6				grad5				grad4				r/w
0x2B	TCLUT_B3_L	grad3				grad2				grad1				grad0				r/w
0x2C	TCLUT_B3_H	grad7				grad6				grad5				grad4				r/w
0x2D	CCOMP_A0	EN	RES	AMP						SLP								r/w
0x2E	CCOMP_A2	EN	RES	AMP						SLP								r/w
0x2F	CCOMP_B0	EN	RES	AMP						SLP								r/w
0x30	CCOMP_B2	EN	RES	AMP						SLP								r/w

8.2 Register details

The registers of BGMC1210 are described below in detail.

8.2.1 VENDOR register

Address: **00_h**

Name: **VENDOR**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VERSION								VENDOR							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Table 19 VENDOR register details

Bit	Field	Type	Default	Description
15-8	VERSION	r	00_h	Version code
7-0	VENDOR	r	02_h	Vendor code

8.2.2 TEMP register

Address: **01_h**

Name: **TEMP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES							TEMPERATURE								
Default:	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

Table 20 TEMP register details

Bit	Field	Type	Default	Description
15-9	RES	r	00_h	Reserved bits
8-0	TEMPERATURE	r/(w)	$08C_h$	DTS enabled: actual measured die temperature (read only) DTS disabled: temperature for temperature compensation needs to be written here (read/write access)

8.2.3 V_ISNS_A register

Address: **02_h**

Name: **V_ISNS_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21 V_ISNS_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits

Bit	Field	Type	Default	Description
10-0	VALUE	r	000_h	11 bit result of VADC measured at ISNS_A+

8.2.4 V_ISNS_B register

Address: **03_h**

Name: **V_ISNS_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22 V_ISNS_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ISNS_B+

8.2.5 ADC0 register

Address: **04_h**

Name: **ADC0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23 ADC0 register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ADC0

8.2.6 ADC1 register

Address: **05_h**

Name: **ADC1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24 ADC1 register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at ADC1

8.2.7 VDD register

Address: **06h**

Name: **VDD**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25 VDD register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDD

8.2.8 VDDP register

Address: **07h**

Name: **VDDP**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26 VDDP register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDDP

8.2.9 VDDA_A register

Address: **08h**

Name: **VDDA_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27 VDDA_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00_h	Reserved bits
10-0	VALUE	r	000_h	11 bit result of VADC measured at VDDA_A

8.2.10 VDDA_B register

Address: **09h**

Name: **VDDA_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28 VDDA_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at VDDA_B

8.2.11 Vref_A register

Address: **0Ah**

Name: **Vref_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29 Vref_A register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at Vref_A

8.2.12 Vref_B register

Address: **0Bh**

Name: **Vref_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES					VALUE										
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30 Vref_B register details

Bit	Field	Type	Default	Description
15-11	RES	r	00h	Reserved bits
10-0	VALUE	r	000h	11 bit result of VADC measured at Vref_B

8.2.13 I_ISNS_A register

Address: **0C$_h$**

Name: **I_SNS_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES				VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 31 I_ISNS_A register details

Bit	Field	Type	Default	Description
15-12	RES	r	0_h	Reserved bits
11-0	VALUE	r	000_h	12 bit result of Current Shunt ADC measured across (ISNS_A+ - ISNS_A-)

8.2.14 I_ISNS_B register

Address: **0D$_h$**

Name: **I_SNS_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES				VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 32 I_ISNS_B register details

Bit	Field	Type	Default	Description
15-12	RES	r	0_h	Reserved bits
11-0	VALUE	r	000_h	12 bit result of Current Shunt ADC measured across (ISNS_B+ - ISNS_B-)

8.2.15 DAC feedback register

Address: **0F$_h$**

Name: **DAC_FB**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES	DAC_SIDE	DAC_CH		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 33 DAC_FB register details

Bit	Field	Type	Default	Description
15	RES	r	0_b	Reserved bit
14	DAC_SIDE	r/w	0_b	0_b: side A 1_b: side B
13-12	DAC_CH	r/w	00_b	Channel of DAC: 00_b: 0 01_b: 1

Bit	Field	Type	Default	Description
				10_b: 2 11_b: 3
11-0	VALUE	r	000_h	Digital representation of calculated 12 bit value of selected DAC. Note: this field is read only – any data attempted to be written ill be ignored

8.2.16 ADC enable register

Address: **10_h**

Name: **ADC_EN**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RES			DTS_EN	RES			VADC_EN	ISNS_B_RNG			ISNS_B_EN	ISNS_A_RNG			ISNS_A_EN
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 34 ADC_EN register details

Bit	Field	Type	Default	Description
15-13	RES	r	000_b	Reserved bits
12	DTS_EN	r/w	0_b	Enable Die Temperature Sensor (DTS)
11-9	RES	r	0_b	Reserved bit
8	VADC_EN	r/w	0_b	Enable Voltage ADC
7-5	ISNS_B_RNG	r/w	000_b	Full Scale Range of ISNS_B ADC: 000_b: 15 mV 001_b: 30 mV 010_b: 60 mV 011_b: 120 mV 100_b - 111_b: 240mV
4	ISNS_B_EN	r/w	0_b	Enable Shunt ADC B
3-1	ISNS_A_RNG	r/w	000_b	Full Scale Range of ISNS_A ADC: 000_b: 15 mV 001_b: 30 mV 010_b: 60 mV 011_b: 120 mV 100_b - 111_b: 240 mV
0	ISNS_A_EN	r/w	0_b	Enable Shunt ADC A

8.2.17 DACCNF1 register

Address: **11_h**

Name: **DACCNF1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCOMP_EN	SLP			TRK_B3toB2	TRK_B1toB0	TRK_A3toA2	TRK_A1toA0	OUT_CTRL_B2		OUT_CTRL_B0		OUT_CTRL_A2		OUT_CTRL_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 35 DACCNF1 register details

Bit	Field	Type	Default	Description
15	TCOMP_EN	r/w	0_b	Enable Temperature Compensation
14-12	SLP	r/w	000_b	Slope settings for update rate of DAC value: 000_b: immediate update (1 count per 50 ns) 001_b: 1 µs (1 count per 1 µs) 010_b: 5 µs (1 count per 5 µs) 011_b: 10 µs (1 count per 10 µs) 100_b: 100 µs (1 count per 100 µs) 101_b: 250 µs (1 count per 250 µs) 110_b: 1 ms (1 count per 1 ms) 111_b: 4 ms (1 count per 4 ms)
11	TRK_B3toB2	r/w	0_b	Enables tracking of odd DAC (DAC_B3(1), DAC_A3(1)) to the even DAC (DAC_B2(0), DAC_A2(0))
10	TRK_B1toB0	r/w	0_b	
9	TRK_A3toA2	r/w	0_b	
8	TRK_A1toA0	r/w	0_b	
7-6	OUT_CTRL_B2	r/w	0_b	OUT_CTRL_xy: 00_b: use EN_OUT_xy for controlling OUT_xy 01_b: force clamping of OUT_xy (connect to VCLMP potential) 10_b: force enable of OUT_xy (connect to DAC_xy) 11_b: use EN_OUT_!xy from other side for controlling OUT_xy (!A = B, !B = A)
5-4	OUT_CTRL_B0	r/w	0_b	
3-2	OUT_CTRL_A2	r/w	0_b	
1-0	OUT_CTRL_A0	r/w	0_b	

8.2.18 DACCNF2 register

Address: **12_h**

Name: **DACCNF2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LD_B3		LD_B2		LD_B1		LD_B0		LD_A3		LD_A2		LD_A1		LD_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 36 DACCNF register details

Bit	Field	Type	Default	Description
15-14	LD_B3	r/w	00_b	LD_xy: 00_b: normal mode
13-12	LD_B2	r/w	00_b	

Bit	Field	Type	Default	Description
11-10	LD_B1	r/w	00_b	01_b: enables high current mode 10_b, 11_b: enables stability for low cap values in normal mode
9-8	LD_B0	r/w	00_b	
7-6	LD_A3	r/w	00_b	
5-4	LD_A2	r/w	00_b	
3-2	LD_A1	r/w	00_b	
1-0	LD_A0	r/w	00_b	

8.2.19 VCLMP_A register

Address: **13_h**

Name: **VCLMP_A**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVAL_A2						SEL_A2		DVAL_A0						SEL_A0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 1 VCLMP_A register details

Bit	Field	Type	Default	Description
15-10	DVAL_A2	r/w	00_h	Value of delta voltage referred to DAC_A2
9-8	SEL_A2	r/w	00_b	Select clamping potential: 00_b: VREF_A 01_b: DAC_A3 (also enables DAC_A3) 10_b, 11_b: VCLMP buffer
7-2	DVAL_A0	r/w	00_h	Value of delta voltage referred to DAC_A0
1-0	SEL_A0	r/w	00_b	Select clamping potential: 00_b: VREF_A 01_b: DAC_A1 (also enables DAC_A1) 10_b, 11_b: VCLMP buffer

8.2.20 VCLMP_B register

Address: **14_h**

Name: **VCLMP_B**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVAL_B2						SEL_B2		DVAL_B0						SEL_B0	
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 2 VCLMP_A register details

Bit	Field	Type	Default	Description
15-10	DVAL_B2	r/w	00_h	Value of delta voltage referred to DAC_B2
9-8	SEL_B2	r/w	00_b	Select clamping potential: 00_b: VREF_B 01_b: DAC_B3 (also enables DAC_B3)

Bit	Field	Type	Default	Description
				10_b, 11_b: VCLMP buffer
7-2	DVAL_B0	r/w	00_h	Value of delta voltage referred to DAC_B0
1-0	SEL_B0	r/w	00_b	Select clamping potential: 00_b: VREF_B 01_b: DAC_B1 (also enables DAC_B1) 10_b, 11_b: VCLMP buffer

8.2.21 DAC_A0 register

Address: **15_h**

Name: **DAC_A0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3 DAC_A0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A0
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A0 output value

8.2.22 DAC_A1 register

Address: **16_h**

Name: **DAC_A1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4 DAC_A1 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A1
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A1 output value

8.2.23 DAC_A2 register

Address: **17_h**

Name: **DAC_A2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5 DAC_A2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A2
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A2 output value

8.2.24 DAC_A3 register

Address: **18_h**

Name: **DAC_A3**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 6 DAC_A3 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_A3
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 3.0V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_A3 output value

8.2.25 DAC_B0 register

Address: **19_h**

Name: **DAC_B0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 7 DAC_B0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B0
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B0 output value

8.2.26 DAC_B1 register

Address: **$1A_h$**

Name: **DAC_B1**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8 DAC_B1 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B1
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B1 output value

8.2.27 DAC_B2 register

Address: **$1B_h$**

Name: **DAC_B2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 9 DAC_B2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B2
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B2 output value

8.2.28 DAC_B3 register

Address: **$1C_h$**

Name: **DAC_B3**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RNG	OFFS		VALUE											
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10 DAC_B3 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable DAC_B3
14	RNG	r/w	0_b	Range: 0_b: 0 – 3.5V 1_b: 0 – 7V

Bit	Field	Type	Default	Description
13-12	OFFS	r/w	00_b	Add offset to DAC output: 00_b: 0V (for both RNG settings) 01_b: 0.5V in 3.5V range / 1V in 7V range 10_b: 1.5V in 3.5V range / 1V in 7V range 11_b: 2.5V in 3.5V range / 1V in 7V range
11-0	VALUE	r/w	000_h	DAC_B3 output value

8.2.29 TCLUT_A0_L register

Address: **$1D_h$**

Name: **TCLUT_A0_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 11 TCLUT_A0_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT1: 4 Low half-bytes for temperature compensation of DAC_A0 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

8.2.30 TCLUT_A0_H register

Address: **$1E_h$**

Name: **TCLUT_A0_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 12 TCLUT_A0_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT1: 4 High half-bytes for temperature compensation of DAC_A0 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.31 TCLUT_A1_L register

Address: **1F$_h$**

Name: **TCLUT_A1_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 13 TCLUT_A1_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0$_h$	LUT2: 4 Low half-bytes for temperature compensation of DAC_A1 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0$_h$	
7-4	grad1	r/w	0$_h$	
3-0	grad0	r/w	0$_h$	

8.2.32 TCLUT_A1_H register

Address: **20$_h$**

Name: **TCLUT_A1_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 14 TCLUT_A1_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0$_h$	LUT2: 4 High half-bytes for temperature compensation of DAC_A1 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0$_h$	
7-4	grad5	r/w	0$_h$	
3-0	grad4	r/w	0$_h$	

8.2.33 TCLUT_A2_L register

Address: **21$_h$**

Name: **TCLUT_A2_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 15 TCLUT_A2_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0$_h$	
11-8	grad2	r/w	0$_h$	

Bit	Field	Type	Default	Description
7-4	grad1	r/w	0_h	LUT3: 4 Low half-bytes for temperature compensation of DAC_A2 (signed values for each gradient -8 to 7)
3-0	grad0	r/w	0_h	

8.2.34 TCLUT_A2_H register

Address: **22_h**

Name: **TCLUT_A2_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 16 TCLUT_A2_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT3: 4 High half-bytes for temperature compensation of DAC_A2 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.35 TCLUT_A3_L register

Address: **23_h**

Name: **TCLUT_A3_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 17 TCLUT_A3_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT4: 4 Low half-bytes for temperature compensation of DAC_A3 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

8.2.36 TCLUT_A3_H register

Address: **24_h**

Name: **TCLUT_A3_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 18 TCLUT_A3_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT4: 4 High half-bytes for temperature compensation of DAC_A3 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.37 TCLUT_B0_L register

Address: **25_h**

Name: **TCLUT_B0_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 19 TCLUT_B0_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT5: 4 Low half-bytes for temperature compensation of DAC_B0 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

8.2.38 TCLUT_B0_H register

Address: **26_h**

Name: **TCLUT_B0_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 20 TCLUT_B0_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT5: 4 High half-bytes for temperature compensation of DAC_B0 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.39 TCLUT_B1_L register

Address: **27h**

Name: **TCLUT_B1_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 21 TCLUT_B1_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0h	LUT6: 4 Low half-bytes for temperature compensation of DAC_B1 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0h	
7-4	grad1	r/w	0h	
3-0	grad0	r/w	0h	

8.2.40 TCLUT_B1_H register

Address: **28h**

Name: **TCLUT_B1_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 22 TCLUT_B1_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0h	LUT6: 4 High half-bytes for temperature compensation of DAC_B1 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0h	
7-4	grad5	r/w	0h	
3-0	grad4	r/w	0h	

8.2.41 TCLUT_B2_L register

Address: **29h**

Name: **TCLUT_B2_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 23 TCLUT_B2_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0h	
11-8	grad2	r/w	0h	

Bit	Field	Type	Default	Description
7-4	grad1	r/w	0_h	LUT7: 4 Low half-bytes for temperature compensation of DAC_B2 (signed values for each gradient -8 to 7)
3-0	grad0	r/w	0_h	

8.2.42 TCLUT_B2_H register

Address: **$2A_h$**

Name: **TCLUT_B2_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 24 TCLUT_B2_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT7: 4 High half-bytes for temperature compensation of DAC_B2 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.43 TCLUT_B3_L register

Address: **$2B_h$**

Name: **TCLUT_B3_L**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad3				grad2				grad1				grad0			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 25 TCLUT_B3_L register details

Bit	Field	Type	Default	Description
15-12	grad3	r/w	0_h	LUT8: 4 Low half-bytes for temperature compensation of DAC_B3 (signed values for each gradient -8 to 7)
11-8	grad2	r/w	0_h	
7-4	grad1	r/w	0_h	
3-0	grad0	r/w	0_h	

8.2.44 TCLUT_B3_H register

Address: **$2C_h$**

Name: **TCLUT_B3_H**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	grad7				grad6				grad5				grad4			
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 26 TCLUT_B3_H register details

Bit	Field	Type	Default	Description
15-12	grad7	r/w	0_h	LUT8: 4 High half-bytes for temperature compensation of DAC_B3 (signed values for each gradient -8 to 7)
11-8	grad6	r/w	0_h	
7-4	grad5	r/w	0_h	
3-0	grad4	r/w	0_h	

8.2.45 CCOMP_A0 register

Address: **$2D_h$**

Name: **CCOMP_A0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 27 CCOMP_A0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

8.2.46 CCOMP_A2 register

Address: **$2E_h$**

Name: **CCOMP_A2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 28 CCOMP_A2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

8.2.47 CCOMP_B0 register

Address: **2F$_h$**

Name: **CCOMP_B0**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 29 CCOMP_B0 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

8.2.48 CCOMP_B2 register

Address: **30$_h$**

Name: **CCOMP_B2**

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN	RES	AMP						SLP							
Default:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 30 CCOMP_B2 register details

Bit	Field	Type	Default	Description
15	EN	r/w	0_b	Enable clamping compensation
14	RES	r	0_b	Reserved bit
13-8	AMP	r/w	00_h	Amplitude setting: preliminary offset (in LSB) during OUT_EN_x=0
7-0	SLP	r/w	00_h	Returning slope update rate (multiples of 1 µs per decrement)

9 Package Information

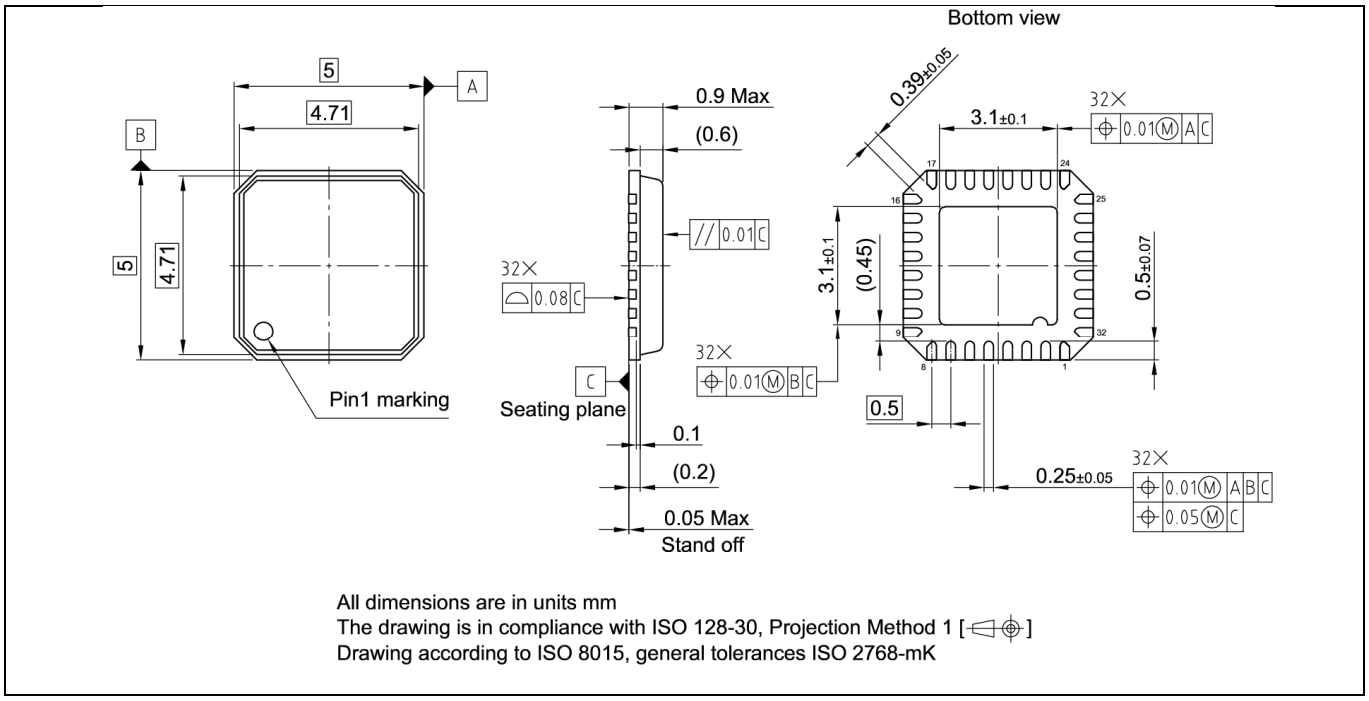


Figure 75 PG-VQFN-32-24 package outline

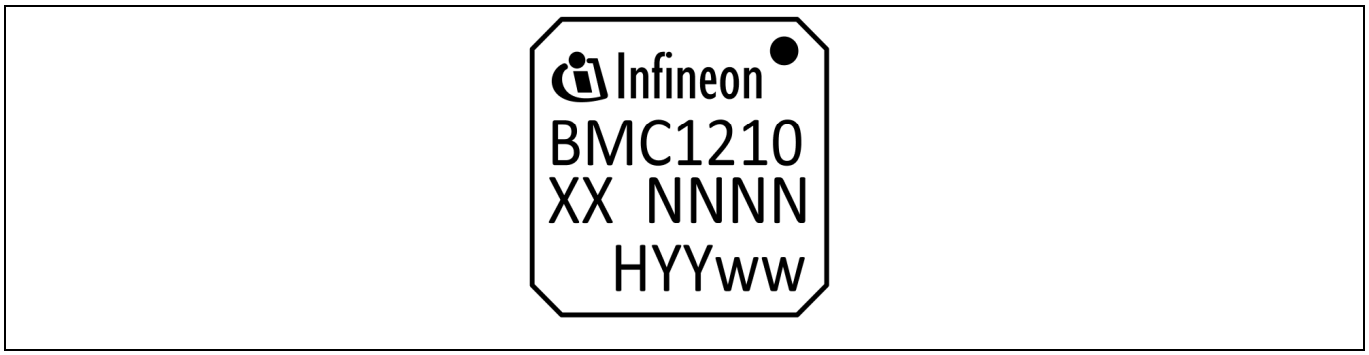


Figure 76 Marking specification

Marking details:

- Infineon logo + pin 1 marking
- BMC1210: Part name abbreviated (actually BGMC1210)
- XX: Lot specific
- NNNN: Serial number
- H: Halogen free
- YY: Production year (e.g. 23 = 2023)
- ww: Production week (e.g. 41 = week 41)

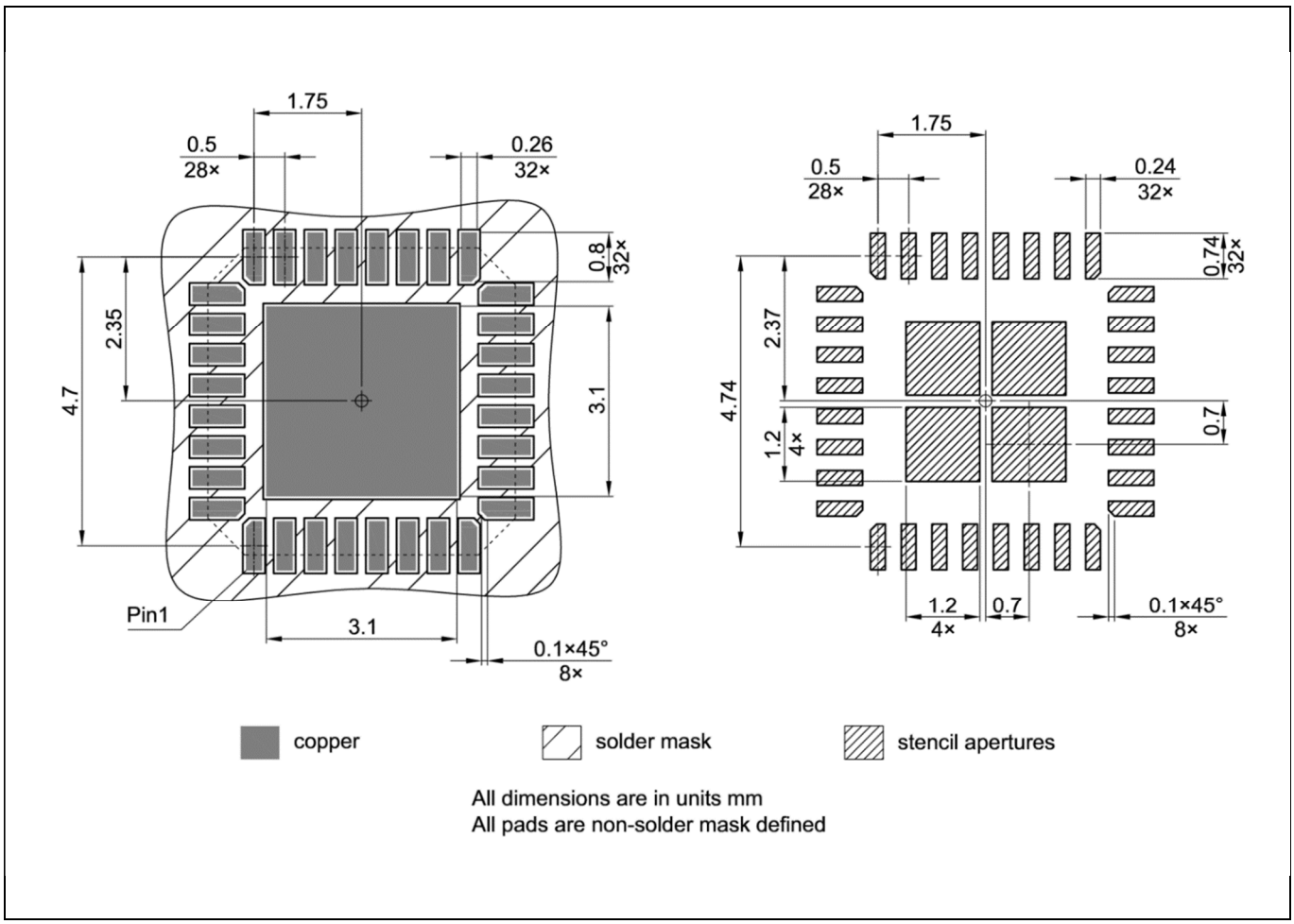


Figure 77 PG-VQFN-32-24 PCB footprint

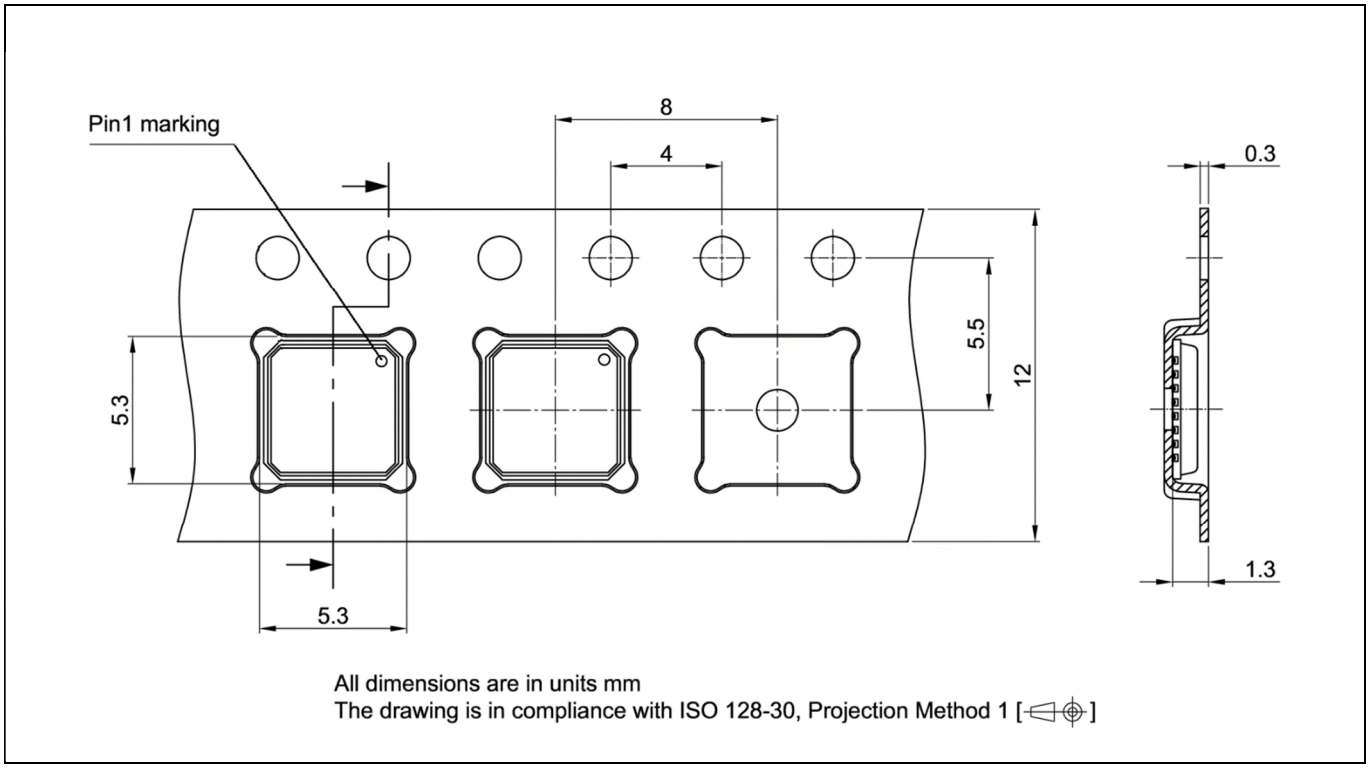


Figure 78 PG-VQFN-32-24 Tape information

Revision history

Document version	Date of release	Description of changes
V2.2	2025-05-05	• ISNS min/max value in table #3 • Note for $FSR_{VADC,ISNS}$ in table #10 • Table #14: swapped V_{IH} (max) with V_{IH} (min) • Table #14: swapped V_{IL} (min) with V_{IL} (max) • Section 4.3.3: Note regarding reset events <50ns • Figure 72: Replaced V_{sns} with V_{shunt} • Page 62: ISNS safety precautions • Page 63: RSTn pin section • Figure 77: PCB footprint drawing • Several minor spelling/cosmetic updates
V2.1	2024-02-19	Package footprint and type number PG-VQFN-32-24 (was -21) Chip marking, added Voh + Vol data
V2.0	2024-02-01	Reworked section ‘Reference design’ Several minor updates (spelling etc.)
V1.6	2023-08-01	Reworked sections: Functional Description; Application and implementation; I2C/I3C Serial Digital Interface
V1.5	2023-02-13	DTS accuracy updated; Digital interface section updated; Added sections: Functional behavior, DAC Output Voltage configuration, Typical application information
V1.4	2022-08-22	Corrections, Table 3.5.8 Digital logic added
V1.3	2022-03-21	Features, electrical characteristics, multiple sections update, register map update
V 1.2	2021-10-22	Features, electrical characteristics, tape information update
V 1.1	2021-09-03	Package drawing update
V 1.0	2021-07-16	Initial version

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2025-05-05

Published by

Infineon Technologies AG

81726 München, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

ifx1

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics (“Beschaffenheitsgarantie”) .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer’s compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer’s products and any use of the product of Infineon Technologies in customer’s applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer’s technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies’ products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.