

Features

- Wide operating voltage: 2.7V~5.5V
- Internal Programmable Gain Amplifier
- Integrated serial interface module, including I²C and SPI interfaces, for external communication
- A/D Converter output data rate: 10Hz~1.28kHz
- Internal temperature sensor for compensation
- Package type: 20-pin SSOP

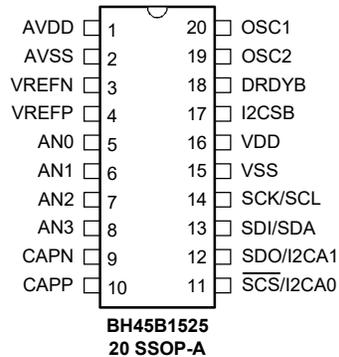
Applications

- Instrumentation
- Health Monitoring Equipment
- Precision Sensing

General Description

The BH45B1525 is a multi-channel 24-bit Delta Sigma A/D converter which includes programmable gain amplifier (PGA) functions and is designed for applications that interface differentially to analog signals. The device has the benefits of low noise and high accuracy and communicates with external hardware using internal I²C or SPI bus. This highly functionally integrated Delta Sigma analog to digital converter with its high accuracy and low power specifications offers a superior solution for interfacing to external sensors especially for battery powered applications.

Pin Assignment



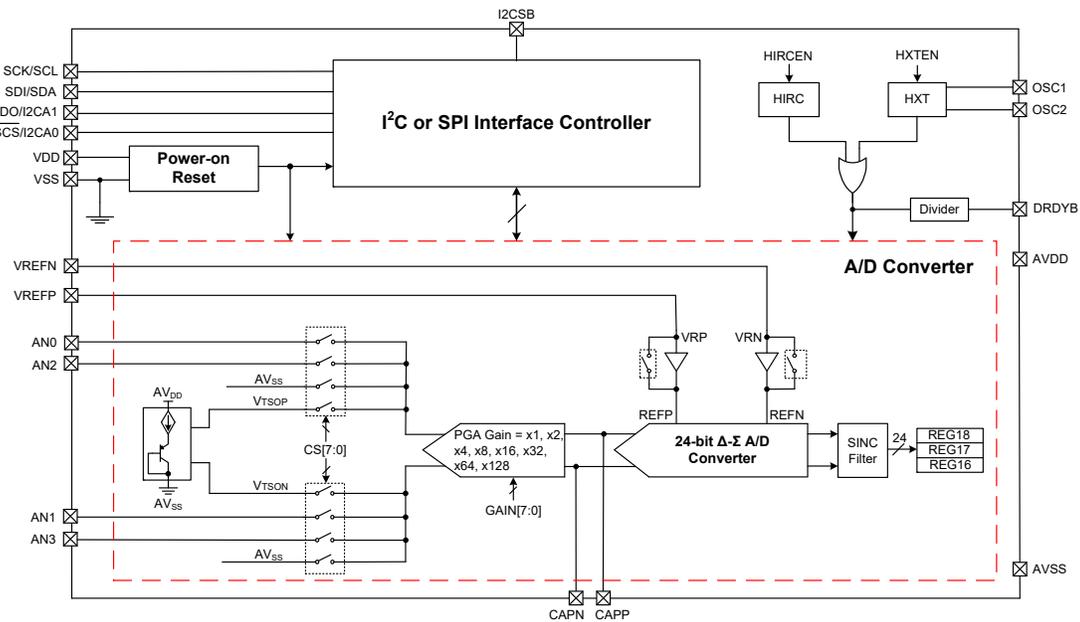
Pin Description

Pin Name	Function	Type	Description
OSC1	OSC1	HXT	HXT oscillator input
OSC2	OSC2	HXT	HXT oscillator output
DRDYB	DRDYB	O	Data ready: indicates valid data by going low HIRC or HXT clock output
I2CSB	I2CSB	I	Low: I ² C, High: SPI
SDI/SDA	SDI	I	SIM: SPI serial data input
	SDA	I/O	SIM: I ² C data line
SCK/SCL	SCK	I	SIM: SPI serial clock
	SCL	I	SIM: I ² C clock line
SDO/I2CA1	SDO	O	SIM: SPI serial data output
	I2CA1	I	I ² C slave address select
$\overline{\text{SCS}}$ /I2CA0	$\overline{\text{SCS}}$	I/O	SIM: SPI slave chip select
	I2CA0	I	I ² C slave address select
AVSS	AVSS	PWR	A/D converter negative power supply
AVDD	AVDD	PWR	A/D converter positive power supply
AN0	AN0	AI	A/D converter input channel 0
AN1	AN1	AI	A/D converter input channel 1
AN2	AN2	AI	A/D converter input channel 2
AN3	AN3	AI	A/D converter input channel 3
VERFP	VERFP	AI	A/D converter positive reference input
VERFN	VERFN	AI	A/D converter negative reference input
CAPP	CAPP	AI	A/D converter positive cap. input
CAPN	CAPN	AI	A/D converter negative cap. input
VDD	VDD	PWR	Digital positive power supply
VSS	VSS	PWR	Digital negative power supply

Pin Type Legends

Pin Type	Description
HXT	High frequency crystal oscillator
AI	Analog input
AO	Analog output
I	Digital input
O	Digital output
I/O	Digital input/output
PWR	Power

Block Diagram



Absolute Maximum Ratings

Supply Voltage	V _{SS} -0.3V to 6.0V	I _{OL} Total	80mA
Input Voltage	V _{SS} -0.3V to V _{DD} +0.3V	I _{OH} Total	-80mA
Storage Temperature	-60°C to 150°C	Total Power Dissipation	500mW
Operating Temperature	-40°C to 85°C		

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C Characteristics

T_a=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{DD}	Operating Voltage (HXT)	—	f _{sys} =f _{HXT} =4MHz	2.7	—	5.5	V
	Operating Voltage (HIRC)	—	f _{sys} =f _{HIRC} =4.9152MHz	2.7	—	5.5	V
I _{DD}	Operating Current (HXT)	3V	No load, all peripherals off,	—	0.50	0.75	mA
		5V	f _{sys} =f _{HXT} =4MHz	—	1.0	1.5	
	Operating Current (HIRC)	3V	No load, all peripherals off,	—	0.4	0.6	mA
		5V	f _{sys} =f _{HIRC} =4.9152MHz	—	0.8	1.2	
I _{STB}	Standby Current	3V	No load, all peripherals off	—	—	1	μA
		5V		—	—	2	

A.C Characteristics

Ta=25°C, unless otherwise specified

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
f _{sys}	System Clock (HXT)	2.7V~5.5V	f _{sys} =f _{HXT} =4MHz	—	4	—	MHz
	System Clock (HIRC)	2.7V~5.5V	f _{sys} =f _{HIRC} =4.9152MHz	—	4.9152	—	MHz
f _{HIRC}	High Speed Internal RC Oscillator (HIRC)	3V	Ta=25°C	-2%	4.9152	+2%	MHz
		3V±0.3V	Ta=0°C~70°C	-5%	4.9152	+5%	
			Ta=-40°C~85°C	-10%	4.9152	+10%	
		2.7V~5.5V	Ta=0°C~70°C	-7%	4.9152	+7%	
Ta=-40°C~85°C	-10%		4.9152	+10%			

A/D Converter Electrical Characteristics

 All specifications are tested under the conditions: Ta=-40°C~+85°C, AV_{DD}=V_{DD}=V_{REFP}=+5V, V_{REFN}=AV_{SS} and VREF Buffer is disabled, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Analog Inputs					
Full-Scale Input Voltage (A _{INP} -A _{INN})	—	±V _{REF} /Gain			V
Common-Mode Input Range	—	AV _{SS} +0.4	—	AV _{DD} -0.95	V
Differential Input Current	Gain=128	—	±2	—	nA
System Performance					
Resolution	No Missing Codes	24	—	—	Bit
Data Rate	ADC CLK=4.9152MHz	10	—	1280	SPS
Digital Filter Settling Time	Full Settling	—	4	—	Conversions
Integral Non-linearity (INL)	Gain=128	—	7	—	ppm
Input Offset Error	Gain=128	—	±1.6	—	ppm
Input Offset Drift	Gain=128	—	±4	—	nV/°C
Gain Error	Gain=128	—	±0.3	—	%
Gain Drift	Gain=128	—	±2.5	—	ppm/°C
Normal Mode Rejection	External Oscillator, f _{DATA} =10SPS f _{in} =50Hz or 60Hz, ±1Hz	—	130	—	dB
Common-Mode Rejection	at DC, Gain=128, ΔV=0.1V	—	110	—	dB
Power-Supply Rejection	at DC, Gain=128, ΔV=0.1V	—	120	—	dB
Voltage Reference Input					
Internal Voltage Reference Input (V _{REF})	V _{REF} =(V _{REFP} - V _{REFN})×0.5	0.75	AV _{DD} /2	(AV _{DD} +0.1)/2	V
Negative Reference Input (V _{REFN})	—	AV _{SS} -0.1	—	V _{REFP} -1.5	V
Positive Reference Input (V _{REFP})	—	V _{REFN} +1.5	—	AV _{DD} +0.1	V
Voltage Reference Input Current	—	—	10	—	nA
Power Supply (ADC power may be 5~10% more)					
Power Supply Voltage (AV _{DD} , V _{DD})	—	2.7	—	5.5	V
Analog Supply Current	AV _{DD} =5V, Gain=128	—	1350	2500	μA
	Power Down	—	—	1	
Digital Supply Current	DV _{DD} =5V, Gain=128	—	75	120	μA
	Power Down	—	—	1	
Digital					
Input Leakage	0<V _{IN} <V _{DD}	—	—	±10	μA
ADC Clock Input Frequency	—	1.0000	4.9152	6.0000	MHz

Effective Number of Bits (ENOB)
 $V_{REF}=2.5V$

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
10	22.8	22.8	22.8	22.7	22.7	22.4	21.8	20.9
20	22.3	22.2	22.2	22.2	22.2	22.0	21.4	20.5
40	21.5	21.5	21.5	21.5	21.4	21.2	20.8	20.1
80	20.9	20.9	20.9	20.8	20.8	20.6	20.3	19.6
160	20.1	20.1	20.1	20.1	20.1	20.0	19.7	19.1
320	19.3	19.3	19.3	19.3	19.2	19.2	19.0	18.5
640	18.3	18.3	18.3	18.3	18.3	18.2	18.1	17.7
1280	16.5	16.4	16.4	16.5	16.3	16.4	16.4	16.3

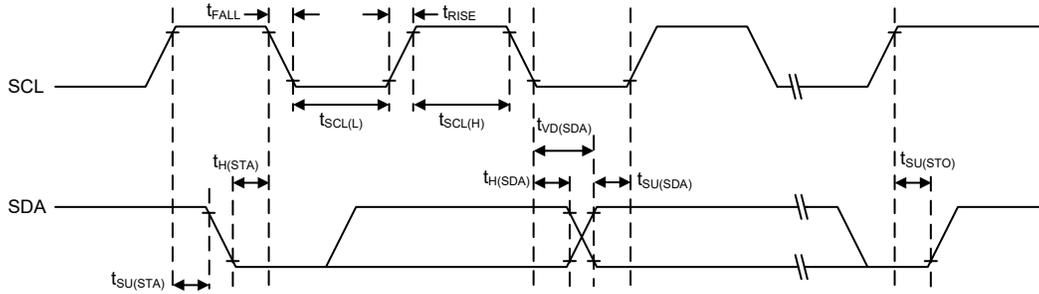
 $V_{REF}=1.65V$

Data Rate (SPS)	PGA Gain							
	1	2	4	8	16	32	64	128
10	22.2	22.3	22.2	22.2	22.0	21.9	21.3	20.4
20	21.8	21.7	21.7	21.7	21.6	21.4	20.8	19.9
40	20.5	20.5	20.4	20.4	20.4	20.4	20.0	19.4
80	20.1	20.1	20.1	20.1	20.0	19.9	19.5	18.9
160	19.7	19.7	19.7	19.7	19.6	19.5	19.1	18.5
320	19.0	19.0	19.0	19.0	19.0	19.0	18.9	18.0
640	18.2	18.2	18.2	18.2	18.2	18.1	17.9	17.4
1280	16.4	16.4	16.4	16.4	16.4	16.3	16.3	16.2

I²C Electrical Characteristics
 $T_a=25^{\circ}C$

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
f _{I2C}	I ² C Standard Mode (100kHz) f _{sys} Frequency <small>(Note)</small>	—	No clock debounce	2	—	—	MHz
	I ² C Fast Mode (400kHz) f _{sys} Frequency <small>(Note)</small>	—	No clock debounce	4	—	—	MHz
f _{SCL}	SCL Clock Frequency	3V/5V	Standard mode	—	—	100	kHz
			Fast mode	—	—	400	
t _{SCL(H)}	SCL Clock High Time	3V/5V	Standard mode	3.5	—	—	μs
			Fast mode	0.9	—	—	
t _{SCL(L)}	SCL Clock Low Time	3V/5V	Standard mode	3.5	—	—	μs
			Fast mode	0.9	—	—	
t _{FALL}	SCL and SDA Fall Time	3V/5V	Standard mode	—	—	1.3	μs
			Fast mode	—	—	0.34	
t _{RISE}	SCL and SDA Rise Time	3V/5V	Standard mode	—	—	1.3	μs
			Fast mode	—	—	0.34	
t _{SU(SDA)}	SDA Data Setup Time	3V/5V	Standard mode	0.25	—	—	μs
			Fast mode	0.1	—	—	
t _{H(SDA)}	SDA Data Hold Time	3V/5V	—	0.1	—	—	μs

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
t _{VD(SDA)}	SDA Data Valid Time	3V/5V	—	—	—	0.6	μs
t _{SU(STA)}	Start Condition Setup Time	3V/5V	Standard mode	3.5	—	—	μs
			Fast mode	0.6	—	—	
t _{H(STA)}	Start Condition Hold Time	3V/5V	—	0.6	—	—	μs
t _{SU(STO)}	Stop Condition Setup Time	3V/5V	Standard mode	3.5	—	—	μs
			Fast mode	0.6	—	—	

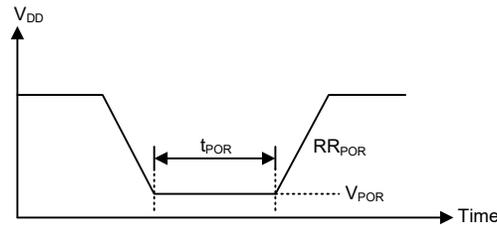


I²C Timing Diagram

Power on Reset Electrical Characteristics

T_a=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V _{DD}	Conditions				
V _{POR}	V _{DD} start voltage to ensure power-on reset	—	—	—	—	100	mV
RR _{POR}	V _{DD} rising rate to ensure power-on reset	—	—	0.035	—	—	V/ms
t _{POR}	Minimum time for V _{DD} stays at V _{POR} to ensure power-on reset	—	—	1	—	—	ms



Functional Description

The BH45B1525 contains a high accuracy multi-channel 24-bit Delta Sigma analog-to-digital converter which can directly interface to external analog signals, such as that from sensors or other control signals and convert these signals directly into a 24-bit digital value. In addition to the core analog-to-digital converter circuitry, the device also includes an internal Programmable Gain Amplifier, PGA. The PGA gain control determine the amplification gain for ADC input signal, giving users a flexible way of setting up an overall gain to achieve an optimum amplification of the input signal for their specific applications. The converter has a total of four inputs allowing the formation of two differential input

channels. The input signal can be amplified by PGA before entering the 24-bit Delta Sigma ADC modulator. The converter output is filtered via a SINC filter and the result stored as a 24-bit value in three data registers. A temperature sensor is included for A/D converter compensation due to temperature effects.

Internal Registers

The device is setup and operated using a series of internal registers. Device commands and data are written to and read from the device using its internal I²C or SPI interface. This list provides a summary of all internal registers, their detailed operation is described under their relevant sections in the functional description.

Address	Register Name	Bit							
		7	6	5	4	3	2	1	0
00H	REG0	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
01H	REG1	GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
02H	REG2	DR2	DR1	DR0	D4	D3	D2	D1	D0
03H	REG3	D7	D6	D5	D4	D3	D2	D1	D0
04H	REG4	D7	D6	D5	D4	D3	D2	D1	D0
05H	REG5	D7	D6	D5	D4	D3	D2	D1	D0
06H	REG6	D7	D6	D5	D4	D3	D2	D1	D0
07H	REG7	D7	D6	D5	D4	D3	D2	D1	D0
08H	REG8	D7	D6	D5	D4	D3	D2	D1	D0
09H	REG16	D7	D6	D5	D4	D3	D2	D1	D0
0AH	REG17	D15	D14	D13	D12	D11	D10	D9	D8
0BH	REG18	D23	D22	D21	D20	D19	D18	D17	D16
0CH	REG19	—	—	—	—	—	—	—	D0
0EH	SIMC0	—	—	—	—	—	—	—	SIMICF
0FH	SIMC2	—	—	CKPOLB	CKEG	MLS	CSEN	WCOL	—
10H	SIMTOC	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
11H	HIRCC	—	—	—	—	—	HIRCO	HIRCF	HIRCEN
12H	HXTC	—	—	—	—	HXTO	HXTM	HXTF	HXTEN

Register Initial Values

The following table shows the internal value of the individual register after a power on reset.

Register	Reset (Power on)	Register	Reset (Power on)
REG0	0000 0000	REG16	xxxx xxxx
REG1	0000 0000	REG17	xxxx xxxx
REG2	0000 0001	REG18	xxxx xxxx
REG3	0000 0001	REG19	---- --1
REG4	0010 0110	SIMC0	---- --0
REG5	0010 0000	SIMC2	0000 0000
REG6	0000 0111	SIMTOC	0000 0000
REG7	0000 0001	HIRCC	---- -000
REG8	0001 0100	HXTC	---- 0000

Table Legends

Item	Description
–	Unimplemented
u	Unchanged
x	Unknown

Oscillators

There are two kinds of oscillators used for this device, a fully internal oscillator and an external crystal oscillator. Oscillator selection and operations are selected through relevant control registers. Note that only one oscillator selection can be made. It is not allowed to enable both oscillators at the same time.

Type	Name	Freq.	Pins
External Crystal	HXT	4MHz	OSC1/OSC2
Internal High Speed RC	HIRC	4.9152MHz	—

Oscillator Types
Oscillator Control Registers

There are two control registers for the device oscillators, one for the internal oscillator and one for the external oscillator. Which oscillator is used in the device is determined by register configuration.

• HIRCC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	HIRCO	HIRCF	HIRCEN
R/W	—	—	—	—	—	R/W	R	R/W
POR	—	—	—	—	—	0	0	0

Bit 7~3 Unimplemented, read as "0"

Bit 2 **HIRCO**: HIRC Clock Output
 0: Disable
 1: Enable

When HIRCO is set to 1, then HIRC clock divided by 4096 will output through DRDYB pin.

Bit 1 **HIRCF**: HIRC Oscillator Stable Flag
 0: HIRC unstable
 1: HIRC stable

This bit is used to indicate whether the HIRC oscillator is stable or not. If the HIRC oscillator is selected then a full 16 clock cycle time is required for the oscillator to stabilise.

Bit 0 **HIRCEN**: HIRC Oscillator Enable Control
 0: Disable
 1: Enable

If this bit is set high to select the internal HIRC oscillator, then the HXT clock control bit HXTEN must be cleared to disable the external HXT oscillator.

• HXTC Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	HXTO	HXTM	HXTF	HXTEN
R/W	—	—	—	—	R/W	R/W	R	R/W
POR	—	—	—	—	0	0	0	0

Bit 7~4 Unimplemented, read as "0"

Bit 3 **HXTO**: HXT Clock Output
 0: Disable
 1: Enable

When HXTO is set to 1, the HXT clock divided by 4096 will output through DRDYB pin.

Bit 2 **HXTM**: HXT Mode Selection
 0: HXT frequency \leq 10MHz – Small sink/source current
 1: HXT frequency > 10MHz – Large sink/source current

This bit is used to select the HXT oscillator operating mode. If this bit is cleared to zero, the low voltage characteristics may be poor. If this bit is set to 1, the oscillator frequency and current are not guaranteed. Note that this bit must be properly configured before the HXT is enabled. When the HXTEN bit is set to 1 to enable the HXT oscillator, it is invalid to change the value of this bit.

Bit 1 **HXTF**: HXT Oscillator Stable Flag
 0: HXT unstable
 1: HXT stable

This bit is used to indicate whether the HXT oscillator is stable or not. When the HXTEN bit is set to 1 to enable the HXT oscillator, the HXTF bit will first be cleared to 0 and then set to 1 after the HXT oscillator is stable.

Bit 0 **HXTEN**: HXT Oscillator Enable Control
 0: Disable
 1: Enable

If this bit is set high to select the external HXT oscillator, then the HIRC clock control bit HIRCEN must be cleared to disable the internal HIRC oscillator.

Input Signal Gain Control Amplifier – PGA

An internal programmable gain amplifier is provided to amplify the differential input signal before being converted. All input signals to the analog to digital converter must pass through the PGA. In addition to the external analog input to be measured by the converter, there are several other internal analog voltage lines which can be connected to the converter. These come from a range of sources such as temperature sensor and are normally used for calibration purposes.

PGA Input Channel Selection

The PGA input channels can be determined using the REG0 register.

• REG0 Register

Bit	7	6	5	4	3	2	1	0
Name	CS7	CS6	CS5	CS4	CS3	CS2	CS1	CS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **CS7~CS0**: PGA Input Channel Pair Selection
 00010001: ADCINPUT(+)=AN0, ADCINPUT(-)=AN1
 00100010: ADCINPUT(+)=AN2, ADCINPUT(-)=AN3
 01100110: ADCINPUT(+)=V_{TSOP}, ADCINPUT(-)=V_{TSON} (Use temperature sensor)
 Others: Reserved

PGA Gain Setting

The input signals to the analog to digital converter will be amplified when pass through the PGA. This pre-processing of the input signal enables an optimal signal range to be setup to obtain a converted value with optimal resolution. The PGA gain can be setup to have a value range from 1 to 128 and is controlled by the GAIN[7:0] bits in the REG1 register.

• REG1 Register

Bit	7	6	5	4	3	2	1	0
Name	GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **GAIN7~GAIN0**: A/D Converter Gain Setting

00000000: Gain=1
 00000001: Gain=2
 00000010: Gain=4
 00000011: Gain=8
 00000100: Gain=16
 00000101: Gain=32
 00000110: Gain=64
 01000110: Gain=128
 Others: Reserved

Analog to Digital Converter Operation

The analog to digital converter received a differential analog signal from the PGA output and converts in using a Delta Sigma converter into a 24-bit digital value. Since the REG3 register value is recommended to be 0100_1111b, the A/D converter is powered up and the A/D converter clock input is enabled. The A/D converter converted data will be update continuously by new converted data. The A/D converter output data rate is selected by the DR2~DR0 bits in the REG2 register.

A/D Converter Control Registers Description

The overall operation of the converter is controlled by a series of control registers.

• REG2 Register

Bit	7	6	5	4	3	2	1	0
Name	DR2	DR1	DR0	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	1

Bit 7~5 **DR2~DR0**: A/D Converter Output Data Rate Selection ($f_{ADC}=81.92kHz$)

000: $f_{ADC}/64=1280Hz$
 001: $f_{ADC}/128=640Hz$
 010: $f_{ADC}/256=320Hz$
 011: $f_{ADC}/512=160Hz$
 100: $f_{ADC}/1024=80Hz$
 101: $f_{ADC}/2048=40Hz$
 110: $f_{ADC}/4096=20Hz$
 111: $f_{ADC}/8192=10Hz$

Bit 4~0 **D4~D0**: Reserved bits

This bit field must be fixed at a value of "00001".

• REG3 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	1

Bit 7~0 0100_1111b is recommended

• REG4 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	1	1	0

Bit 7~0 0010_0000b is recommended

• REG5 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	0	0	0	0	0

Bit 7~0 1010_0000b is recommended

• REG6 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	1	1	1

Bit 7~0 1000_1111b is recommended

• REG7 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	1

Bit 7~0 0100_1111b is recommended

• REG8 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	1	0	1	0	0

Bit 7~0 0001_0000b is recommended

• REG19 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	D0
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	1

Bit 7~0 0000_0001b is recommended

A/D Converter Reference Voltage

The differential reference voltage supply to the A/D Converter can be supplied from an external reference source supplied on pins VREFP and VREFN.

A/D Converted Data

The A/D converter data is stored in three individual registers, REG16, REG17 and REG18. The converted data is related to the input voltage and the PGA selection setup and is generated in a two's complement binary code format. The length of this output code is 24 bits and the MSB is a signed bit. When the MSB is "0", this indicates that the input is "positive", while if the MSB is "1", this indicates that the input is "negative". The maximum value data is 8388607 and the minimum value is -8388608. If the input signal exceeds the maximum value, the converted data is limited to 8388607, and if the input signal is less than the minimum value, the converted data is limited to -8388608.

Temperature Sensor

The device includes a fully internal temperature sensor to allow for compensation due to temperature effects. By selecting the PGA input channels as V_{TSOP} and V_{TSON} signals, the A/D Converter can obtain temperature information and then use the result to compensate the A/D converted data to minimize the effects of temperature.

• REG16 Register

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 A/D Conversion Data Register bit 7 ~ bit 0

• REG17 Register

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 A/D Conversion Data Register bit 15 ~ bit 8

• REG18 Register

Bit	7	6	5	4	3	2	1	0
Name	D23	D22	D21	D20	D19	D18	D17	D16
R/W	R	R	R	R	R	R	R	R
POR	x	x	x	x	x	x	x	x

"x": Unknown

Bit 7~0 A/D Conversion Data Register bit 23 ~ bit 16

External Interface Communication

The device contains a Serial Interface Module, which includes I²C and SPI interfaces, to allow an easy method of communication with external peripheral hardware. The SIM function is always enabled. As both interface types share the same pins and registers, the choice of whether the SPI or I²C type is used is made using the I2CSB pin. Note that after the power on reset, the I2CSB pin is low.

I2CSB	I ² C/SPI	SDI/ SDA	SCK/ SCL	SDO/ I2CA1	SCS/ I2CA0
0	I ² C	SDA	SCL	I2CA1	I2CA0
1	SPI	SDI	SCK	SDO	SCS

I²C Serial Interface

The device will communicate with external hardware using its internal I²C interface if the I2CSB pin is low. Originally developed by Philips, the I²C interface is a two line low speed serial interface for bidirectional synchronous serial data transfer between different ICs or modules. With the advantage of only two lines for communication, a relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interfaces type for many applications.

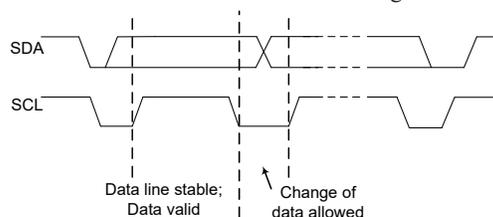
I²C Operation

The I²C serial interface is a two line interface, a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors. When the bus is free, both lines are high. Devices connected to the bus must have open-drain or open-collector outputs to implement a wired-or function. Data transfer is initiated only when the bus is not busy.

Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus. When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus, and it is only the master that will drive the SCL clock line. This device only operates in the slave mode, and will therefore only operate in response to the master. There are two methods for this device to transfer data on the I²C bus, the slave transmit mode and the slave receive mode.

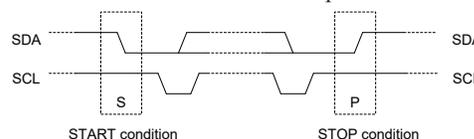
Data Validity

The data on the SDA line must be stable during the high period of the serial clock. The high or low state of the data line can only change when the clock signal on the SCL line is low as shown in the diagram.



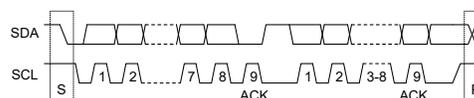
START and STOP Conditions

Normally the SDA line can only change when the SCL line is low. There are two exceptions however and that is for the Start and Stop conditions, where the SCL line will be forced high by the master and the SDA line will change state. As the diagram shows, when the SCL line is high, a high to low SDA transition indicates a Start condition and a low to high SDA line transition indicates a Stop condition.



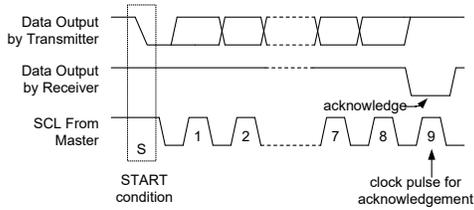
Byte Format

Every byte put on the SDA line must be 8-bit long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit, MSB, first.



Acknowledge

Each bytes of eight bits is followed by one acknowledge bit. This Acknowledge bit is a low level placed on the bus by the receiver. The master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an Acknowledge, ACK, after the reception of each byte. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse so that it remains stable low during the high period of this clock pulse.



Slave Addressing

The slave address byte is the first byte received following the START condition from the master device. The first seven bits of the first byte make up the slave address. The eighth bit defines a read or write operation to be performed. When the R/W bit is "1", then a read operation is selected. A "0" selects a write operation. When an address byte is sent, the device compares the first seven bits after the START condition. If they match, the device outputs an Acknowledge on the SDA line.

I²C Address Selection

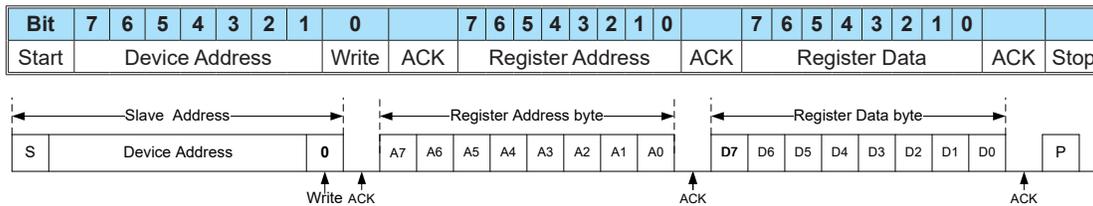
As this device only operates as a slave, and as it may be connected to a common I²C bus along with other I²C devices, it will require a specific address for it to be communicated to by the external master. The address of the device is setup using the I2CA0 and I2CA1 pins which allows for 4 different address values. However as the I2CA0 and I2CA1 pins are shared with the SPI interface pins, their addressing function is only enabled when the I2CSB pin is low. When the I2CSB pin is high the I2CA0 and I2CA1 addressing function will be disabled. Note that only the high 7 bits of the slave address is effective.

I2CSB	I2CA1	I2CA0	I ² C Slave Address
0	0	0	0xA0
	0	1	0xB0
	1	0	0xC0
	1	1	0xD0

I²C Interface Read/Write Operation

• I²C Interface Write Operation

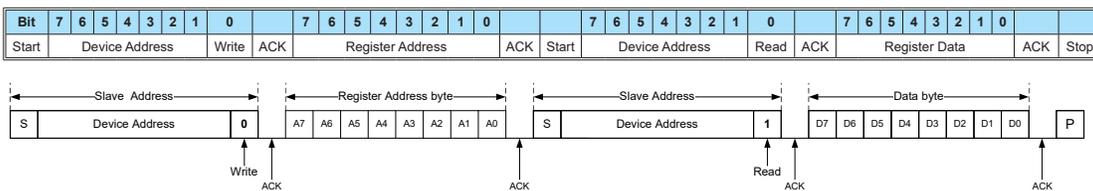
A single data byte write operation requires a START condition, a slave address with an R/W bit, a valid Register Address byte, a Data byte and a STOP condition.



I²C Interface Single Data Byte Write Operation

• I²C Interface Read Operation

In this mode, the master reads the device data after setting the slave address. Following the R/W bit (=‘0’) is an acknowledge bit and the register address byte which is written to the internal address pointer. After the start address of the Read Operation has been configured, another START condition and the slave address transferred on the bus followed by the R/W bit (=‘1’). Then the MSB of the data which was addressed is transmitted first on the I²C bus.



I²C Interface Single Data Byte Read Operation

I²C Timeout Function

The I²C interface includes a timeout function which is controlled by a single register. This register sets the overall enable/disable function as well as the timeout value in system clock units. Determining whether the I²C bus has timed out is implemented by reading the SIMTOF bit. This bit will be automatically set high when the I²C bus times out, but needs to be cleared manually by the application program.

• SIMTOC Register

Bit	7	6	5	4	3	2	1	0
Name	SIMTOEN	SIMTOF	SIMTOS5	SIMTOS4	SIMTOS3	SIMTOS2	SIMTOS1	SIMTOS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7 **SIMTOEN**: I²C Time-out Control

0: Disable

1: Enable

Bit 6 **SIMTOF**: I²C Time-out Flag

0: Not occurred

1: Occurred

This bit is set by Time-out function and can only be cleared by the application program.

Bit 7 **SIMTOS5~SIMTOS0**: I²C Time-out Selection Time

0: Disable

1: Enable

The I²C Time-Out clock source is $f_{SUB}/32$. ($f_{SUB}=f_{SYS}/128$)

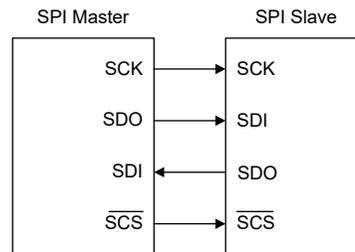
The I²C Time-Out time is $(SIMTOS[5:0]+1) \times (32/f_{SUB})$.

SPI Serial Interface

The device will communicate with external hardware using its internal SPI interface if the I2CSB pin is high. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

SPI Interface Operation

The SPI interface is a four line interface with pin names SDI, SDO, SCK and \overline{SCS} . Pins SDI and SDO are the Serial Data Input and Serial Data Output lines. The SCK pin is the Serial Clock line and \overline{SCS} is the Slave Select line. The communication is full duplex and operates as a slave/master type, where the device only operates as a slave. The master uses I/O pins to select the slave device.



SPI Master/Slave Connection

SPI Registers Description

Two registers control the overall operation of the SPI interface.

• SIMC0 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	—	SIMICF
R/W	—	—	—	—	—	—	—	R/W
POR	—	—	—	—	—	—	—	0

Bit 7~1 Unimplemented, read as "0"

Bit 0 **SIMICF**: SIM SPI Incomplete Flag

0: SIM SPI incompleting is not occurred

1: SIM SPI incompleting is occurred

The SIMICF bit is determined by \overline{SCS} pin. When \overline{SCS} pin is set high, the SPI counter will be cleared.

• SIMC2 Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	CKPOLB	CKEG	MLS	CSEN	WCOL	—
R/W	—	—	R/W	R/W	R/W	R/W	R/W	—
POR	—	—	0	0	0	0	0	—

Bit 7~6 Unimplemented, read as "0"

Bit 5 **CKPOLB**: Determines the Base Condition of the Clock Line

0: The SCK line will be high when the clock is inactive

1: The SCK line will be low when the clock is inactive

The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.

Bit 4 **CKEG**: Determines SPI SCK Active Clock Edge Type

CKPOLB=0

0: SCK is high base level and data capture at SCK rising edge

1: SCK is high base level and data capture at SCK falling edge

CKPOLB=1

0: SCK is low base level and data capture at SCK falling edge

1: SCK is low base level and data capture at SCK rising edge

The CKEG and CKPOLB bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.

Bit 3 **MLS**: SPI Data Shift Order

0: LSB first

1: MSB first

This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.

Bit 2 **CSEN**: SPI \overline{SCS} Pin Control

0: Disable

1: Enable

The CSEN bit is used as an enable/disable for the \overline{SCS} pin. If this bit is low, then the \overline{SCS} pin will be disabled and placed into a floating condition. If the bit is high the \overline{SCS} pin will be enabled and used as a select pin.

Bit 1 **WCOL**: SPI Write Collision Flag

0: No collision

1: Collision

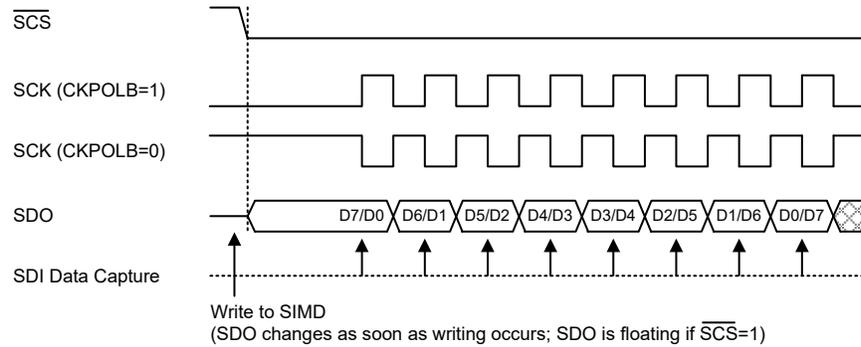
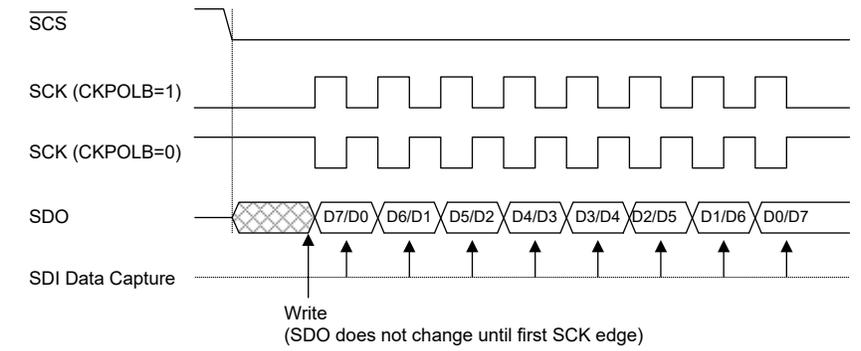
The WCOL flag is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMD register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program.

Bit 0 Unimplemented, read as "0"

SPI Communication

After the SPI interface is enabled using the application program, then in the Slave Mode, when the clock signal from the master has been received, any data in the SPI TX FIFOs will be transmitted by the SDO pin and any data on the SDI pin will be shifted into the SPI RX FIFOs.

The master should output a \overline{SCS} signal to enable the slave device before a clock signal is provided. The slave data to be transferred should be well prepared at the appropriate moment relative to the SCK signal depending upon the configurations of the CKPOLB bit and CKEG bit. The accompanying timing diagram shows the relationship between the slave data and SCK signal for various configurations of the CKPOLB and CKEG bits. The SPI will continue to function if the SPI clock source is still active.



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the \overline{SCS} level.

SPI Interface Read/Write Operation

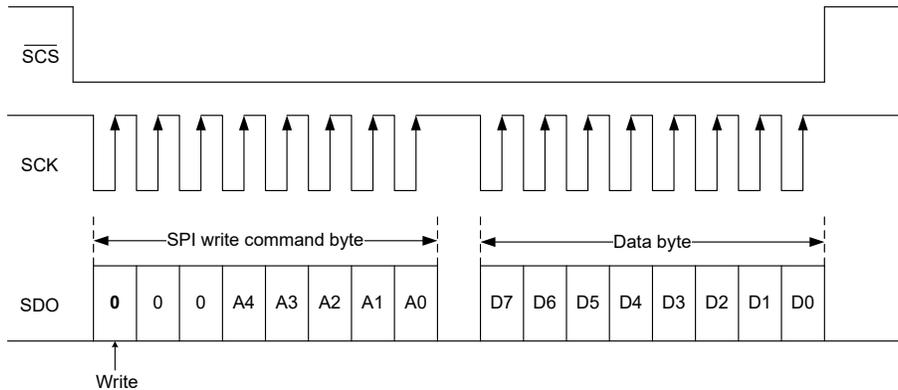
The first byte of SPI is the command to determine Read or Write and Register address. When finish the command, the following byte is the data. The SPI read/write command byte is shown as below.

Bit	7	6	5	4	3	2	1	0
Name	SPIR/SPIW	—	—	SPIA4	SPIA3	SPIA2	SPIA1	SPIA0
Description	Read=1 Write=0	Reserved	Reserved	Address bit 4	Address bit 3	Address bit 2	Address bit 1	Address bit 0
Status	1/0	0	0	1/0	1/0	1/0	1/0	1/0

◆ SPI Interface Write Operation

The single data byte write operation consists of an SPI write command, which contains the register address, and a write data byte.

SCS	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	SCS
High → Low	Write	Register Address							Register Data							Low → High	

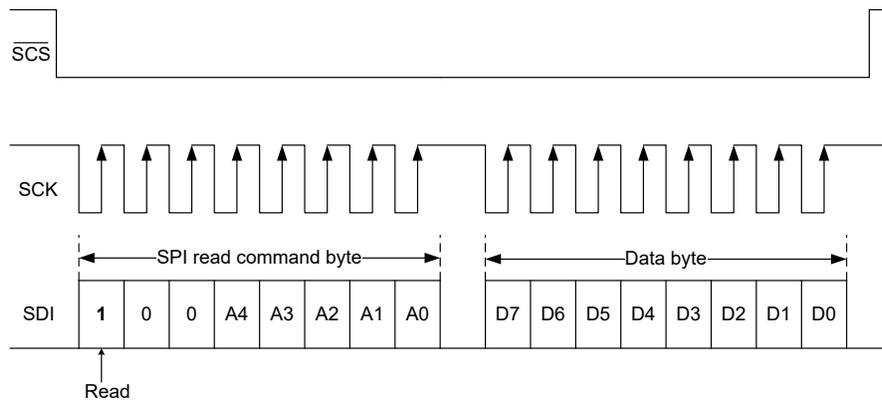


SPI Interface Single Data Byte Write Operation

SPI Interface Read Operation

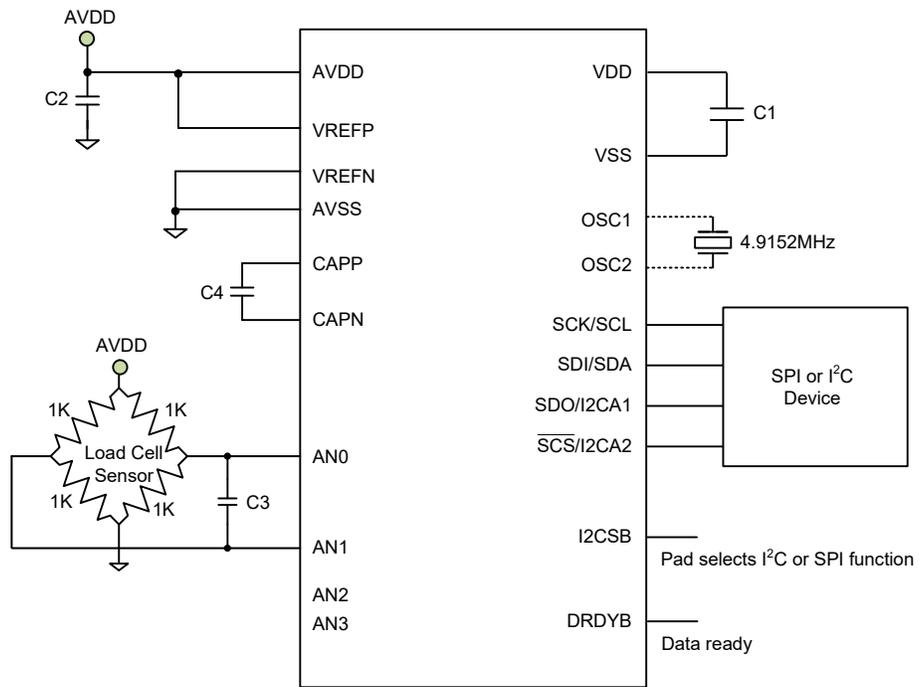
In this mode, the master reads the device data after sending the SPI read command when the $\overline{\text{SCS}}$ pin changes state from high to low. Following the read/write control bit, which is contained in the SPI read command, is the register address which is written to the internal address pointer. After that the MSB of the data which was addressed is transmitted first on the SPI bus.

SCS	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	SCS
High → Low	Read	Register Address							Register Data							Low → High	



SPI Interface Single Data Byte Read Operation

Application Circuits

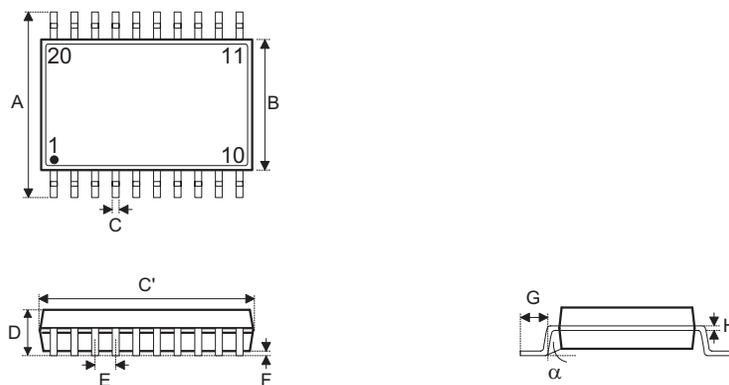


Package Information

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Additional supplementary information with regard to packaging is listed below. Click on the relevant section to be transferred to the relevant website page.

- Package Information (include Outline Dimensions, Product Tape and Reel Specifications)
- Packing Materials Information
- Carton information

20-pin SSOP (150mil) Outline Dimensions


Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.236 BSC		
B	0.154 BSC		
C	0.008	—	0.012
C'	0.341 BSC		
D	—	—	0.069
E	0.025 BSC		
F	0.004	—	0.010
G	0.016	—	0.050
H	0.004	—	0.010
α	0°	—	8°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	6.00 BSC		
B	3.90 BSC		
C	0.20	—	0.30
C'	8.66 BSC		
D	—	—	1.75
E	0.635 BSC		
F	0.10	—	0.25
G	0.41	—	1.27
H	0.10	—	0.25
α	0°	—	8°

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