Ultra Low Power/High Speed CMOS SRAM 512K X 8 bit

Green package materials are compliant to RoHS

BH62UV4000

■ FEATURES

- Wide V_{CC} low operation voltage : 1.65V ~ 3.6V
- Ultra low power consumption :
  - V_{CC} = 3.6V Operation current : 10mA (Max.)at 55ns
    - 2mA (Max.) at 1MHz
    - Standby current : 2.0uA (Typ.) at 3.0V/25°C
  - V_{CC} = 1.2V Data retention current : 1.0uA at 25°C
- High speed access time :
  - -55 55ns (Max.) at V_{CC}=1.65~3.6V
- Automatic power down when chip is deselected
- Easy expansion with $\overline{CE}$ and $\overline{OE}$ options
- Three state outputs and TTL compatible
- Fully static operation, no clock, no refresh
- Data retention supply voltage as low as 1.0V

■ DESCRIPTION

The BH62UV4000 is a high performance, ultra low power CMOS Static Random Access Memory organized as 524,288 by 8 bits and operates in a wide range of 1.65V to 3.6V supply voltage.

Advanced CMOS technology and circuit techniques provide both high speed and low power features with typical operating current of 1.5mA at 1MHz at 3.6V/25°C and maximum access time of 55ns at 1.65V/85°C.

Easy memory expansion is provided by an active LOW chip enable ($\overline{CE}$) and active LOW output enable ($\overline{OE}$) and three-state output drivers.

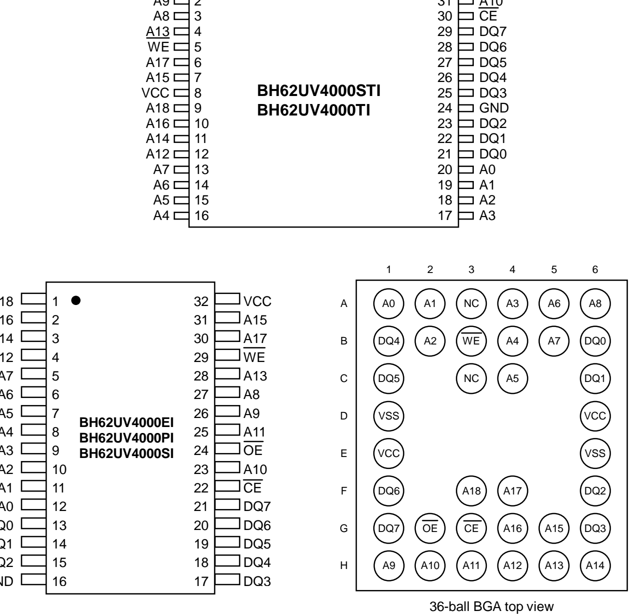
The BH62UV4000 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.

The BH62UV4000 is available in DICE form, JEDEC standard 32 pin 450mil Plastic SOP, 400mil TSOP-II, 600mil Plastic DIP, 8mmx13.4mm STSOP, 8mmx20mm TSOP and 36-ball BGA package.

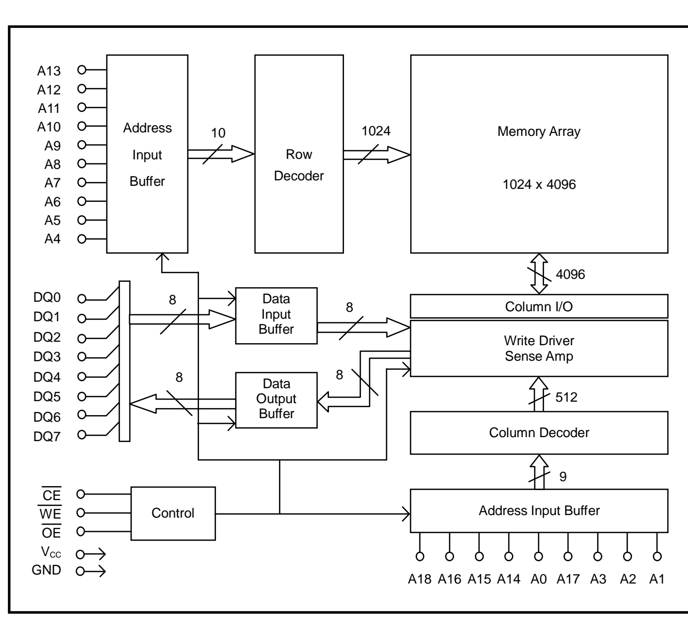
■ POWER CONSUMPTION

PRODUCT FAMILY	OPERATING TEMPERATURE	POWER DISSIPATION								PKG TYPE
		Icc STANDBY (I_{CCSB1}, Max)		Icc Operating (I_{CC}, Max)						
		V_{CC}=3.6V	V_{CC}=1.8V	V_{CC}=3.6V			V_{CC}=1.8V			
				1MHz	10MHz	$f_{Max.}$	1MHz	10MHz	$f_{Max.}$	
BH62UV4000DI	Industrial -40°C to +85°C	10uA	10uA	2mA	6mA	10mA	1.5mA	5mA	8mA	DICE
BH62UV4000EI										TSOP-II
BH62UV4000HI										BGA-36-0608
BH62UV4000PI										PDIP-32
BH62UV4000SI										SOP-32
BH62UV4000STI										STSOP-32
BH62UV4000TI										TSOP-32

■ PIN CONFIGURATIONS



■ BLOCK DIAGRAM



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Detailed product characteristic test report is available upon request and being accepted.

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PIN DESCRIPTIONS

Name	Function
A0-A18 Address Input	These 19 address inputs select one of the 524,288 x 8 bit in the RAM
$\overline{CE}$ Chip Enable 1 Input	$\overline{CE}$ is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and is in standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impendence state when $\overline{OE}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	8 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power Supply
V_{SS}	Ground

TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O OPERATION	V_{CC} CURRENT
Chip De-selected (Power Down)	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	L	H	H	High Z	I_{CC}
Read	L	H	L	D_{OUT}	I_{CC}
Write	L	L	X	D_{IN}	I_{CC}

NOTES: H means V_{IH}; L means V_{IL}; X means don't care (Must be V_{IH} or V_{IL} state)

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5(2) to 4.6V	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. –2.0V in case of AC pulse width less than 30 ns

OPERATING RANGE

RANG	AMBIENT TEMPERATURE	V_{CC}
Industrial	$-40^{O}C$ to $+ 85^{O}C$	1.65V ~ 3.6V

CAPACITANCE (1) ($T_A = 25^{O}C$, f = 1.0MHz)

SYMBOL	PAMAMETER	CONDITIONS	MAX.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{IO}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not 100% tested.

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n DC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP.[1]	MAX.	UNITS
V_{CC}	Power Supply			1.65	--	3.6	V
V_{IL}	Input Low Voltage		V_{CC}=1.8V	-0.3[2]	--	0.4	V
			V_{CC}=3.6V			0.8	
V_{IH}	Input High Voltage		V_{CC}=1.8V	1.4	--	V_{CC}+0.3[3]	V
			V_{CC}=3.6V	2.2			
I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CC}, $\overline{CE}$ = V_{IH}		--	--	1	uA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}, $\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}		--	--	1	uA
V_{OL}	Output Low Voltage	V_{CC} = Max, I_{OL} = 0.1mA	V_{CC}=1.8V	--	--	0.2	V
		V_{CC} = Max, I_{OL} = 2.0mA	V_{CC}=3.6V			0.4	
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -0.1mA	V_{CC}=1.8V	V_{CC}-0.2	--	--	V
		V_{CC} = Min, I_{OH} = -1.0mA	V_{CC}=3.6V	2.4			
I_{CC}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, f = F_{MAX}[4]	V_{CC}=1.8V	--	--	8	mA
			V_{CC}=3.6V			10	
I_{CC1}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, I_{DQ} = 0mA, f = 1MHz	V_{CC}=1.8V	--	1.0	1.5	mA
			V_{CC}=3.6V		1.5	2.0	
I_{CCSB}	Standby Current – TTL	$\overline{CE}$ = V_{IH}, I_{DQ} = 0mA	V_{CC}=1.8V	--	--	0.5	mA
			V_{CC}=3.6V			1.0	
I_{CCSB1}	Standby Current – CMOS	$\overline{CE}$ ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V	V_{CC}=1.8V	--	2.0	10	uA
			V_{CC}=3.6V		2.0[5]	10	

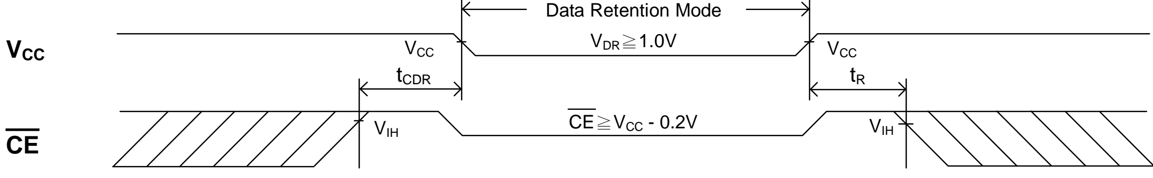
1. Typical characteristics are at T_A=25°C and not 100% tested.
2. Undershoot: -1.0V in case of pulse width less than 20 ns.
3. Overshoot: V_{CC}+1.0V in case of pulse width less than 20 ns.
4. F_{MAX}=1/t_{RC}.
5. V_{CC}=3.0V

n DATA RETENTION CHARACTERISTICS (T_A = -40°C to +85°C)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. [1]	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$\overline{CE}$ ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V		1.0	--	--	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≧ V_{CC}-0.2V, V_{IN} ≧ V_{CC}-0.2V or V_{IN} ≦ 0.2V	V_{CC}=1.2V	--	1.0	5.0	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform		0	--	--	ns
t_R	Operation Recovery Time			t_{RC} [2]	--	--	ns

1. Typical characteristics are at T_A=25°C and not 100% tested.
2. t_{RC} = Read Cycle Time.

n LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE}$ Controlled)



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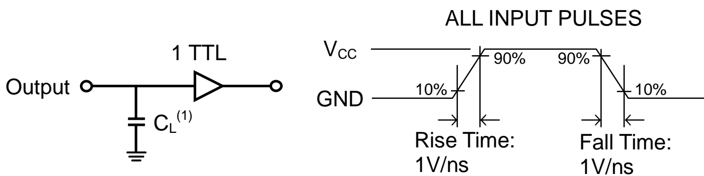
AC TEST CONDITIONS
(Test Load and Input/Output Reference)

Input Pulse Levels		V_{CC} / 0V
Input Rise and Fall Times		1V/ns
Input and Output Timing Reference Level		0.5Vcc
Output Load	t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{WHZ}, t_{OW}	C_L = 5pF+1TTL
	Others	C_L = 30pF+1TTL



1. Including jig and scope capacitance.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM "H" TO "L"	WILL BE CHANGE FROM "H" TO "L"
	MAY CHANGE FROM "L" TO "H"	WILL BE CHANGE FROM "L" TO "H"
	DON'T CARE ANY CHANGE PERMITTED	CHANGE : STATE UNKNOW
	DOES NOT APPLY	CENTER LINE IS HIGH INPEDANCE "OFF" STATE

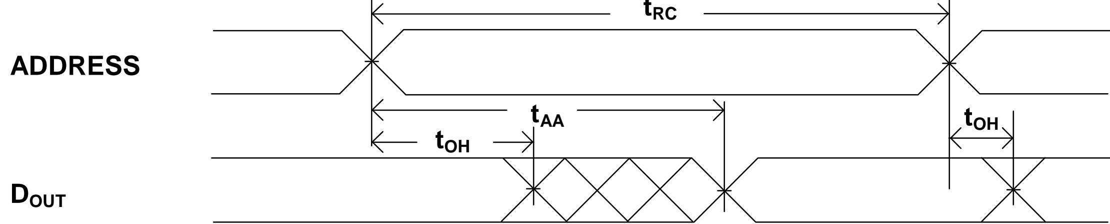
AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

READ CYCLE

JEDEC PARAMETER NAME	PARANETER NAME	DESCRIPTION	CYCLE TIME : 55ns			UNITS
			MIN.	TYP.	MAX.	
t_{AVAX}	t_{RC}	Read Cycle Time	55	--	--	ns
t_{AVQX}	t_{AA}	Address Access Time	--	--	55	ns
t_{E1LQV}	t_{ACS}	Chip Select Access Time	--	--	55	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	--	--	30	ns
t_{E1LQX}	t_{CLZ}	Chip Select to Output Low Z	10	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output Low Z	10	--	--	ns
t_{E1HQZ}	t_{CHZ}	Chip Select to Output High Z	--	--	30	ns
t_{GHQZ}	t_{OHZ}	Output Enable to Output High Z	--	--	25	ns
t_{AVQX}	t_{OH}	Data Hold from Address Change	10	--	--	ns

SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE 1 (1,2,4)



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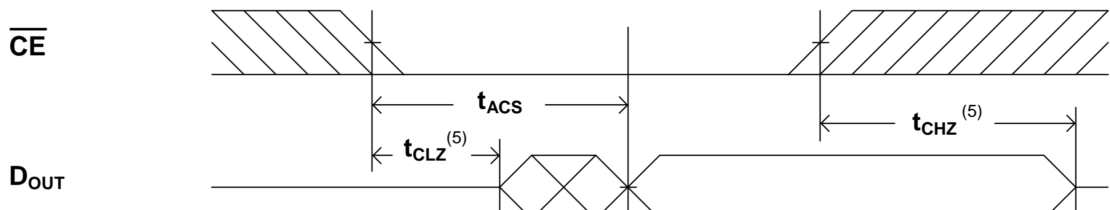
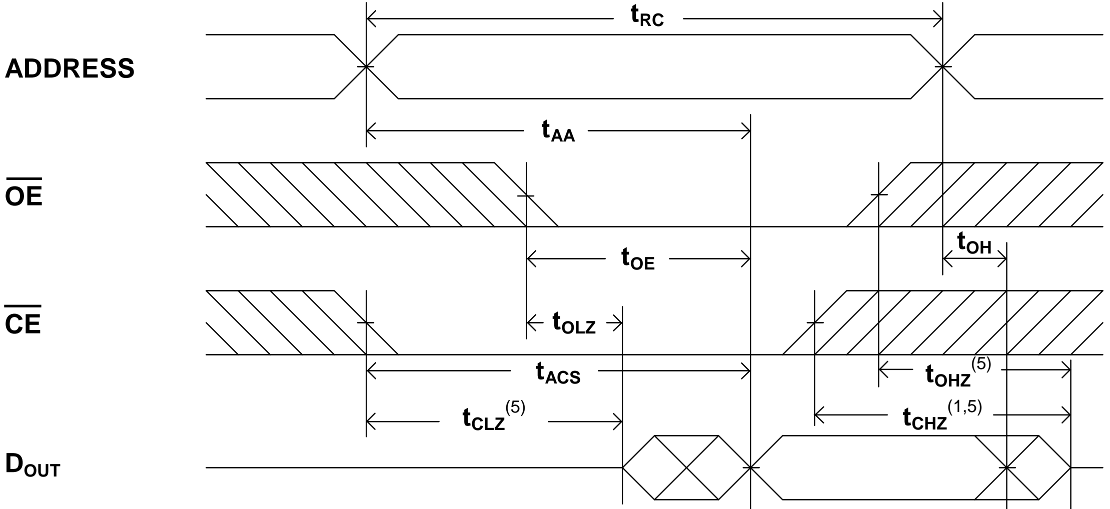
READ CYCLE 2 (1,3,4)



READ CYCLE 3 (1, 4)



NOTES:
1. $\overline{WE}$ is high in read Cycle.
2. Device is continuously selected when $\overline{CE} = V_{IL}$
3. Address valid prior to or coincident with $\overline{CE}$ transition low and/or CE2 transition high.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF.
   The parameter is guaranteed but not 100% tested.

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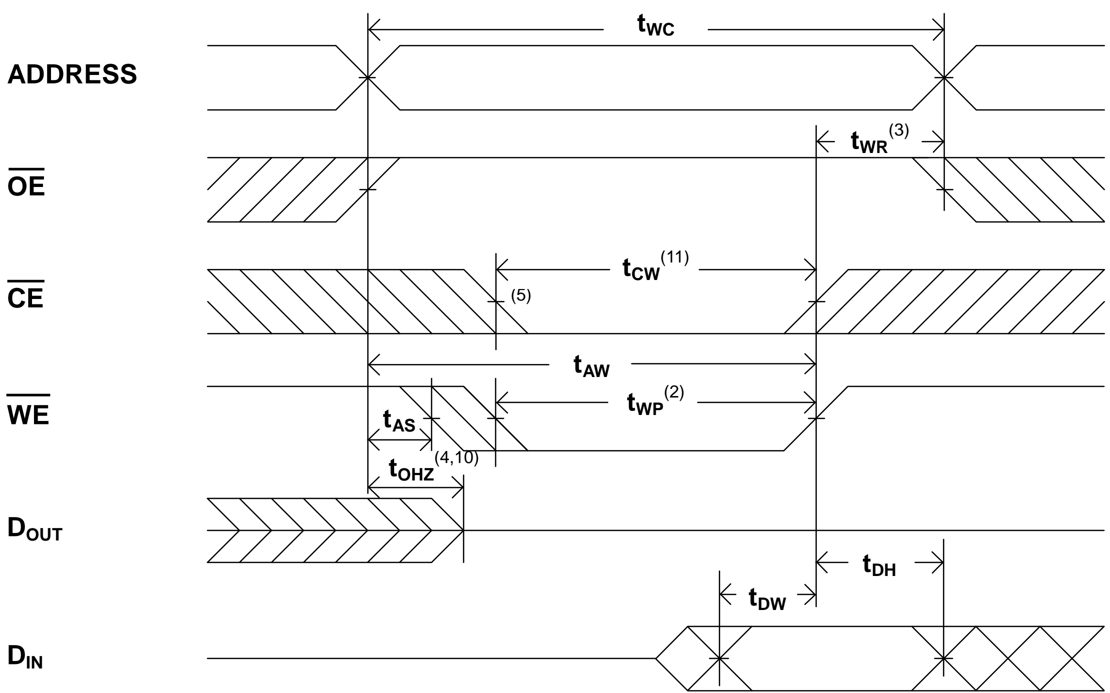
n AC ELECTRICAL CHARACTERISTICS (T_A = -40°C to +85°C)

WRITE CYCLE

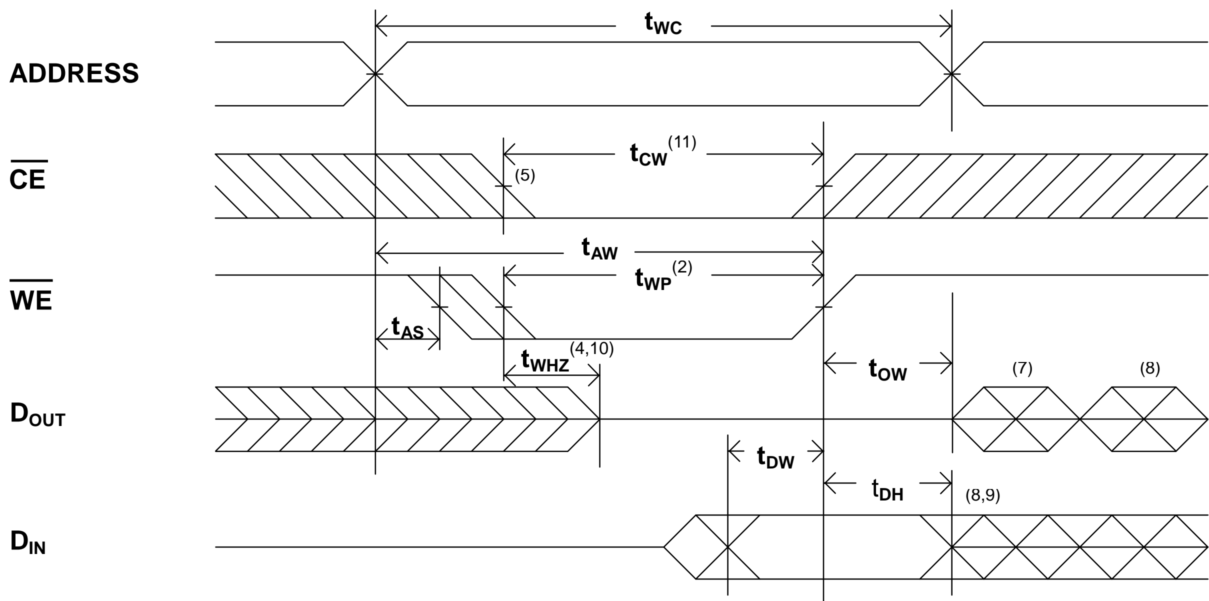
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 55ns			UNITS
			MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	55	--	--	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45	--	--	ns
t_{ELWH}	t_{CW}	Chip Select to End of Write	45	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	--	--	ns
t_{WHAX}	t_{WR}	Write Recovery Time (CE, WE)	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output High Z	--	--	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	25	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	--	--	ns

n SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE 1 (1)



WRITE CYCLE 2 (1,6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE}$ and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or $\overline{WE}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured $\pm$ 500mV from steady state with C_L = 5pF.
    The parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{CE}$ going low to the end of write.

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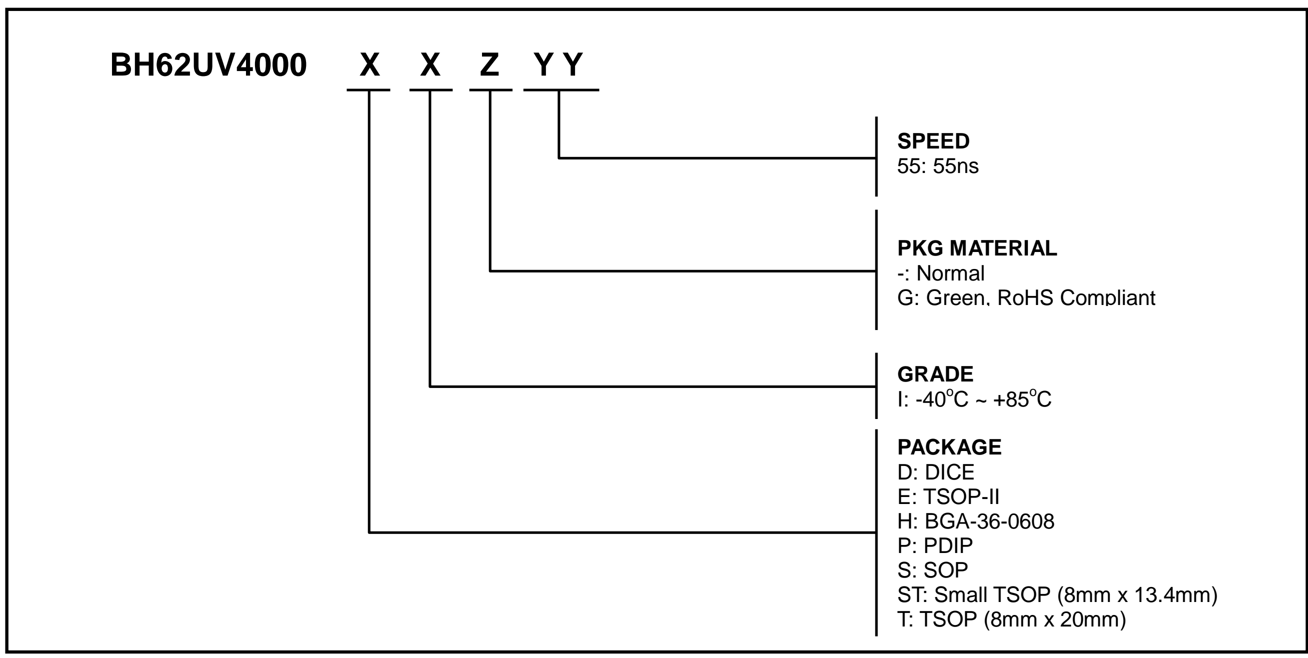
ORDERING INFORMATION



Note:
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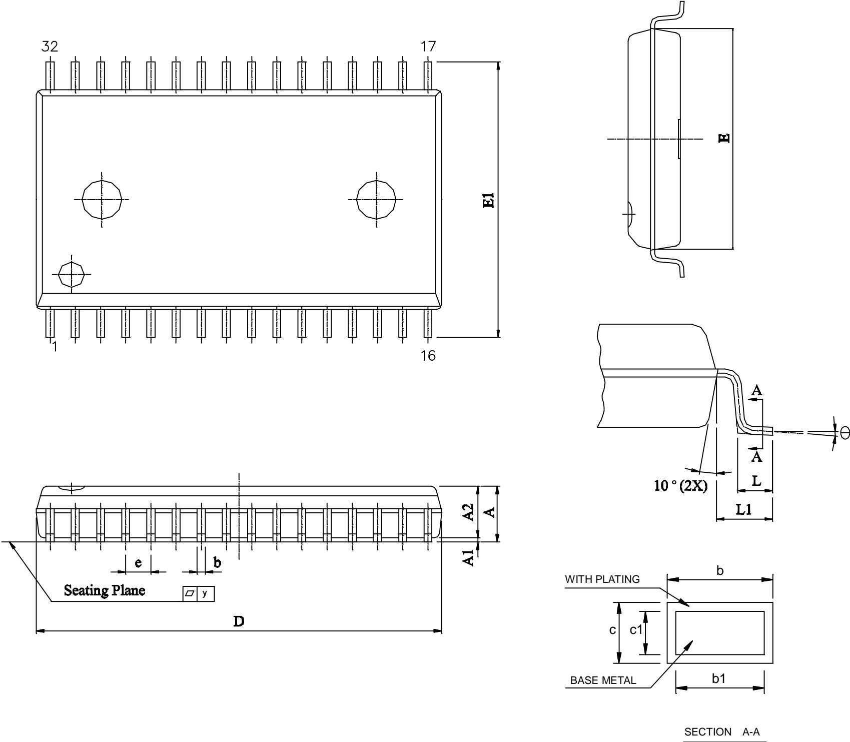
PACKAGE DIMENSIONS



SYMBOL \ UNIT	INCH	MM
A	0.111±0.007	2.821±0.176
A1	0.009±0.005	0.229±0.127
A2	0.1055±0.0055	2.680±0.140
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.46
c	0.006 ~ 0.012	0.15 ~ 0.32
c1	0.006 ~ 0.011	0.15 ~ 0.28
D	0.805±0.005	20.447±0.127
E	0.445±0.005	11.303±0.127
E1	0.555±0.012	14.097±0.305
e	0.050±0.006	1.270±0.152
L	0.033±0.010	0.834±0.25
L1	0.055±0.008	1.397±0.203
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

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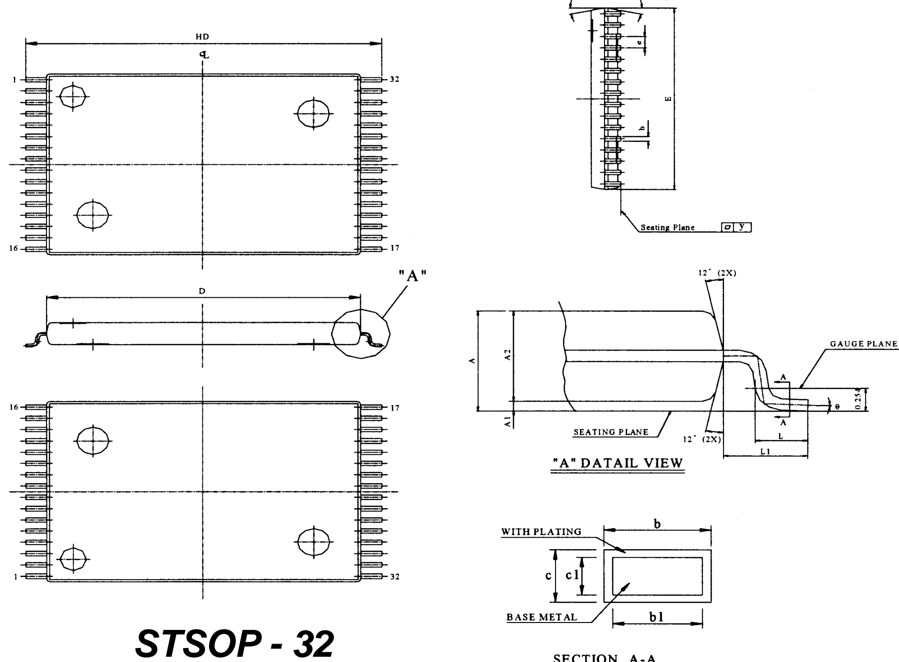
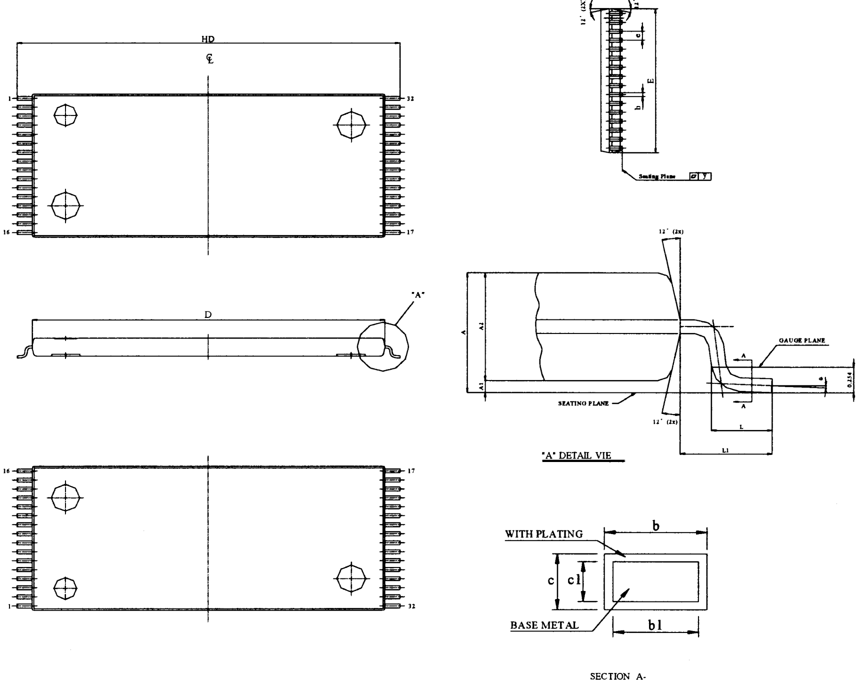
n PACKAGE DIMENSIONS (continued)



UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.528± 0.008	13.40± 0.20
L	$0.0197^{+0.008}_{-0.004}$	$0.50^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°



UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.724± 0.004	18.40± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.787± 0.008	20.00± 0.20
L	$0.0197^{+0.008}_{-0.004}$	$0.50^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

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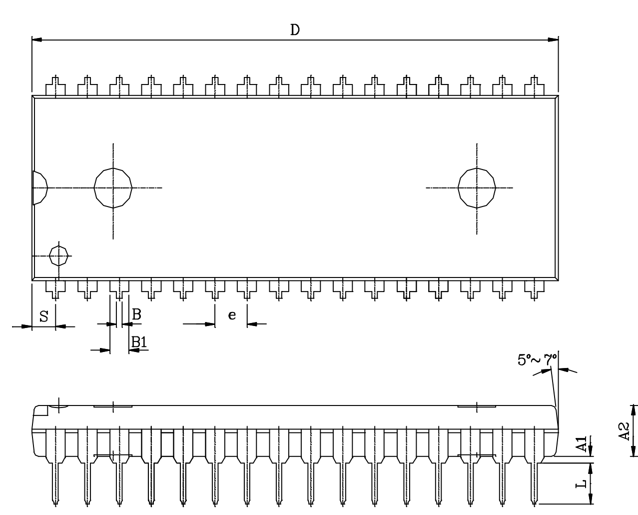
■ PACKAGE DIMENSIONS (continued)

UNIT / SYMBOL	INCH(BASE)	MM(REF)
A1	0.010(MIN)	0.254(MIN)
A2	0.154±0.005	3.912±0.127
B	0.018±0.005	0.457±0.127
B1	0.050±0.005	1.270±0.127
c	0.010±0.004	0.254±0.102
D	1.650±0.005	41.910±0.127
E	0.600±0.010	15.240±0.254
E1	0.544±0.004	13.818±0.102
e	0.100(TYP)	2.540(TYP)
eB	0.650±0.020	16.510±0.508
L	0.130±0.010	3.302±0.254
S	0.075±0.010	1.905±0.254
Q1	0.070±0.005	1.778±0.127



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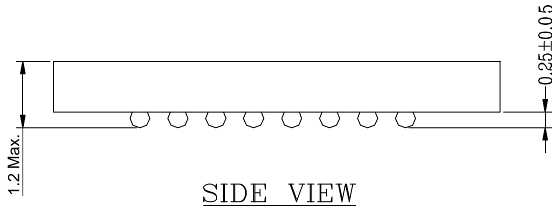


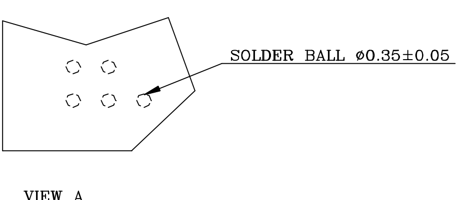
SIDE VIEW

NOTES

1: CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2: PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3: SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.

BALL PITCH e = 0.75				
D	E	N	D1	E1
8.0	6.0	48	5.25	3.75

D±0.1
D1
e
E1
E±0.1
VIEW A



VIEW A

TOP VIEW

36 mini-BGA (6 x 8mm)

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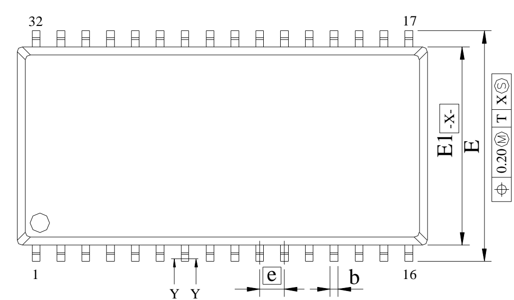
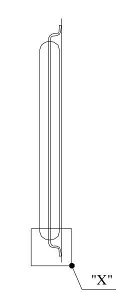
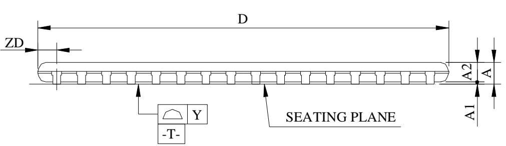
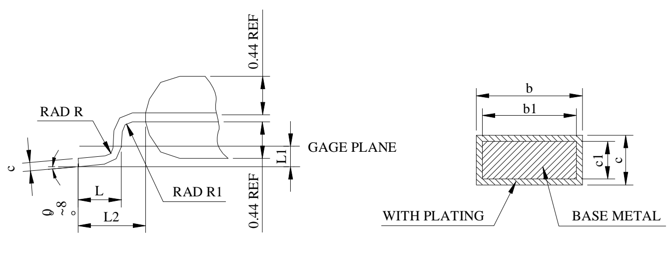
n PACKAGE DIMENSIONS (continued)







SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.30		0.52	0.012		0.020
b1	0.30	0.40	0.45	0.012	0.016	0.018
c	0.12		0.21	0.005		0.008
c1	0.10	0.127	0.16	0.004	0.005	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
e	1.27 BASIC			0.050 BASIC		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.25 BASIC			0.010 BASIC		
L2	0.8 REF			0.031 REF		
R	0.12		0.25	0.005		0.010
R1	0.12			0.005		
ZD	0.95 REF			0.037 REF		
Y			0.10			0.004



DETAIL "X"

SECTION Y-Y

NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS.
2. REFREENCE DOCUMENT : JEDEC MS-024
3. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.15(0.006") PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25(0.01") PER SIDE.
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.

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■ Revision History

Revision No.	History	Draft Date	Remark
1.0	Initial Production Version	Dec. 21,2005	Initial
1.1	Change I-grade operation temperature range - from –25°C to –40°C	May. 25, 2006	
1.2	To Add 600 mil PDIP package type To Add 400 mil TSOP-II package type To Add 36-ball BGA package type To Improve Icc spec. - from 12mA to 10mA	Aug. 08, 2006	

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