BH95640

64K-Bit SPI Serial CMOS E²PROM

FEATURES

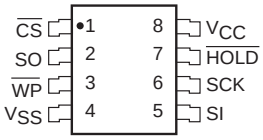
- **5 MHz SPI Compatible**
- **2.7 to 5.0 Volt Operation**
- **Hardware and Software Protection**
- **Zero Standby Current**
- **Low Power CMOS Technology**
- **SPI Modes (0,0 &1,1)**
- **Commercial, Industrial Temperature Ranges**
- **1,000,000 Program/Erase Cycles**
- **100 Year Data Retention**
- **Self-Timed Write Cycle**
- **8-Pin SOP TSSOP**
- **32-Byte Page Write Buffer**
- **Block Write Protection**
  – Protect 1/4, 1/2 or all of E²PROM Array

DESCRIPTION

The BH95640 is a 64K-Bit SPI Serial CMOS E²PROM internally organized as 8Kx8 bits. reduces device power requirements. The BH95640 features a 32-byte page write buffer. The device operates via the SPI bus serial interface and is enabled though a Chip Select ($\overline{CS}$). In addition to the Chip Select, the clock input (SCK), data in (SI) and data out (SO) are required to access the device. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence. The BH95640 is designed with software and hardware write protection features including Block write protection. The device is available in 8-pin SOP TSSOP.

PIN CONFIGURATION

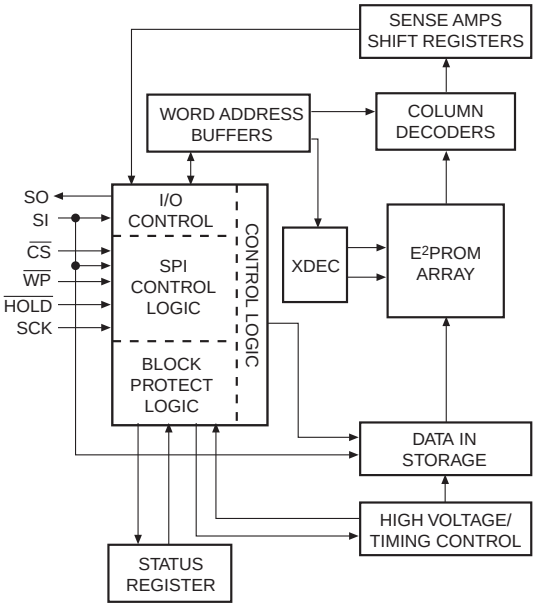
SOP Package **TSSOP Package**



PIN FUNCTIONS

Pin Name	Function
SO	Serial Data Output
SCK	Serial Clock
$\overline{WP}$	Write Protect
V_{CC}	+2.5V to +5.5V Power Supply
V_{SS}	Ground
$\overline{CS}$	Chip Select
SI	Serial Data Input
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... –20°C to +80 °C

Storage Temperature ..... –65°C to +150°C

Voltage on any Pin with Respect to V_{SS} ..... –2.0V to +V_{CC} +2.0V

V_{CC} with Respect to V_{SS} ..... –2.0V to +7.0V

Package Power Dissipation Capability (Ta = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current ..... 100 mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

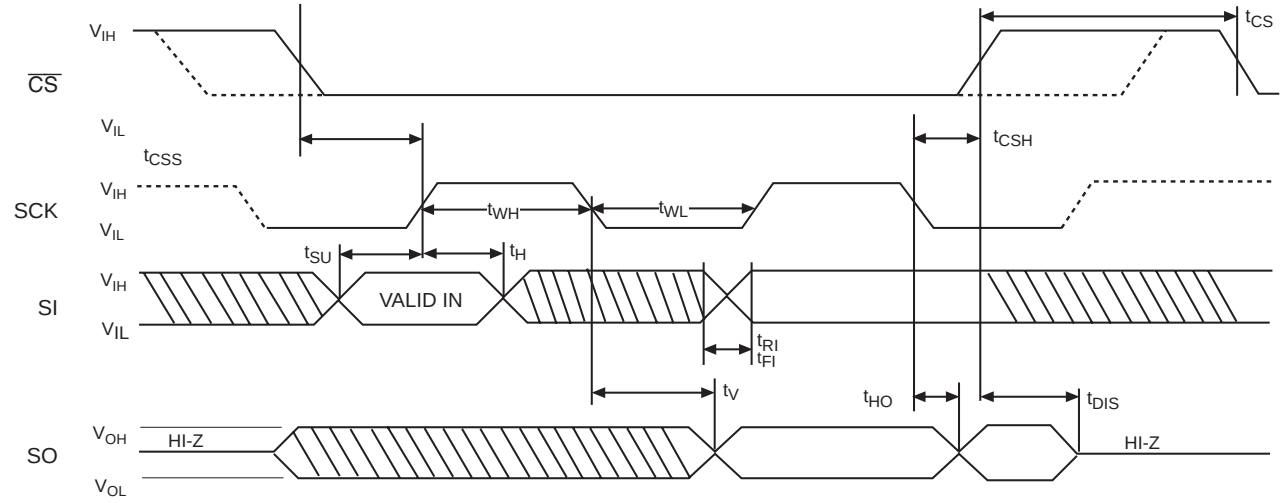
	Parameter	Min.	Max.	Units	Reference Test Method
	Endurance	1,000,000		Cycles/Byte	
	Data Retention	100		Years	
	ESD Susceptibility	2000		Volts	
	Latch-Up	100		mA	

D.C. OPERATING CHARACTERISTICS

V_{CC} = +1.8V to +6.0V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.	Max.		
I_{CC1}	Power Supply Current (Operating Write)			10	mA	V_{CC} = 5V @ 10MHz SO=open; CS=Vss
I_{CC2}	Power Supply Current (Operating Read)			2	mA	V_{CC} = 5.0V F_{CLK} = 10MHz
I_{SB}	Power Supply Current (Standby)			0	µA	$\overline{CS}$ = V_{CC} V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current			2	µA	
I_{LO}	Output Leakage Current			3	µA	V_{OUT} = 0V to V_{CC}, CS = 0V
V_{IL}	Input Low Voltage	-1		V_{CC} x 0.3	V	
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output Low Voltage			0.4	V	4.5V≤V_{CC}<5.5V I_{OL} = 3.0mA I_{OH} = -1.6mA
V_{OH1}	Output High Voltage	V_{CC} - 0.8			V	
V_{OL2}	Output Low Voltage			0.2	V	1.8V≤V_{CC}<2.7V I_{OL} = 150µA I_{OH} = -100µA
V_{OH2}	Output High Voltage	V_{CC}-0.2			V	

Figure 1. Sychronous Data Timing



Note: Dashed Line= mode (1, 1) — — — —

A.C. CHARACTERISTICS

		Limits							
		Vcc= 2.5V-3.3V		V_{CC} = 2.5V-5.5V		V_{CC} = 4.5V-5.5V			Test
SYMBOL	PARAMETER	Min.	Max.	Min.	Max.	Min.	Max.	UNITS	Conditions
t_{SU}	Data Setup Time	50		50		20		ns	
t_H	Data Hold Time	50		50		20		ns	
t_{WH}	SCK High Time	250		125		40		ns	
t_{WL}	SCK Low Time	250		125		40		ns	
f_{SCK}	Clock Frequency	DC	1	DC	3	DC	10	MHz	
t_{LZ}	$\overline{HOLD}$ to Output Low Z		50		50		50	ns	
t_{RI}	Input Rise Time		2		2		2	µs	
t_{FI}(1)	Input Fall Time		2		2		2	µs	C_L = 50pF
t_{HD}	$\overline{HOLD}$ Setup Time	100		100		40		ns	
t_{CD}	$\overline{HOLD}$ Hold Time	100		100		40		ns	
t_{WC}	Write Cycle Time		10		10		5	ms	
t_V	Output Valid from Clock Low		250		250		80	ns	
t_{HO}	Output Hold Time	0		0		0		ns	
t_{DIS}	Output Disable Time		250		250		75	ns	
t_{HZ}	$\overline{HOLD}$ to Output High Z		150		100		50	ns	
t_{CS}	$\overline{CS}$ High Time	500		250		200		ns	
t_{CSS}	$\overline{CS}$ Setup Time	500		250		100		ns	
t_{CSH}	$\overline{CS}$ Hold Time	500		250		100		ns	

FUNCTIONAL DESCRIPTION

The BH95640 supports the SPI bus data transmission protocol. The synchronous Serial Peripheral Interface (SPI) helps the BH95640 to interface directly with many of today's popular microcontrollers. The BH95640 contains an 8-bit instruction register. (The instruction set and the operation codes are detailed in the instruction set table)

After the device is selected with $\overline{CS}$ going low, the first byte will be received. The part is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The first byte contains one of the six op-codes that define the operation to be performed.

PIN DESCRIPTION

SI: Serial Input
SI is the serial data input pin. This pin is used to input all opcodes, byte addresses, and data to be written to the BH95640. Input data is latched on the rising edge of the serial clock.

SO: Serial Output
SO is the serial data output pin. This pin is used to transfer data out of the BH95640. During a read cycle, data is shifted out on the falling edge of the serial clock.

SCK: Serial Clock
SCK is the serial clock pin. This pin is used to synchronize the communication between the microcontroller and the BH95640. Opcodes, byte addresses, or data present on the SI pin are latched on the rising edge of the SCK. Data on the SO pin is updated on the falling edge of the SCK.

$\overline{CS}$: Chip Select

$\overline{CS}$ is the Chip select pin. $\overline{CS}$ low enables the BH95640 and $\overline{CS}$ high disables the BH95640. $\overline{CS}$ high takes the SO output pin to high impedance and forces the devices into a Standby Mode (unless an internal write operation is underway). The BH95640 draws ZERO current in the Standby mode. A high to low transition on $\overline{CS}$ is required prior to any sequence being initiated. A low to high transition on $\overline{CS}$ after a valid write sequence is what initiates an internal write cycle.

$\overline{WP}$: Write Protect
$\overline{WP}$ is the Write Protect pin. The Write Protect pin will allow normal read/write operations when held high. When $\overline{WP}$ is tied low and the WPEN bit in the status register is set to "1", all write operations to the status register are inhibited. $\overline{WP}$ going low while $\overline{CS}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no effect on any write operation to the status register. The $\overline{WP}$ pin function is blocked when the WPEN bit is set to 0.

$\overline{HOLD}$: Hold
The $\overline{HOLD}$ pin is used to pause transmission to the BH95640 while in the middle of a serial sequence without having to re-transmit entire sequence at a later time. To pause, $\overline{HOLD}$ must be brought low while SCK is low. The SO pin is in a high impedance state during the time the part is paused, and transitions on the SI pins will be ignored. To resume communication, $\overline{HOLD}$ is brought high, while SCK is low. ($\overline{HOLD}$ should be held high any time this function is not being used.) $\overline{HOLD}$ may be tied high directly to V_{cc} or tied to V_{cc} through a resistor.

INSTRUCTION SET

Instruction	Opcode	Operation
WREN	0000 0110	Enable Write Operations
WRDI	0000 0100	Disable Write Operations
RDSR	0000 0101	Read Status Register
WRSR	0000 0001	Write Status Register
READ	0000 0011	Read Data from Memory
WRITE	0000 0010	Write Data to Memory

DEVICE OPERATION

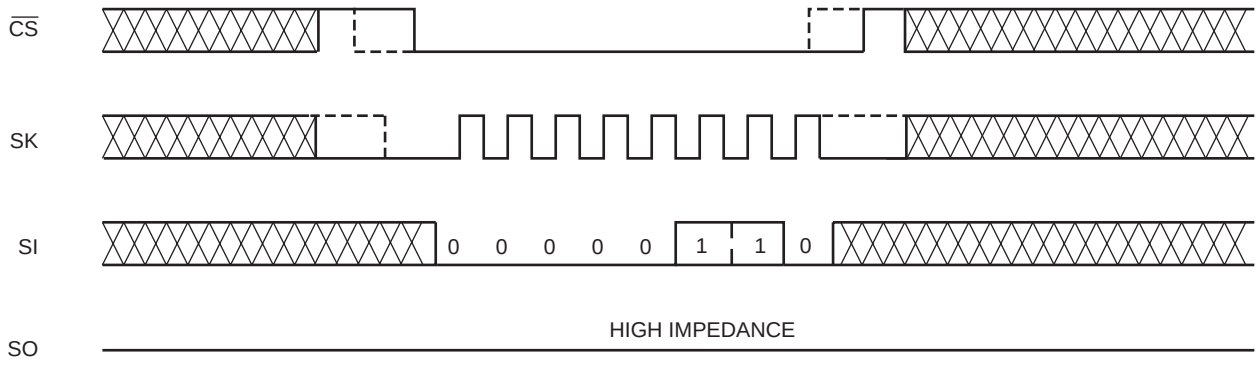
Write Enable and Disable

The BH95640 contains a write enable latch. This latch must be set before any write operation. The device powers up in a write disable state when V_{CC} is applied. WREN instruction will enable writes (set the latch) to the device. WRDI instruction will disable writes (reset the latch) to the device. Disabling writes will protect the device against inadvertent writes.

READ Sequence

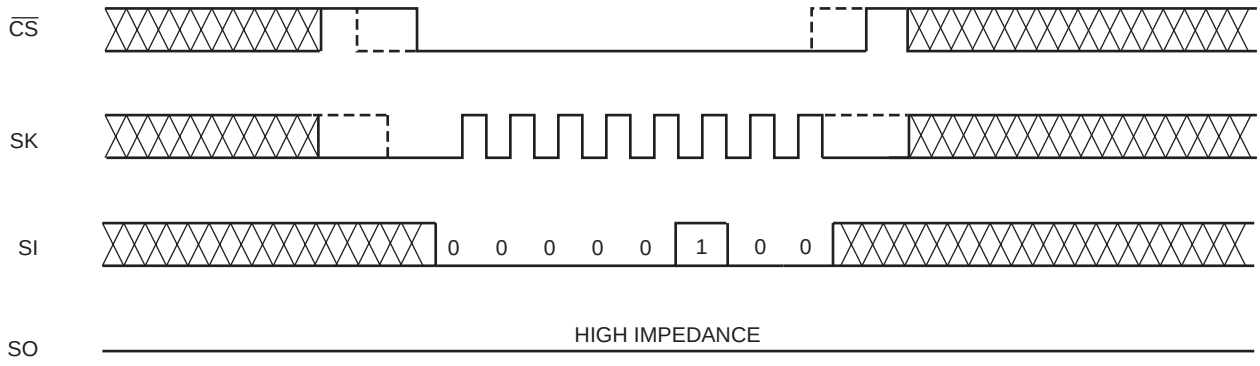
The part is selected by pulling $\overline{CS}$ low. The 8-bit read instruction is transmitted to the BH95640, followed by the 16-bit address

Figure 2. WREN Instruction Timing



Note: Dashed Line= mode (1, 1) — — — —

Figure 3. WRDI Instruction Timing



Note: Dashed Line= mode (1, 1) — — — —

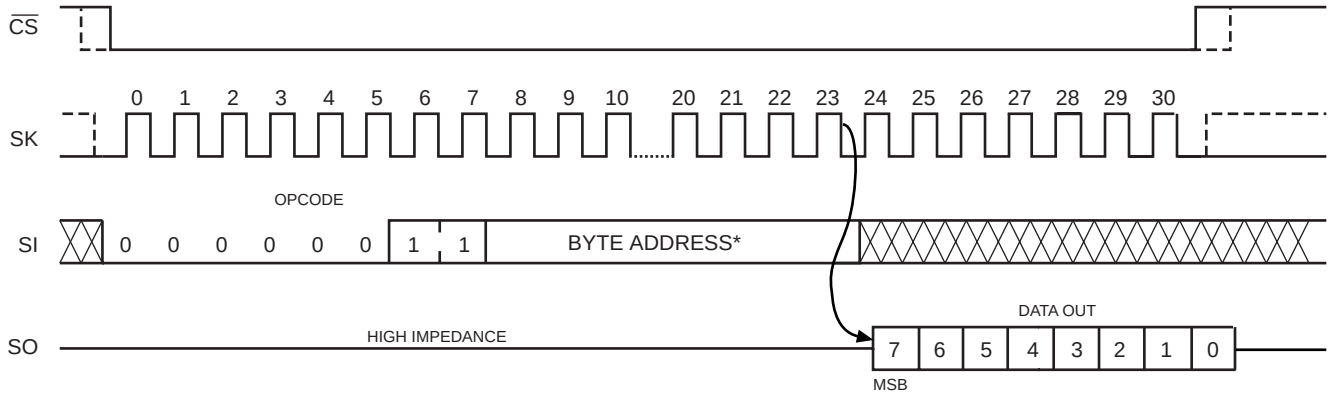
WRITE Sequence

The BH95640 powers up in a Write Disable state. Prior to any write instructions, the WREN instruction must be sent to BH95640. The device goes into Write enable state by pulling the $\overline{CS}$ low and then clocking the WREN instruction into BH95640. The $\overline{CS}$ must be brought high after the WREN instruction to enable writes to the device. If the write operation is initiated immediately after the WREN instruction without $\overline{CS}$ being brought high, the data will not be written to the array because the write enable latch will not have been properly set. Also, for a successful write operation the address of the memory location(s) to be programmed must be outside the protected address field location selected by the block protection level.

Byte Write

Once the device is in a Write Enable state, the user may proceed with a write sequence by setting the $\overline{CS}$ low, issuing a write instruction via the SI line, followed by the 16-bit address and then the data to be written. Programming will start after the $\overline{CS}$ is brought high. Figure 6 illustrates byte write sequence.

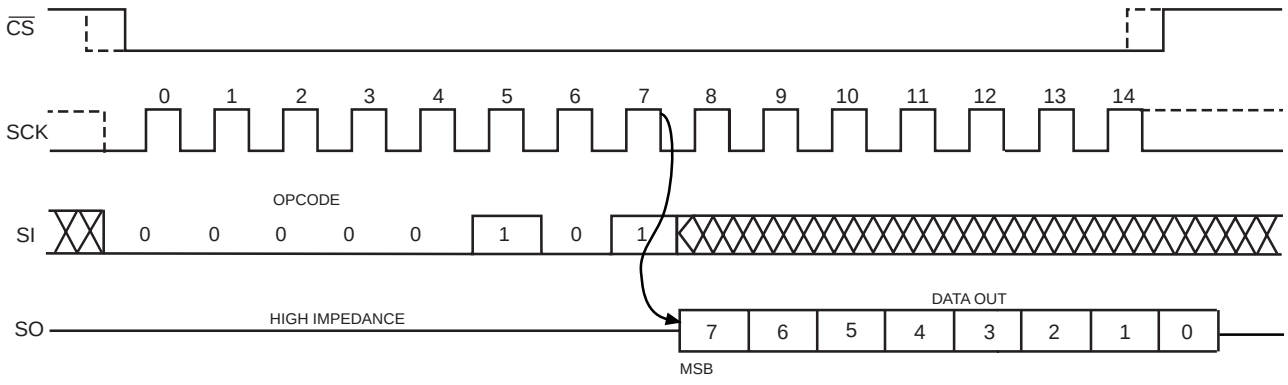
Figure 4. Read Instruction Timing



*Please check the instruction set table for address

Note: Dashed Line= mode (1, 1) — — — —

Figure 5. RDSR Instruction Timing



Note: Dashed Line= mode (1, 1) — — — —

During an internal write cycle, all commands will be ignored except the RDSR (Read Status Register) instruction.

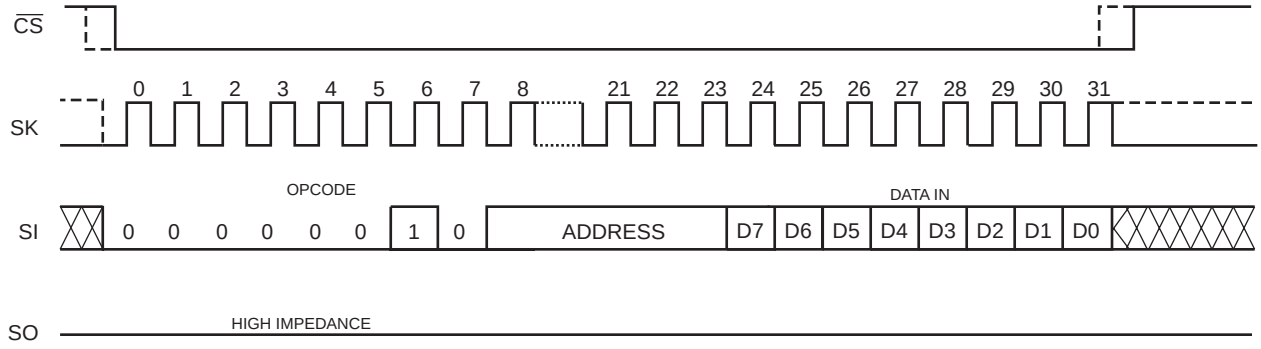
The Status Register can be read to determine if the write cycle is still in progress. If Bit 0 of the Status Register is set at 1, write cycle is in progress. If Bit 0 is set at 0, the device is ready for the next instruction.

Page Write

The BH95640 features page write capability. After the first initial byte the host may continue to write up to 32 bytes of data to the BH95640. After each byte of data is received, six lower order address bits are internally incremented by one; the high order bits of address will remain constant. The only restriction is that the 32 bytes must reside on the same page. If the address counter reaches the end of the page and clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been written. The BH95640 is automatically returned to the write disable state at the completion of the write cycle.

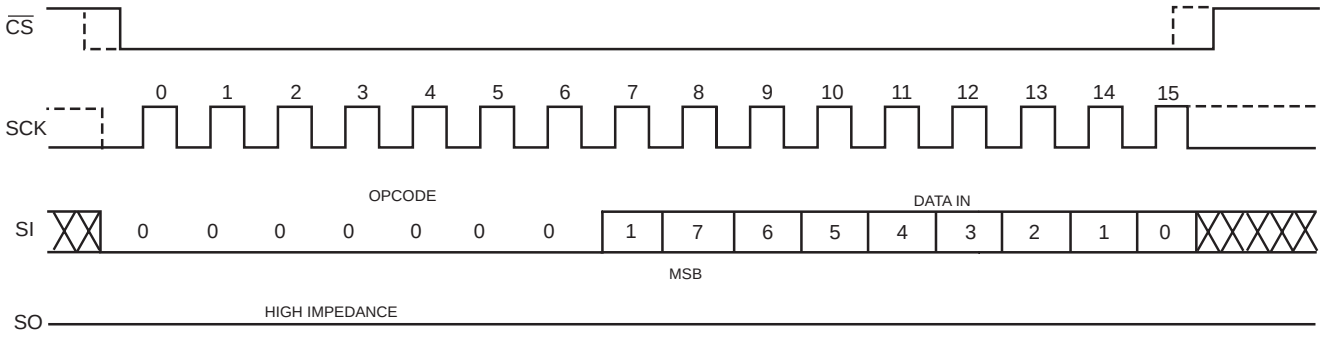
To write to the status register, the WRSR instruction should be sent. Only Bit 2, Bit 3 and Bit 7 of the status register can be written using the WRSR instruction. Figure 7 illustrates the sequence of writing to status register.

Figure 6. Write Instruction Timing



Note: Dashed Line= mode (1, 1) – – – –

Figure 7. WRSR Instruction Timing



Note: Dashed Line= mode (1, 1) — — — —