Data Sheet

BIT1605

10-Bit Digital Video Decoder

Version: A5

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Figure

1 General Description

BIT1605是一個10位元的影像輸入處理器，內含2個通道的類比訊號處理電路，包括AFE、路徑控制和2D梳型濾波器、自動箝位和訊號放大控制、PLL電路、一個數字式多重標準視訊解碼器(PAL BDGHI，PAL M，PAL N，PAL 60，NTSC M，NTSC Japan，NTSC 4.43和SECAM BDGKL，SECAM K1)，亮度、對比度和飽和度控制電路，及多重標準的VBI數據分離器。

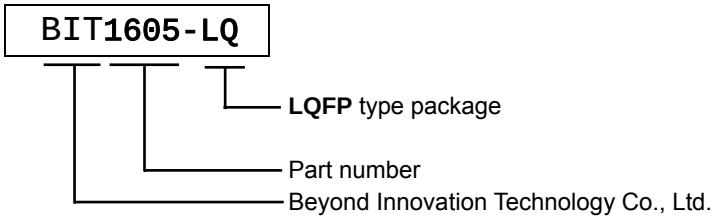
BIT1605是一個適用於消費性視訊解碼器的高度集成積體電路，用精確的1.8 V/3.3V作爲core及AFE CMOS電路之電源。 解碼器的設計基於線性鎖定的時脈信號解碼並且能解碼PAL、SECAM和NTSC的色彩信號，成爲CCIR-656標準的色彩元件資料。 BIT1605接受所有類比輸入CVBS或S-video(Y/C)之影像來源。

本積體電路是受控於TWSI (雙線式串列介面)匯流排。 高性能多重標準的VBI數據分離器支援多種VBI數據標準。

2 Features

- Three analog inputs, internal analog source selectors, e.g. 3 × CVBS or 1 × Y/C or (1 × Y/C and 1 × CVBS)
- Two 10-bit video CMOS Analog-to-Digital Converters (ADCs) in differential CMOS style for best S/N-performance
- Fully programmable static gain or automatic gain control (AGC) for selected CVBS or Y/C channel : 0~12db(Analog) and 0~18db(Digital)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- On-chip clock generator
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources, e.g. consumer grade VTR
- Requires only one crystal (24.576 MHz) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Accepts NTSC (J, M, 4.43), PAL (60, B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video signal
- User programmable luminance peaking or aperture correction
- Adaptive 3/5-line comb filter for two dimensional chrominance/luminance separation
- PAL delay line for correcting PAL phase errors
- Brightness, Contrast, Saturation (BCS) and Hue control on-chip
- Four multi functional real-time output pins controlled by TWSI bus
- Multi-standard VBI-data slicer including closed caption.
- MV copy protection detection
- Standard ITU 656 YUV 4 : 2 : 2 format (8-bit) on output bus
- TWSI controlled (full read-back ability) by an external controller, bit rate up to 400 kbits/s
- Auto blank screen when signal un-lock
- Built-in 4 types (Pure color, Ramp, Grid and Color Bar) TV pattern
- User programmable sharpness filter
- FIFO for DVR Application
- User programmable U/V Gain and CTI function
- Pin options at power-on reset stage
- Low power consumption and low operating voltage design (1.8V / 3.3V)
- Small package (LQFP48)
- 5 V tolerance digital I/O ports

3 Order Information



4 Block Diagram

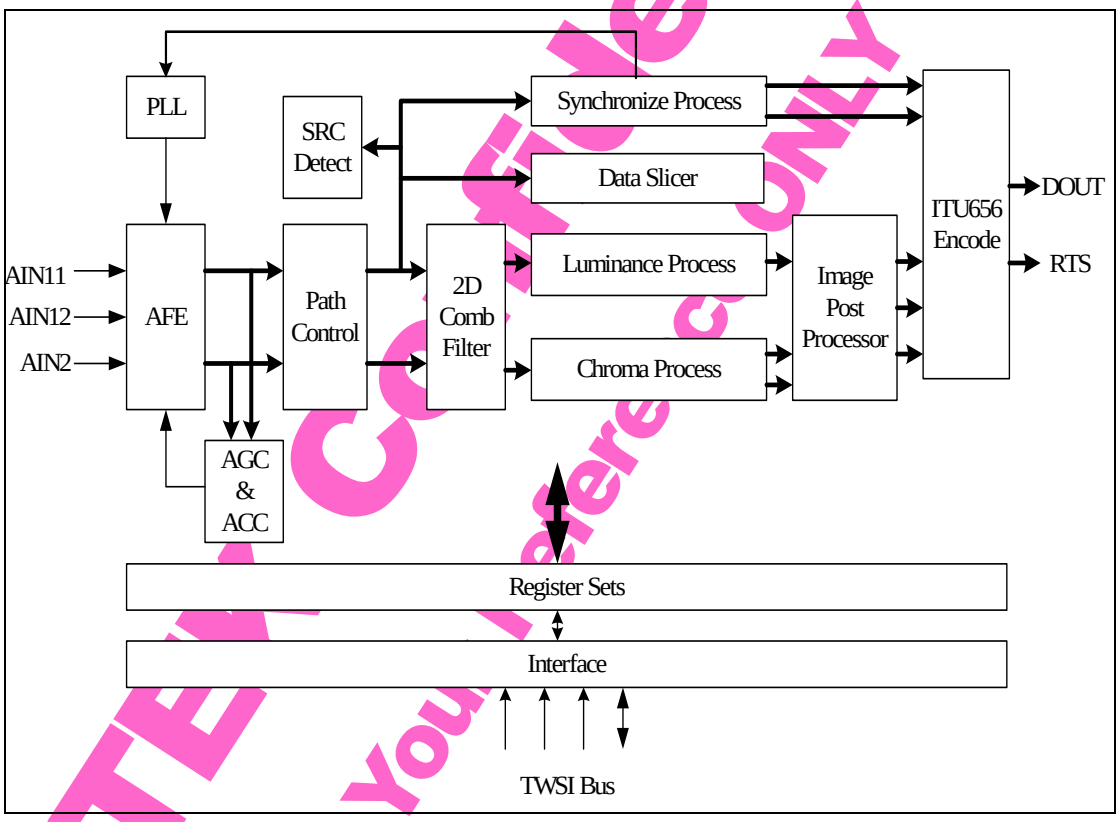


Figure 4-1 BIT1605 Architecture

5 Pin Definition

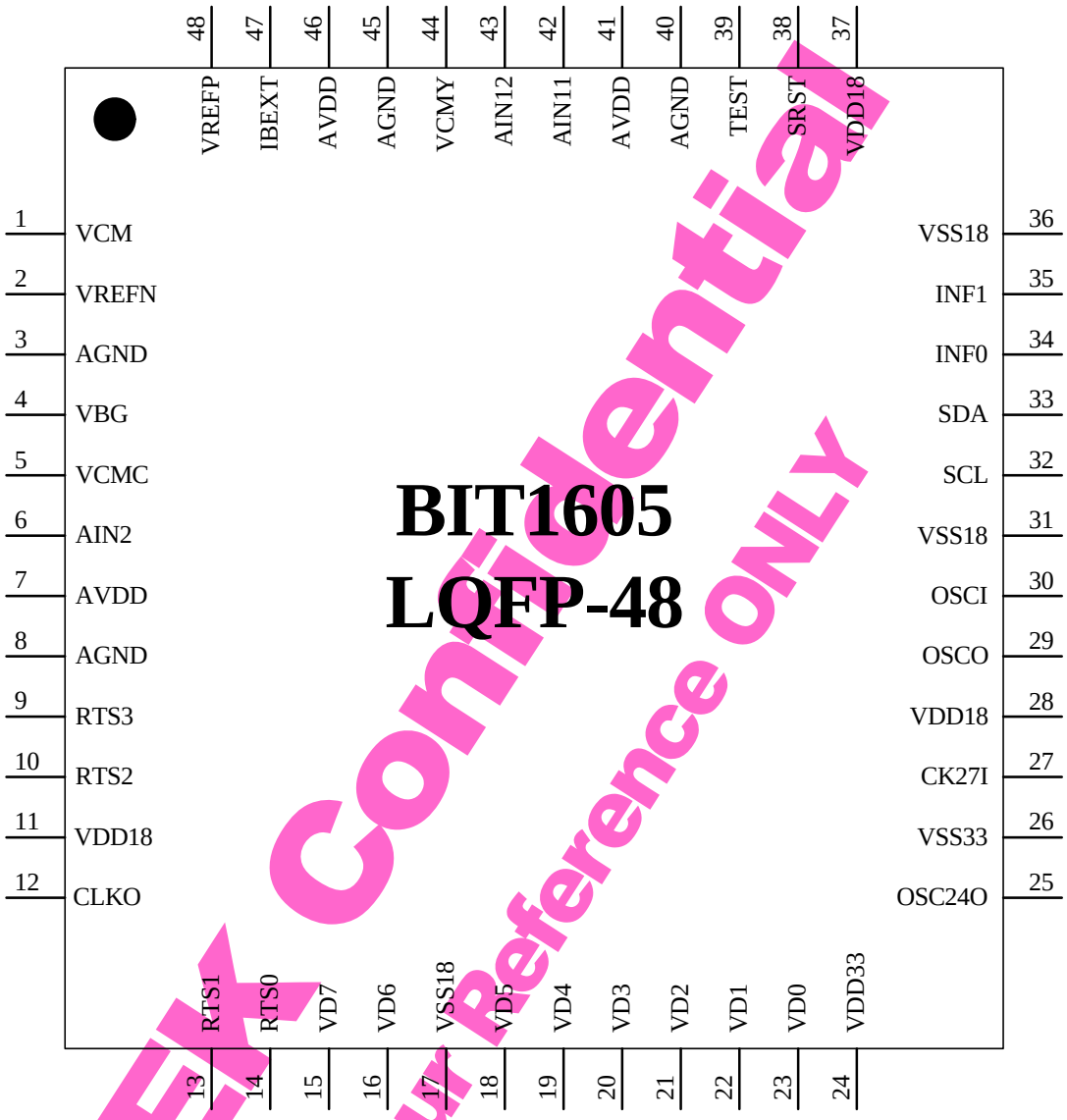


Figure 5-1 Pin configuration

Table 5-1 BIT1605 PIN Definition

Pin #	Pin Name	Pin Type	Function Description
1	VCM	AIN/AOUT	Output for decoupling or bypass Common Mode Voltage
2	VREFN	AIN/AOUT	Output for decoupling or bypass of Negative Internal Reference Voltages
3	AGND	AGND	AFE Power Ground
4	VBG	AIN/AOUT	Output for decoupling or bypass of Bandgap Voltage
5	VCMC	AIN	ADC2 Channel PGA negative reference input
6	AIN2	AIN	ADC2 Channel Analog input
7	AVDD	AVDD	AFE Power Supply (3.3V)
8	AGND	AGND	AFE Power Ground
9	RTS3	I/O	Real Time Signal 3 Output / Option 1 input Pull-Up
10	RTS2	I/O	Real Time Signal 2 Output / Option 0 input Pull-Up
11	VDD18	VDD18	Core Power Supply (1.8V)

12	CLKO	O	Clock Output	
13	RTS1	O	Real Time Signal 1 Output	
14	RTS0	O	Real Time Signal 0 Output	
15	VD7	O	Video Data Output Port [7]	
16	VD6	O	Video Data Output Port [6]	
17	VSS18	VSS18	Core Power ground	
18	VD5	O	Video Data Output Port [5]	
19	VD4	O	Video Data Output Port [4]	
20	VD3	O	Video Data Output Port [3]	
21	VD2	O	Video Data Output Port [2]	
22	VD1	O	Video Data Output Port [1]	
23	VD0	O	Video Data Output Port [0]	
24	VDD33	VDD33	I/O Power Supply (3.3V)	
25	OSC24O	O	24.576MHz Clock Output	
26	VSS33	VSS33	I/O Power Ground	
27	CLK27I	I	FIFO Mode Output Clock Input	
28	VDD18	VDD18	Core Power Supply (1.8V)	
29	OSCO	O	Crystal Oscillator Output	
30	OSCI	I	Crystal Oscillator Input	
31	VSS18	VSS18	Core Power Ground	
32	SCL	I	TWSI SCL	
33	SDA	I/O	TWSI SDA	
34	INF0	I	TWSI Slave Address Select 0	Pull-Up
35	INF1	I	TWSI Slave Address Select 1	Pull-Up
36	VSS18	VSS18	Core Power Ground	
37	VDD18	VDD18	Core Power Supply (1.8V)	
38	SRST	I	Reset / Chip Enable (Low Reset)	Pull-Up
39	TEST	I	Test Mode Enable (High Enable)	Pull-Down
40	AGND	AGND	AFE Power Ground	
41	AVDD	AVDD	AFE Power Supply (3.3V)	
42	AIN11	AIN	ADC1 Channel Analog Input 1	
43	AIN12	AIN	ADC1 Channel Analog Input 2	
44	VCMY	AIN	ADC1 Channel PGA Negative Reference Input	
45	AGND	AGND	AFE Power Ground	
46	AVDD	AVDD	AFE Power Supply (3.3V)	
47	IBEXT	AIN/AOUT	Monitoring or External bypass of Bias Current	
48	VREFP	AIN/AOUT	Output for decoupling or bypass of Positive Internal Reference Voltages	

6 Functional Description

6.1 Version Control

BIT1605 內部提供硬體版本資訊及軟體版本資訊兩組Register作爲版本控管，相關Register請參考 **Table 6-1**。

Table 6-1 Version Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_HW_VER	0x00	R	8	[1:0] Product Version [4:2] Product Number [7:5] Product Group	0xD4
R_SW_VER	0x01	RW	8	Software Version Control	0x00

6.2 Interrupt Function

BIT1605 Interrupt Function提供INT Pin (Pin 14, Pin 13, Pin 10 和Pin 9)作爲Interrupt Trigger Output(請參考“Special Output Setup”小節的說明)，經由Register可設定爲Edge or Level trigger output 。當Level Trigger時並可設定爲High or Low Active，若爲Edge Trigger時則可設定爲Falling or Rising Active。其Interrupt架構採用三層架構(FLAG、ACK and MASK)，架構請參考 **Figure 6-1**。BIT1605 提供 8 個Interrupt Flags 和 12 個 Interrupt Sources請參考 **Table 6-2**，相關Register設定請參考 **Table 6-3**。

Table 6-2 Interrupt Source and Flags

Interrupt Source	Bit	Function	
R_HASSIG_FLAG	0	Active when Video Decoder locks selected source(see **Table 6-4**)	
R_NOSIG_FLAG	1	Active when Video Decoder un-locks selected source(see **Table 6-4**)	
R_MODE_FLAG	2	Active when input video mode change occurs.	
		R_INTFIDT_EN (0x05[5]) = 0	Disable
		R_INTFIDT_EN (0x05[5]) = 1	Enable
R_VSYNC_FLAG	3	Active when selected VSYNC falling edge occurs.	
		R_INT_VSPOL (0x05[6]) =0	VSYNC Normal
		R_INT_VSPOL (0x05[6]) =1	VSYNC Invert
R_ERROR_FLAG	4	FIFO Over or FIFO Under or CC or MV Detection(see **Table 6-4**)	
R_SRC_FLAG	5	Source Detection(AIN11 or AIN12 or AIN2, see **Table 6-4**)	
R_AGCRDY_FLAG	6	AGC1 or AGC2 or Standard is ready(see **Table 6-4**)	
R_AGCNORDY_FLAG	7	AGC1 or AGC2 or Standard is not ready(see **Table 6-4**)	

Table 6-3 Interrupt Controller Register

Mnemonic	Address	R/W	Bits	Description	Default
R_INT_FLAG	0x02[7:0]	R	8	Interrupt Flag 0: Nothing 1: Interrupt event occurs	-
R_INT_MASK	0x03[7:0]	RW	8	Interrupt MASK 0: Interrupt Mask Off (Enable interrupt) 1: Interrupt Mask On (Disable interrupt)	0x00
R_INT_ACK	0x04[7:0]	RW	8	Interrupt ACK 0: Clear Interrupt Flag and Disable Interrupt 1: Enable Interrupt	0x00
R_INT_TYPE	0x05[0]	RW	1	Interrupt TYPE 0: Level Type 1: Edge Type	0
R_POL_INT	0x05[1]	RW	1	Interrupt Polarity 0: High level active (Level Type) 0: Rising edge active (Edge type) 1: Low level active (Level Type) 1: Falling edge active (Edge type)	0

Table 6-4 Video Decoder Lock Source for Interrupt Select					
Mnemonic	Address	R/W	bit	Description	Default
R_INTSYNCRDY_EN, R_INTHLCK_EN	0x05[3:2]	RW	2	Lock source for interrupt select 00: Disable 01: From HLCK 10: From SYNC_READY 11: From SYNC_READY & HLCK	00
R_INTOVER_EN	0x06[1]	RW	1	FIFO overflow enable 0 : Disable 1 : Enable	0
R_INTUNDER_EN	0x06[0]	RW	1	FIFO underflow enable 0 : Disable 1 : Enable	0
R_INTCC_EN	0x06[7]	RW	1	CC (Closed Caption) detection enable 0 : Disable 1 : Enable	0
R_INTMV_EN	0x05[7]	RW	1	MV detection enable 0 : Disable 1 : Enable	0
R_INTSRC2_EN	0x06[4]	RW	1	SRC2 detection enable 0 : Disable 1 : Enable	0
R_INTSRC12_EN	0x06[5]	RW	1	SRC12 detection enable 0 : Disable 1 : Enable	0
R_INTSRC11_EN	0x06[6]	RW	1	SRC11 detection enable 0 : Disable 1 : Enable	0
R_INTAGC1_EN	0x06[2]	RW	1	AGC1 ready enable 0 : Disable 1 : Enable	0
R_INTAGC2_EN	0x06[3]	RW	1	AGC2 ready enable 0 : Disable 1 : Enable	0
R_INTSTDRDY_EN	0x05[4]	RW	1	Color standard ready enable 0 : Disable 1 : Enable	0

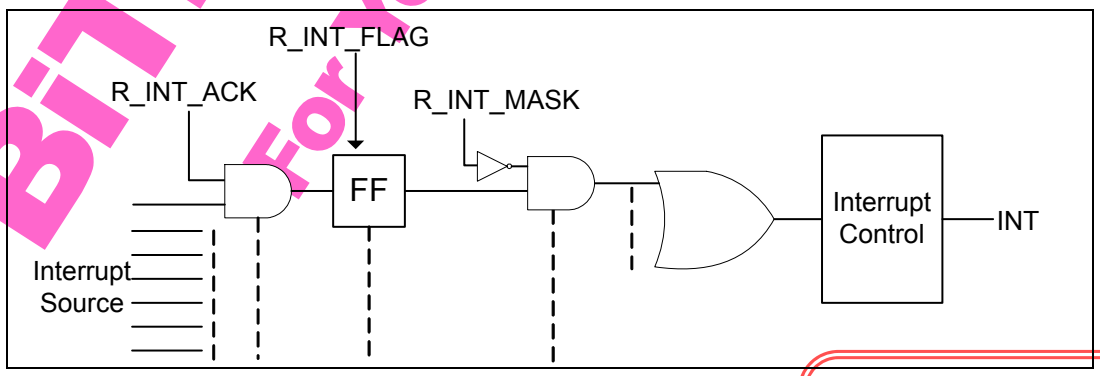


Figure 6-1 Interrupt Function Block

6.3 Pad Type Setup

BIT1605 在輸出的 PAD 可設定爲 Tri-State 輸出，在輸入的 PAD 尚可控制其內建之 Pull-Up 電阻導通或關閉相關 Register 設定請參考下表。

Table 6-5 Output Tri-State Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_RTS0_TRI	0x08[0]	RW	1	RTS0 pin Tri-State Enable	0
R_RTS1_TRI	0x08[1]	RW	1	RTS1 pin Tri-State Enable	0
R_RTS2_TRI	0x08[2]	RW	1	RTS2 pin Tri-State Enable	0
R_RTS3_TRI	0x08[3]	RW	1	RTS3 pin Tri-State Enable	0
R_DOUT_TRI	0x08[4]	RW	1	DOUT pin Tri-State Enable	0
R_OCLK_TRI	0x08[5]	RW	1	OCLK pin Tri-State Enable	0
R_OSC24_TRI	0x08[6]	RW	1	OSC24O pin Tri-State Enable	0
				0 : Normal	
				1 : Tri-State	

Table 6-6 Output Pull-up Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_RTS2_REN	0x07[6]	RW	1	RTS2 pin Pull-Up resistance on/off	1
R_RTS3_REN	0x07[7]	RW	1	RTS3 pin Pull-Up resistance on/off	1
				0:Turn on Pull-Up resistance	
				1: Turn off Pull-Up resistance	

6.4 Clock Domain System

BIT1605 內部存在六個 Clock Domain：

- AFECLK Domain: Source Clock
- DVPCLK Domain: Output Clock
- CLK27 Domain: System Clock
- OCLK Domain: Image Clock
- AFEBUF Domain: Panel Clock
- XCLK Domain: Image Clock

相關Register設定請參考 **Table 6-7**。

Table 6-7 Clock Domain System Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AFECLK_SEL	0x09[6]	RW	1	AFECLK Domain Clock Source Select	0
				0: From 27MHz	
				1: From 13.5MHz	
R_AFECLK_POL	0x09[7]	RW	1	AFECLK Domain Polarity	1
				0: Normal	
				1: Invert	
R_AFECLK_EN	0x0A[6]	RW	1	AFECLK Domain Enable	1
				0: Disable	
				1: Enable	
R_AFEBUF_SEL	0x09[4]	RW	1	AFEBUF Domain Clock Source Select	1
				0: From DVPCLK	
				1: From AFECLK	
R_AFEBUF_POL	0x09[5]	RW	1	AFEBUF Domain Polarity	1
				0: Normal	
				1: Invert	
R_DVPCLK_SEL	0x09[3]	RW	1	DVPCLK Domain Clock Source Select	0
				0: From PLL	
				1: From OSC	
R_DVPCLK_POL	0x09[2]	RW	1	DVPCLK Domain Polarity	1
				0: Normal	
				1: Invert	

R_DVPCLK_EN	0x0A[5]	RW	1	DVPCLK Domain Enable 0: Disable 1: Enable	1
R_CLK27_POL	0x09[0]	RW	1	CLK27 Domain Polarity 0: Normal 1: Invert	0
R_CLK27_EN	0x09[1]	RW	1	CLK27 Domain Enable 0: Disable 1: Enable	1
R_OCLK_SEL	0x0A[3:2]	RW	2	OCLK Domain Clock Source selection(FIFO output clock) 00: FIFO ICLK = OCLK 01: from DVPCLK/2 10: from CK27I(pin27 input clock) 11: from AFECLKI	00
R_OCLK_POL	0x0A[1]	RW	1	OCLK Domain Polarity 0: Normal 1: Invert	0
R_OCLK_EN	0x0A[4]	RW	1	OCLK Domain Enable 0: Disable 1: Enable	1
R_OCLK_PAD	0x0A[0]	RW	1	OCLK_PAD Clock Polarity 0: Normal 1: Invert	0
R_REGS_CKEN	0x0A[7]	RW	1	REG Clock Enable 0: Disable 1: Enable	1

6.5 System Reset and Boot Mode

6.5.1 System Reset

BIT1605 可以從外部 Reset PIN (Pin 38)輸入一個 Asynchronous Reset (Low Active)信號，BIT1605 將會在接受到此信號再等 4 個 Cycle 後設定 Boot Mode，並且在 32 Cycles 後重置 BIT1605 內部的狀態，重新設定爲所選擇的初始化模式。相關波形請參考下圖。

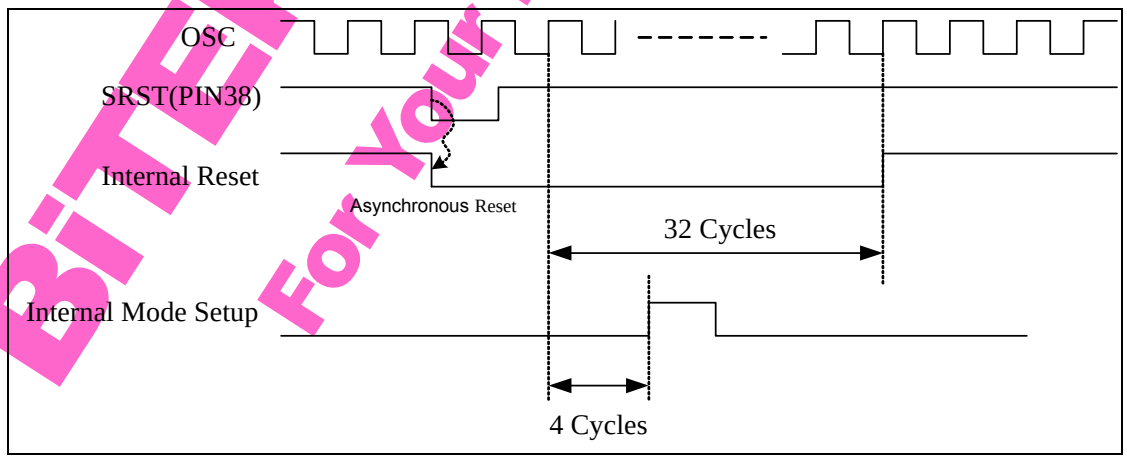


Figure 6-2 System Reset and Initial Mode Setup

6.5.2 Boot Modes

BIT1605 可經由外部 RTS3 (pin 9) 和 RTS2 (pin 10)兩 pin 來設定 Reset 後的工作模式，相關的模式定義請參考下表。

Table 6-8 Boot Mode

RTS3	RTS2	Mode
1	X	Tri-State Mode (output port in tri-state status)
0	1	Normal Y/C Mode Y signal input from AIN12 C signal input from AIN2
0	0	Normal CVBS Mode CVBS signal input from AIN11

Table 6-9 Power on reset Register Value

Register	Address	Tri-State Mode	CVBS Mode	Y/C Mode
R_RTS0_TRI	0x08[0]	1	0	0
R_RTS1_TRI	0x08[1]	1	0	0
R_RTS2_TRI	0x08[2]	1	0	0
R_RTS3_TRI	0x08[3]	1	0	0
R_DOUT_TRI	0x08[4]	1	0	0
R_OCLK_TRI	0x08[5]	1	0	0
R_CLK27_EN	0x09[1]	0	1	1
R_DVPCLK_EN	0x0A[5]	0	1	1
R_OCLK_EN	0x0A[4]	0	1	1
R_COMB_EN	0x0C[6]	~RTS3	1	0
R_CHT_EN	0x0C[5]	~RTS3	1	0
R_YC_EN	0x0C[3]	RTS3	0	1
R_AFE_SEL	0x0C[2]	RTS3	0	1
R_AFE_ENAC	0x5B[5]	0	1	1
R_AFE_ENAY	0x5B[4]	0	1	1
R_AFE_ENVCM	0x5B[3]	0	1	1
R_AFE_ENVBG	0x5B[2]	0	1	1
R_AFE_ENREF	0x5B[1]	0	1	1
R_AFE_ENIB	0x5B[0]	0	1	1
R_PLL_EAPLL	0x5C[1]	0	1	1

6.6 Input Path Select

BIT1605 Video Decoder內建兩組 10 Bits ADC，提供三組Analog信號輸入端，並可經由Register設定，以支援CVBS及Y/C的信號輸入，其相關架構示意圖請參考下圖，相關Register設定請參考 **Table 6-10** 及 **Table 6-11**。

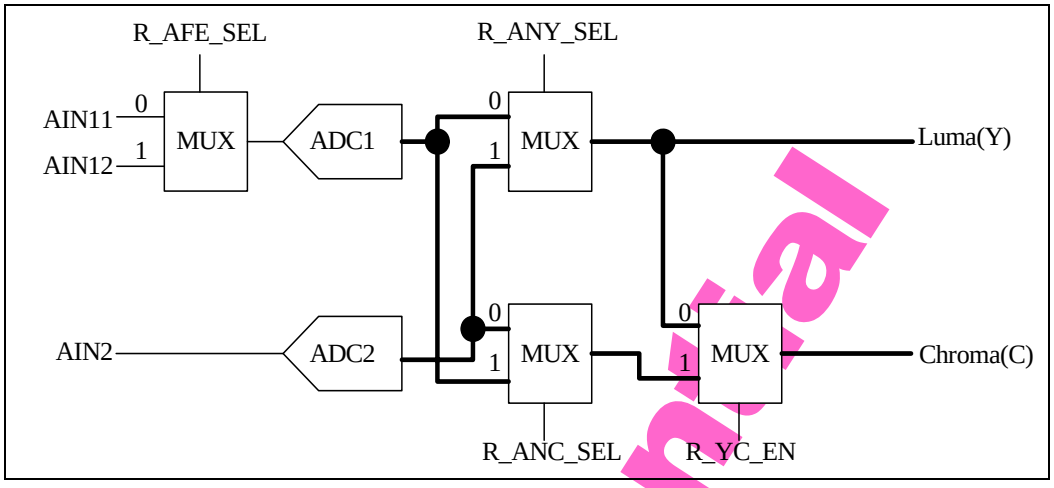


Figure 6-3 Input path

Table 6-10 Analog Input Path Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_ANC_SEL	0x0C[0]	RW	1	Chroma Path Select 0: Data source form ADC2 1: Data source from ADC1	0
R_ANY_SEL	0x0C[1]	RW	1	Luma Path Select 0: Data source from ADC1 1: Data source from ADC2	0
R_AFE_SEL	0x0C[2]	RW	1	Video mux switch for ADC1 0: ADC1 signal from AIN11 pin 1: ADC1 signal from AIN12 pin	0
R_YC_EN	0x0C[3]	RW	1	Y/C Mode Enable 0: Disable 1: Enable	0
(Reserved)	0x0C[4]	RW	1	Always fix to 0	0

Table 6-11 Analog Input Path Register				
Mode	R_ANC_SEL	R_ANY_SEL	R_AFE_SEL	R_YC_EN
CVBS Mode: Signal input from AIN11	0/1	0	0	0
CVBS Mode: Signal input from AIN12	0/1	0	1	0
CVBS Mode: Signal input from AIN2	0/1	1	0/1	0
Y/C Mode: Y signal input from AIN11 C signal input from AIN2	0	0	0	1
Y/C Mode: Y signal input from AIN12 C signal input from AIN2	0	0	1	1
Y/C Mode: Y signal input from AIN2 C signal input from AIN11	1	1	0	1
Y/C Mode: Y signal input from AIN2 C signal input from AIN12	1	1	1	1

6.7 Standard Setting and Detection

BIT1605 可以針對PAL、PAL60、PAL-N、SECAM、PAL-M、NTSC-443-50、NTSC-M、NTSC-443-60 和 Black & White 等Color Standard信號進行解碼，並提供自動、半自動和手動三種模式可供使用者依據其使用環境做設定。相關架構示意圖請參考下圖，相關Register設定請參考 **Table 6-12**.

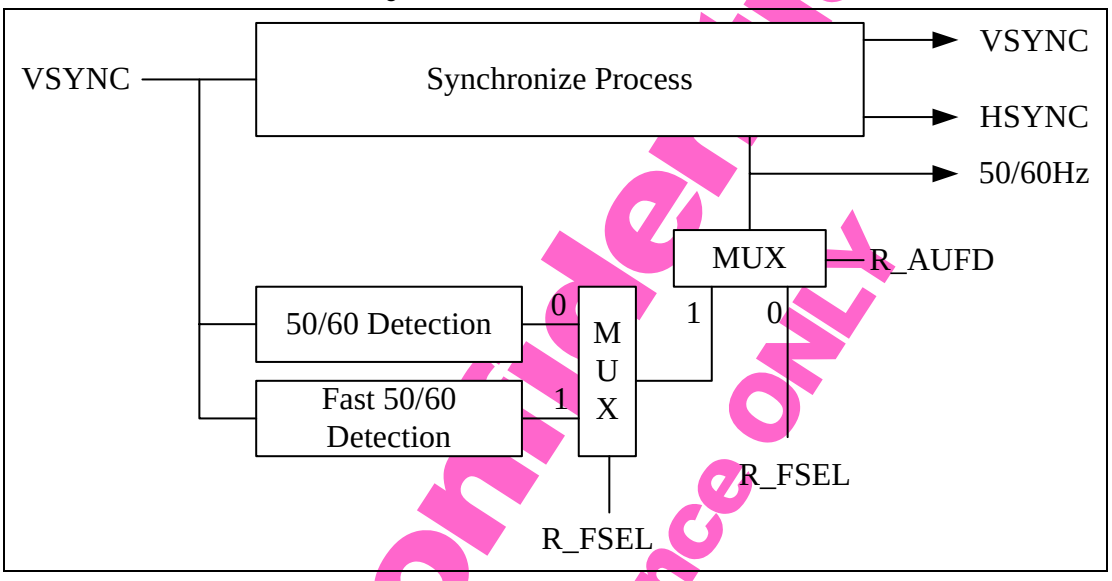


Figure 6-4 Field type select

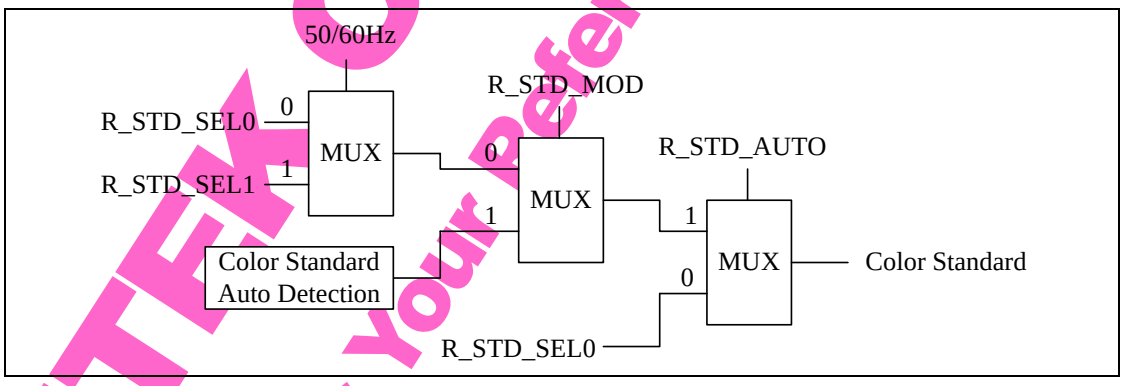


Figure 6-5 Color Standard select

Table 6-12 Standard Setting and Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUFD	0x0D[0]	RW	1	Auto 50/60Hz detect	
				0: Manual 50/60Hz (Defined on 0x0D[1])	0
				1: Auto 50/60Hz detection	
R_FSEL	0x0D[1]	RW	1	Manual 50/60Hz select (R_AUFD=0)	
				0: 50Hz	
				1: 60Hz	0
				Auto 50/60Hz Detect Mode select (R_AUFD=1)	
				0: Normal Mode	
				1: Fast Mode	
R_STD_AUTO	0x0D[2]	RW	1	Color Standard Detection	0

				0: Manual Color Standard (Defined on 0x0D[6:4])	
				1: Auto Color Standard	
R_STD_MOD	0x0D[3]	RW	1	Auto Color Standard Detect Mode Selection	0
				0: Semi-Auto mode	
				1: Fully-Auto mode	
R_STD_SEL0	0x0D[6:4]	RW	3	Color Standard Setup for Manual Setting and Semi-Auto on 50Hz	000
R_STD_SEL1	0x0E[2:0]	RW	3	Color Standard Setup for Semi-Auto on 60Hz	101
				000: PAL/PAL-60	
				001: PAL_N	
				010: SECAM	
				011: PAL_M	
				100: NTSC_4.43_50Hz	
				101: NTSC_M / NTSC_J	
				110: NTSC_4.43_60Hz	
				111: Black & White	

6.8 Image Adjustment

BIT1605 提供多樣的調整機制，使用者可依據需求針對影像作處理以得到最佳之顯示效果。相關架構請參考如下。

6.8.1 Brightness and Contrast

BIT1605 針對 Y Domain 做 Brightness 和 Contrast 的調整。其相對應設定如下所示：

Table 6-13 Color Adjustment Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BRIGHTNESS	0x10[7:0]	RW	8	Brightness Value	0x8A
R_CONTRAST	0x11[7:0]	RW	8	Contrast Value	0x71
R_BLACKLEVEL	0x12[7:0]	RW	8	Black Level Value	0x80

6.8.2 Sharpness Process

BIT1605 針對 Y Domain Data 提供 sharpness 處理可強化影像之銳利度，其相對應設定如下所示：

Table 6-14 Sharpness and Smoothness Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UNSHARP_VAL	0x13[6:0]	RW	7	Sharpness value (0~127) 0x00: Least sharpness 0x7F: Most sharpness	0x00
R_UNSHARP_EN	0x13[7]	RW	1	Sharpness Enable 0: Disable 1: Enable	0
R_UNSHARP_THD	0x14[5:0]	RW	6	Sharpness Threshold Value	0x00

6.8.3 UV Gain、Saturation and Kill Color Process

BIT1605 針對 UV Domain Data 提供 UV gain、Saturation、Hue 和 Kill Color 的處理，可讓使用者依喜好調到較佳的色彩影像，其相對應設定如下所示：

Table 6-15 UV Domain Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UGAIN	0x15[7:0]	RW	8	U Gain Value Adjustment	0x80
R_VGAIN	0x16[7:0]	RW	8	V Gain Value Adjustment	0x80
R_SAT_MODE	0x17[7]	RW	1	SAT Adjustment Control 0: Normal 1: Together Adjust R_SAT_U and R_SAT_V(From R_SAT_U)	1
R_SAT_U	0x17[6:0]	RW	7	U Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_SAT_V	0x18[6:0]	RW	7	V Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_CHROMA_HUE	0x19[7:0]	RW	8	Chrominance HUE control 01111111: +178.6° 0000000: 0° 1000000: -180°	0x00
R_KILL_COLOR	0x1A[7]	RW	1	Control Kill Color Enable 0: Disable 1: Enable	0
R_VDLY	0x1C[1:0]	RW	2	V Data Delay 00: Delay 0 01: Delay 1 10: Delay 2 11: Delay 3	01
R_UDLY	0x1C[3:2]	RW	2	U Data Delay 00: Delay 0 01: Delay 1	01

				10: Delay 2 11: Delay 3	

6.8.4 Chroma Transient Improvement (CTI)

BIT1605 提供 Chroma Transient Improvement(CTI)，相關Register請參考 **Table 6-16**。

Table 6-16 Chroma Transient Improvement Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CTI_THD	0x1B[7:0]	RW	8	CTI Process Threshold Value	0x10
R_CTI_EN	0x1A[0]	RW	1	CTI Enable 0: Disable 1: Enable	0
R_CTI_USEL	0x1A[3:1]	RW	3	CTI Level select for U domain 000: Least CTI enhancement 111: Most CTI enhancement	001
R_CTI_VSEL	0x1A[6:4]	RW	3	CTI Level select for V domain 000: Least CTI enhancement 111: Most CTI enhancement	001

6.9 Synchronization Process

Synchronization Process Block 將 Y/C 分離後的 Luminance 的信號分離解出 HSYNC 和 VSYNC 的信號。

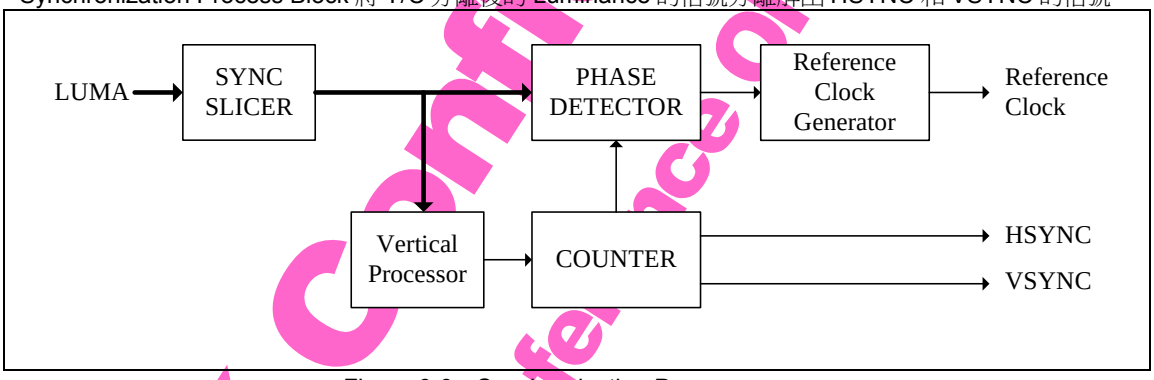


Figure 6-6 Synchronization Process

Table 6-17 Synchronization process Register

Mnemonic	Address	R/W	bit	Description	Default
R_SYNC_IDEL	0x1D[7:0]	RW	8	Horizontal increment delay	0x4A
R_SYNC_HSYS	0x1E[7:0]	RW	8	Horizontal Sync Start	0x2F
R_SYNC_HSYE	0x1F[7:0]	RW	8	Horizontal Sync End	0xFF
R_SYNC_HCS	0x20[7:0]	RW	8	Clamp Signal Start	0xF2
R_SYNC_HCE	0x21[7:0]	RW	8	Clamp Signal End	0xC0
R_SYNC_HSS	0x22[7:0]	RW	8	Horizontal Delay	0xFD
R_BGPU_POINT_N	0x23[7:0]	RW	8	Burst Start point for 60Hz Signal	0x06
R_BGPU_POINT_P	0x24[7:0]	RW	8	Burst Start point for 50Hz Signal	0x16
R_SLICER_THD	0x25[7:0]	RW	8	Sync-Slicer Threshold	0x00
R_VNOISE_MODE	0x26[1:0]	RW	2	VSYNC Noise Reduce Mode 00: Normal Mode 01: Fast Mode 10: Free-run Mode 11: Bypass Mode	01
R_FIDT_THD	0x26[7:4]	RW	4	50/60Hz Detection Threshold	1000
R_SYNC_LPADJ	0x27[1:0]	RW	2	Loop filter tracker speed	11
R_SYNC_PDGAIN	0x27[3:2]	RW	2	Loop filter Phase tracker factor	11
R_SYNC_LPLMT	0x27[4]	RW	1	Loop filter Phase adjustment speed	0
R_SYNC_HPLL	0x27[6:5]	RW	2	PLL Free-run Mode Enable 00: Free-run on 23.928MHz	00

				01: Disable (Normal)	
				10: Free-run on 27MHz	
				11: Free-run on 30.07MHz	
R_VTRC	0x27[7]	RW	1	VCR Mode Enable	0
				0: Disable	
				1: Enable	

6.10 VBI Data Slicer

BIT1605 提供 Data Slicer 功能可針對所設定的 Lines 及 Even/Odd，分離出 16 Bits 的 data 並且經由 Interrupt 及 Register 提供 MCU 做處理，相關的 Register 請參考下表。

Table 6-18 VBI Data Slice Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DATA_SLICER_THD	0x28[7:0]	RW	8	Data Slicer High/Low threshold	0x26
R_DATA_SLICER_START	0x29[7:0]	RW	8	Data Slicer start point	0x99
R_DATA_SLICER_LINE_E	0x2A[5:0]	RW	6	Data Slicer line select for even field	0x11
R_DATA_SLICER_EN_E	0x2A[7]	RW	1	Data Slicer enable for even field	1
				0: disable	
				0: enable	
R_DATA_SLICER_LINE_O	0x2B[5:0]	RW	6	Data Slicer line select for odd field	0x10
R_DATA_SLICER_EN_O	0x2B[7]	RW	1	Data Slicer enable for odd field	1
				0: disable	
				0: enable	
R_CC_DATA_SEL	0x7C[7]	RW	1	Data Slicer output (0x7D,0x7E) select	0
				0: Even Field	
				1: Odd Field	
R_CC_DATA1	0x7D[7:0]	R	8	Data Slicer First Byte	-
R_CC_DATA2	0x7E[7:0]	R	8	Data Slicer Second Bye	-

6.11 Source Detection

BIT1605 提供 Source Detection 的功能可以偵測 AIN11、AIN12 和 AIN2 哪一個輸入有信號的變化，偵測的結果將經由 Interrupt 提供系統使用，相關的 Register 設定請參考下表。

Table 6-19 Source Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CH2_THD	0x2C[1:0]	RW	2	Signal detection threshold for AIN2	00
R_CH12_THD	0x2C[3:2]	RW	2	Signal detection threshold for AIN12	00
R_CH11_THD	0x2C[5:4]	RW	2	Signal detection threshold for AIN11	00
R_SRCDET_MODE	0x2C[7]	RW	1	Source Detection Mode	0
				0: Disable (Normal Mode)	
				1: Source Detection Mode	
R_SRC2	0x7B[0]	R	1	Source detection result for AIN2	-
R_SRC12	0x7B[1]	R	1	Source detection result for AIN12	-
R_SRC11	0x7B[2]	R	1	Source detection result for AIN11	-
				0: No signal toggle	
				1: Signal toggle	

6.12 Luminance Process

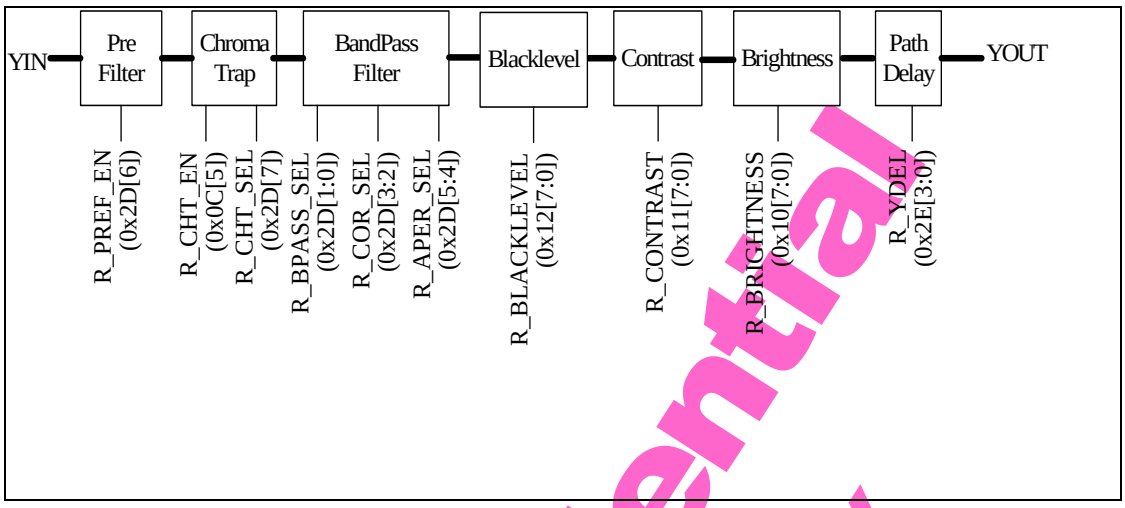


Figure 6-7 Luminance process block

Table 6-20 Luminance Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BPASS_SEL	0x2D[1:0]	RW	2	Band Pass Frequency Select	00
				00: Frequency 1	
				01: Frequency 2	
				10: Frequency 3	
				11: Frequency 4	
R_COR_SEL	0x2D[3:2]	RW	2	Coring Circuit Amplitude Value	00
				00: Coring factor 1	
				01: Coring factor 2	
				10: Coring factor 3	
				11: Coring factor 4	
R_APER_SEL	0x2D[5:4]	RW	2	Aperture Factor	00
				00: 0	
				01: 0.25	
				10: 0.5	
				11: 1.0	
R_CHT_EN	0x0C[5]	RW	1	Chroma Trap Enable	1
				0: Disable	
				1: Enable	
R_CHT_SEL	0x2D[7]	RW	1	Chroma-Trap Control (Internal Test)	1
				0: Type 1	
				1: Type 2	
R_PREF_EN	0x2D[6]	RW	1	Luma Pre-Filter Enable	0
				0: Disable	
				1: Enable	
R_YDEL	0x2E[3:0]	RW	4	Y Data Path Delay	1000
				1111: Delay 16 Clocks	
				1000: Delay 0 Clock	
				0000: Delay -15 Clocks	

6.13 Chroma Process

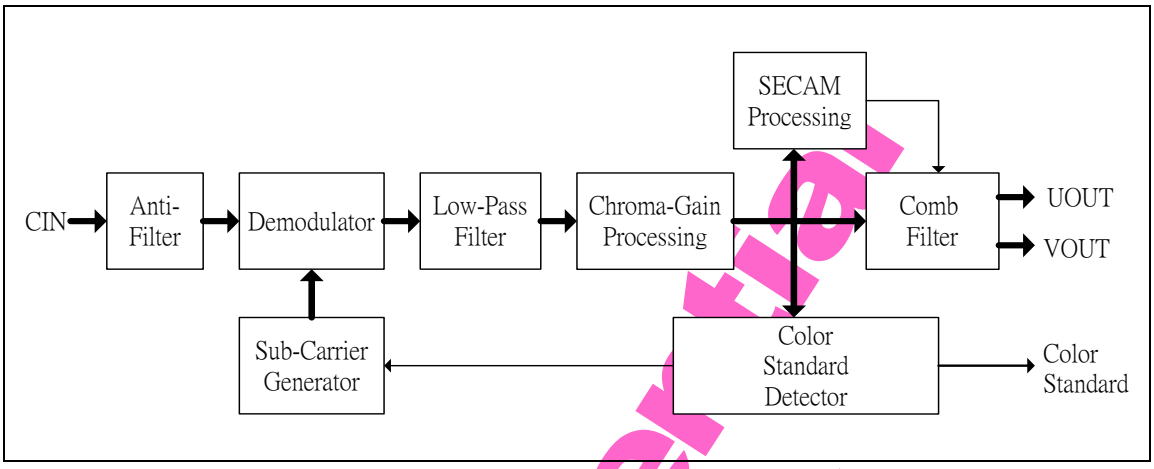


Figure 6-8 Chroma Process Function Block

Table 6-21 Chroma Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CHROMA_GAIN	0x30[6:0]	RW	7	Chroma Fixed-Gain Value 000000: Minimum gain (0.25) 010000: Normal gain (1.0) 111111: Maximum gain (3.5)	0x21
R_CHROMA_GAIN_SEL	0x30[7]	RW	1	Chroma Gain Type Select 0: Auto-Gain 1: Fixed-Gain (Defined on 0x30[6:0])	0
R_GAIN_CTL_VALUE	0x32[0], 0x31[7:0]	RW	9	Chroma Gain Reference value	0x100
R_CDV_SEL	0x32[2]	RW	1	TV / VCR Mode Select 0: Mode 1 1: Mode 2	0
R_CCIR_EN	0x32[3]	RW	1	CCIR Mode 0: Disable 1: Enable	0
R_GAIN_CTRL_SPEED	0x32[5:4]	RW	2	Auto Chroma Gain Loop Filter 00: Slow time constant 01: Medium time constant 10: Fast time constant 11: Frozen	00
R_SECAM_INVERT	0x32[6]	RW	1	SECAM Invert Enable 0: Disable 1: Enable	0
R_SXCR	0x32[7]	RW	1	SECAM Cross Color Reduction 0: Disable 1: Enable	1
R_THRESHOLD_SECAM	0x33[7:0]	RW	8	Color Killer Threshold for SECAM	0x80
R_THRESHOLD_QAM	0x34[7:0]	RW	8	Color Killer Threshold for PAL and NTSC	0x80
R_SECAM_SENSITIVE	0x35[7:0]	RW	8	SECAM Switch Sensitive Level	0x50
R_PAL_SENSITIVE	0x36[7:0]	RW	8	PAL Switch Sensitive Level	0x50
R_LOWER_BOUND	0x37[3:0]	RW	4	Color Standard Detection Threshold 1	0100
R_UPPER_BOUND	0x37[7:4]	RW	4	Color Standard Detection Threshold 2	1100
R_CHROMA_LPPI1	0x38[1:0]	RW	2	Chroma Low Pass Filter Factor 1	01
R_CHROMA_LPPI2	0x38[3:2]	RW	2	Chroma Low Pass Filter Factor 2	10
R_SQP_LMT	0x38 [4]	RW	1	Sub-Carrier Frequency Select 0: Type 1	0

				1: Type 2	
R_SQP_LPPI	0x38[6:5]	RW	2	Sub-Carrier Phase Detection Factor 1	01
R_SQP_SPUP	0x38[7]	RW	1	Sub-Carrier Phase Detection Factor 2	0
R_STD_COUNT	0x39[5:0]	RW	6	Color Standard Detection Ready Threshold	0x38
R_CHROMA_PHASE	0x39[6]	RW	1	Chroma Phase Detection Mode	0
				0: Mode 1	
				1: Mode 2	
R_STD_OFF00	0x3A[7:0]	RW	8	Burst Freq. offset for 3.57MHz	0x00
R_STD_OFF01	0x3B[7:0]	RW	8	Burst Freq. offset for 4.2MHz	0x08
R_STD_OFF10	0x3C[7:0]	RW	8	Burst Freq. offset for 4.43MHz	0x00

6.14 Comb Filter Process

BIT1605 Video Decoder 提供 NTSC 3-Line 和 PAL 5-Line 的 Adaptive Comb Filter 來做 Y/C 分離，其相關設定請參考下表。

Table 6-22 Comb filter process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_COMB_EN	0x0C[6]	RW	1	Comb Filter Enable	0
				0: Disable	
				1: Enable	
R_COMB_CTHD	0x3E[6:0]	RW	7	C Threshold Value	0x20
R_COMB_YTHD12	0x3F[7:0]	RW	8	Y Threshold Value for “NTSC: abs(line0-line1) or abs(line1-line2); PAL: abs(line0-line2) or abs(line2-line4)”	0x20
R_COMB_YTHD3	0x40[7:0]	RW	8	Y Threshold Value for “NTSC: abs(line0-line2) ; PAL: abs(line0-line4)”	0x10
R_LINE_THD1	0x41[7:0]	RW	8	Y Line Threshold 1 Value	0x10
R_LINE_THD2	0x42[7:0]	RW	8	Y Line Threshold 2 Value	0x0A
R_SECS_AUTOSW	0x43[0]	RW	1	SECAM Standard Control	1
				0: Force 1 D	
				1: Auto	
R_N44360_AUTOSW	0x43[1]	RW	1	NTSC_4.43MHz_60Hz Standard Control	1
				0: Force 1 D	
				1: Auto	
R_NOCOR_AUTOSW	0x43[2]	RW	1	No Color Burst Control	1
				0: Force 1 D	
				1: Auto	
R_OUT_SEL	0x43[5:4]	RW	2	Middle Filter Selection	00
				00: Mode 0	
				01: Mode 1	
				10: Mode 2	
				11: Mode 3	
R_Y_SEL	0x44[1:0]	RW	2	Y Domain force 1D Filter Selection (when R_Y_AUTO = 0)	00
				00: Notch filter	
				01: Two-line filter(mode 0)	
				10: Two-line filter(mode 1)	
				11: Three-line filter	
R_Y_AUTO	0x44[2]	RW	1	Y Domain Comb Filter Enable	1
				0: Fixed Filter	
				1: Adaptive Comb Filter	
R_Y1D_SEL	0x44[5:4]	RW	2	Y Domain Notch Filter Selection	00
				00: Type0	
				01: Type1	
				10: Type2	

				11: Type3	
R_CP90_SEL	0x45[2:0]	RW	3	C Domain force 1D Filter Selection (Phase 90)	010
				000:High pass filter	
				001: Two-line filter(mode 2)	
				01x: Two-line filter(mode 0)	
				10x: Two-line filter(mode 1)	
				11x : Three-line filter	
R_CP90_AUTO	0x45[3]	RW	1	C Domain Comb Filter Enable (Phase 90)	1
				0: Fixed Filter	
				1: Adaptive Comb Filter	
R_CP180_SEL	0x45[6:4]	RW	3	C Domain force 1D Filter Selection (Phase 180)	010
				000: High pass filter	
				001: Two-line filter(mode 2)	
				01x: Two-line filter(mode 0)	
				10x: Two-line filter(mode 1)	
				11x: Three-line filter	
R_CP180_AUTO	0x45[7]	RW	1	C Domain Comb Filter Enable (Phase 180)	1
				0: Fixed Filter	
				1: Adaptive Comb Filter	
R_CP90TAB_SEL	0x46[1:0]	RW	2	C Domain Filter Table Selection(Phase 90)	11
				00: Table 0	
				01: Table 1	
				10: Table 2	
				11: Table 3	
R_CREFY_EN	0x46[4]	RW	1	C Domain Reference Y Domain	1
				0:Disable	
				1:Enable	
R_YREFC_EN	0x46[5]	RW	1	Y Domain Reference C Domain	1
				0:Disable	
				1:Enable	
R_YP90REF13_EN	0x46[6]	RW	1	C Domain Reference line 2 and line 4 (Phase 90)	1
				0:Disable	
				1:Enable	

6.15 AGC and ACC Process

BIT1605 提供 AGC (Auto Gain Control)功能以控制 Analog PGA 所提供-6db、 0db、 6db 和 12db 四種 Gain value 及 Digital PGA 所提供+18db ~ -18db Linear Digial PGA，及提供 ACC (Auto Clamp Control)功能以控制 Analog Clamp 和 Digital Clamp。AGC 及 ACC 的控制可以維持輸入信號正常的振幅及準位，使得輸出的結果不會隨著信號的漂移改變而有所變化，進而影響畫面的穩定度。相關的示意圖請參考下圖，相關的 Register 設定請參考下表。

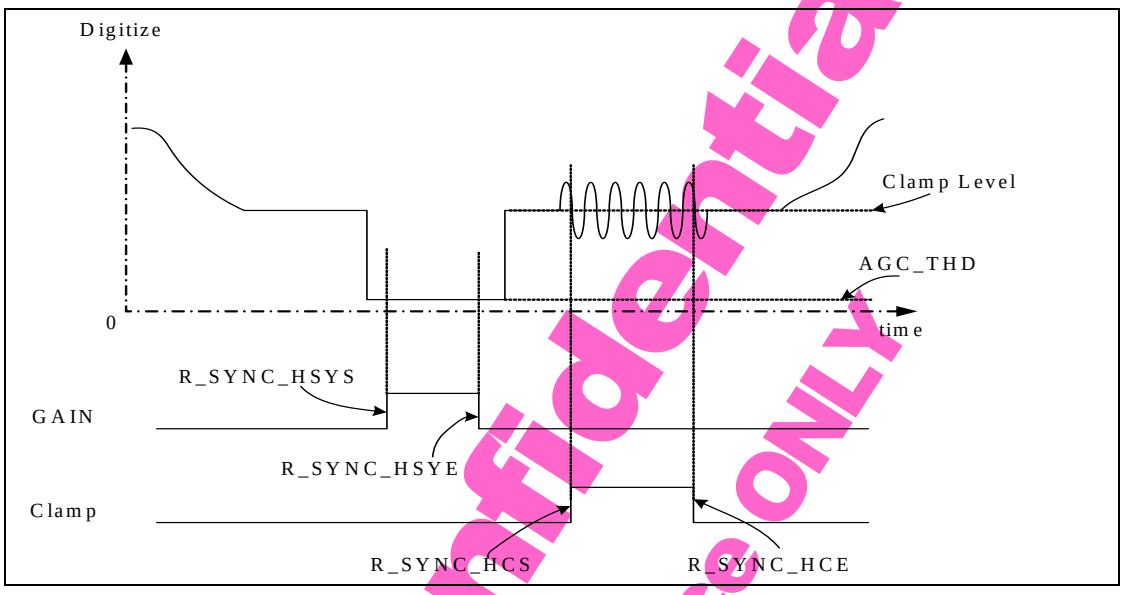


Figure 6-9 AGC and Clamp pulse

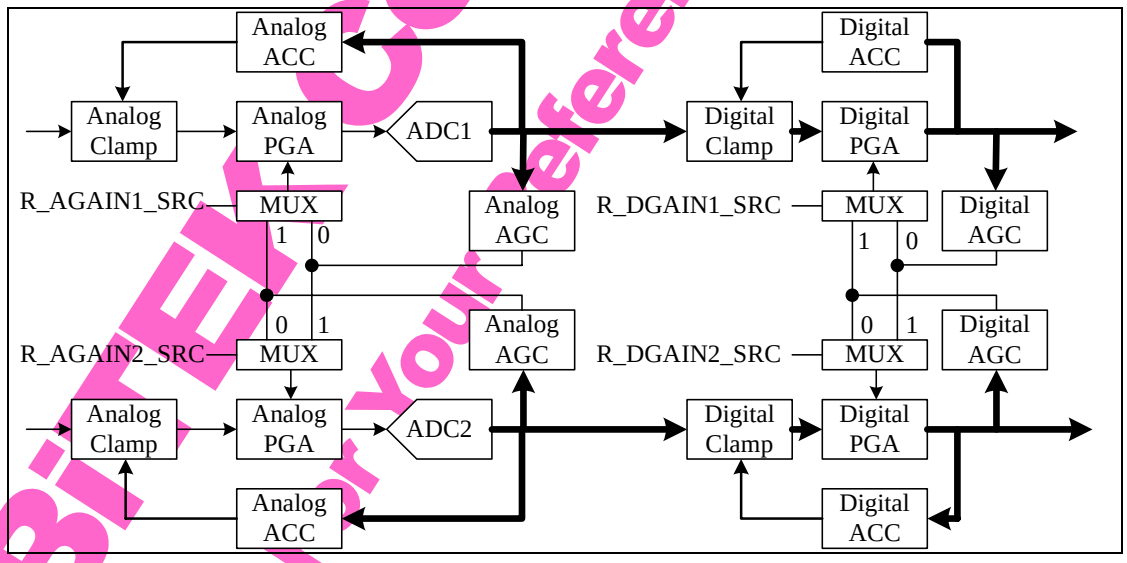


Figure 6-10 AGC Control selection

Table 6-23 AGC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ACLAMP_SPEED	0x47[7:0]	RW	8	Analog Clamp tracer speed	0x18
R_ACLAMP1_LEVEL	0x48[7:0]	RW	8	Analog Clamp 1 Level	0x30
R_ACLAMP2_LEVEL	0x49[7:0]	RW	8	Analog Clamp 2 Level	0x80
R_AAGC1_EN	0x4A[0]	RW	1	Analog AGC Enable for ADC1 0: Disable (R_AAGC1_VALUE) 1: Enable (Auto tracer)	1
R_AAGC1_HOLD	0x4A[1]	RW	1	Analog AGC Hold for ADC1	0

				0: Disable (tracer)	
				1: Enable (hold)	
R_AAGC1_VALUE	0x4A[3:2]	RW	2	Analog PGA 1 Value when AGC disable	10
				00: -6 db (x0.5)	
				01: 0 db (x1)	
				10: 6 db (x2)	
				11: 12 db (x4)	
R_ACLAMP1_EN	0x4A[4]	RW	1	Analog Clamp 1 Enable	1
				0: Disable (turn off Analog Clamp)	
				1: Enable	
R_ACLAMP1_TYPE	0x4A[5]	RW	1	Analog Clamp 1 Level Select	0
				0: R_ACLAMP1_LEVEL	
				1: Middle level	
R_SYNC1_CLAMP	0x4A[6]	RW	1	Analog Clamp 1 update signal	1
				0: VSYNC	
				1: HSYNC	
R_AUTO1_HOLD	0x4A[7]	RW	1	Auto ACC and AGC hold when tracer stable for ADC1	0
				0: Disable	
				1: Enable	
R_AGAIN1_SRC	0x0E[4]	RW	1	Analog gain source select for ADC1	0
				0: From ADC1 source	
				1: Reference with ADC2 AAGC value	
R_DAGC1_EN	0x4B[0]	RW	1	Digital AGC Enable for ADC1	1
				0: Disable (R_DAGC1_VALUE)	
				1: Enable (Auto tracer)	
R_DAGC1_HOLD	0x4B[1]	RW	1	Digital AGC Hold for ADC1	0
				0: Disable (tracer)	
				1: Enable (hold)	
R_DCLAMP1_EN	0x4B[2]	RW	1	Digital Clamp 1 Enable	1
				0: Disable (R_DCLAMP1_VALUE)	
				1: Enable	
R_DACLAMP1_HOLD	0x4B[3]	RW	1	Digital ACC Hold for ADC1	0
				0: Disable (tracer)	
				1: Enable (hold)	
R_DAGC1_THD	0x4B[7:4]	RW	4	Digital AGC 1 Tracer Level	0001
R_DAGC1_VALUE	0x4C[7:0]	RW	8	Manual Digital AGC 1 value	0x40
R_DCLAMP1_LEVEL	0x4D[7:0]	RW	8	Digital clamp1 level	0x3F
R_DCLAMP1_VALUE	0x4E[7:0]	RW	8	Manual Digital clamp1 value	0x00
R_DAGC1_SPEED	0x4F[5:0]	RW	6	Digital AGC 1 tracer speed	0x04
R_DIFFGAIN1_THD	0x4F[7:6]	RW	2	AGC and ACC ready threshold for ADC1	00
R_DGAIN1_SRC	0x0E[5]	RW	1	Digital gain source select for ADC1	0
				0: From ADC1 source	
				1: Reference with ADC2 DAGC value	
R_DAGC1_VSUP	0x50[0]	RW	1	Digital AGC 1 update signal	1
				0: HSYNC	
				1: VSYNC	
R_DAGC2_VSUP	0x50[1]	RW	1	Digital AGC 2 update signal	1
				0: HSYNC	
				1: VSYNC	
R_AAGC2_EN	0x52[0]	RW	1	Analog AGC Enable for ADC2	1
				0: Disable (R_AAGC2_VALUE)	
				1: Enable (Auto tracer)	
R_AAGC2_HOLD	0x52[1]	RW	1	Analog AGC Hold for ADC2	0
				0: Disable (tracer)	

				1: Enable (hold)	
R_AAGC2_VALUE	0x52[3:2]	RW	2	Analog PGA 2 Value when AGC disable	10
				00: -6 db (x0.5)	
				01: 0 db (x1)	
				10: 6 db (x2)	
				11: 12 db (x4)	
R_ACLAMP2_EN	0x52[4]	RW	1	Analog Clamp 2 Enable	1
				0: Disable (turn off Analog Clamp)	
				1: Enable	
R_ACLAMP2_TYPE	0x52[5]	RW	1	Analog Clamp 2 Level Select	1
				0: R_ACLAMP2_LEVEL	
				1: Middle level	
R_SYNC2_CLAMP	0x52[6]	RW	1	Analog Clamp 2 update signal	1
				0: VSYNC	
				1: HSYNC	
R_AUTO2_HOLD	0x52[7]	RW	1	Auto ACC and AGC hold when tracer stable for ADC2	0
				0: Disable	
				1: Enable	
R_AGAIN2_SRC	0x0E[6]	RW	1	Analog gain source select for ADC2	0
				0: From ADC2 source	
				1: Reference with ADC1 AAGC value	
R_DAGC2_EN	0x53[0]	RW	1	Digital AGC Enable for ADC2	1
				0: Disable (R_DAGC2_VALUE)	
				1: Enable (Auto tracer)	
R_DAGC2_HOLD	0x53[1]	RW	1	Digital AGC Hold for ADC2	0
				0: Disable (tracer)	
				1: Enable (hold)	
R_DCLAMP2_EN	0x53[2]	RW	1	Digital Clamp 2 Enable	1
				0: Disable (R_DCLAMP2_VALUE)	
				1: Enable	
R_DACLAMP2_HOLD	0x53[3]	RW	1	Digital ACC Hold for ADC2	0
				0: Disable (tracer)	
				1: Enable (hold)	
R_DAGC2_THD	0x53[7:4]	RW	4	Digital AGC 2 Tracer Level	0001
R_DAGC2_VALUE	0x54[7:0]	RW	8	Manual Digital AGC 2 value	0x40
R_DCLAMP2_LEVEL	0x55[7:0]	RW	8	Digital clamp2 level	0x80
R_DCLAMP2_VALUE	0x56[7:0]	RW	8	Manual Digital clamp2 value	0x00
R_DAGC2_SPEED	0x57[5:0]	RW	6	Digital AGC 2 tracer speed	0x04
R_DIFFGAIN2_THD	0x57[7:6]	RW	2	AGC and ACC ready threshold for ADC2	00
R_DGAIN2_SRC	0x0E[7]	RW	1	Digital gain source select for ADC2	0
				0: From ADC2 source	
				1: Reference with ADC1 DAGC value	

6.16 AFE and PLL Control

BIT1605 內建 AFE(Analog Front End) 設定參數，相關設定請參考下表。

Table 6-24 ADC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AFE_CS	0x5A[1:0]	RW	2	AFE Clamp current	00
R_AFE_CTRPH	0x5A[3:2]	RW	2	AFE Phase Non-overlap time	00
R_AFE_CTRIB	0x5A[6:4]	RW	3	AFE Bias current control	110
R_AFE_SH2VCM	0x5A[7]	RW	1	AFE Internal shortcut on both PGA	0
R_AFE_ENIB	0x5B[0]	RW	1	AFE Bias current enable	1
R_AFE_ENREF	0x5B[1]	RW	1	AFE Reference Generator enable	1
R_AFE_ENVBG	0x5B[2]	RW	1	AFE Band gap Generator enable	1
R_AFE_ENVCM	0x5B[3]	RW	1	AFE common mode voltage Generator enable	1
R_AFE_ENAY	0x5B[4]	RW	1	Power Down Input for ADC1 0: Power Down 1: Normal Operation	1
R_AFE_ENAC	0x5B[5]	RW	1	Power Down Input for ADC2 0: Power Down 1: Normal Operation	1
R_AFE_BYP	0x5B[6]	RW	1	Bypass PGA for ADC test	0
R_AFE_DEC	0x5B[7]	RW	1	Control output data decimator by 8 or none (dec = 0 : normal operation)	0
R_PLL_POR	0x5C[0]	RW	1	PLL Power on Reset	0
R_PLL_EAPLL	0x5C[1]	RW	1	PLL Enable 0: Disable 1: Enable	1
R_PLL_ICP0	0x5C[2]	RW	1	PLL Factor 0	0
R_PLL_ICP1	0x5C[3]	RW	1	PLL Factor 1	0
R_PLLDTO_ROL	0x5C[4]	RW	1	PLL Factor 2	0

6.17 Background and Test Pattern Setup

BIT1605 內部提供 8 種內定Test patterns，分別爲 8 種純色、Color Bar、漸層(Ramp)與格線(Grid)，其相關設定Register及其意義請參考 **Table 6-25**。

Table 6-25 Background and Test Pattern Register

Mnemonic	Address	R/W	Bits	Description	Default
R_TESTPAT_TYPE	0x5F[6:5]	RW	2	Test Pattern Type 00: 8 純色 01: Color Bar 10: 漸層(Ramp) 11: 格線(Grid)	00
R_TESTPAT_MODE	0x5F[4:2]	RW	3	R_TESTPAT_TYPE = 00 000: Black 001: Yellow 010: Cyan 011: Green 100: Magenta 101: Red 110: Blue 111: White R_TESTPAT_TYPE = 10 0x5F[4] = 0:Y = 0x80 0x5F[4] = 1:Y = Ramp 0x5F[3] = 0:U = 0x80 0x5F[3] = 1:U = Ramp	000

				0x5F[2] = 0:V = 0x80	
				0x5F[2] = 1;V = Ramp	
R_TESTPAT_SEL	0x5F[1:0]	RW	2	R_TESTPAT_TYPE = 00,01	
				0x5F[0] = 0: 75%	
				0x5F[0] = 1: 100%	
				R_TESTPAT_TYPE = 10	
				0x5F[1:0] = 00: Right to Left Increase	
				0x5F[1:0] = 01:Left to Right Increase	00
				0x5F[1:0] = 10:Bottom to Top Increase	
				0x5F[1:0] = 11:Top to Bottom Increase	
				R_TESTPAT_TYPE = 11	
				0x5F[0] = 0: 1 Pixel	
				0x5F[0] = 1: 2 Pixels	
R_BACKGROUND_EN	0x5D[6]	RW	1	Background Mode Enable	
				0: Disable	1
				1: Enable	
R_FREERUN_EN	0x5D[7]	RW	1	Free-Run Mode Enable	
				0: Disable	1
				1: Enable	

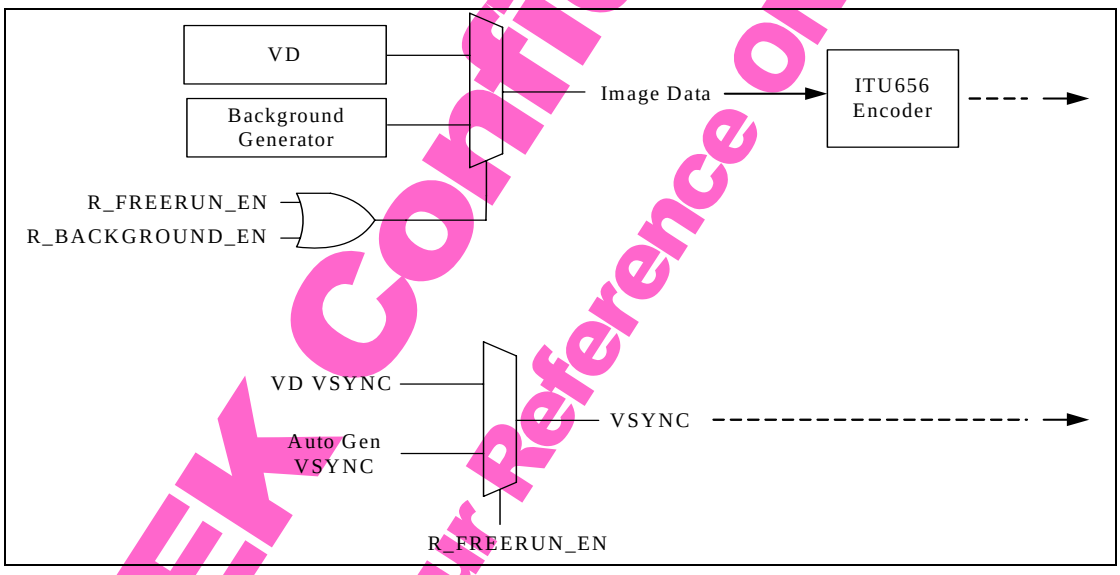


Figure 6-11 Free run and Background

6.18 Auto Blank Screen

BIT1605 內建自動 Blank Screen Function，當訊號中斷或模式切換時將會自動啓動 Blank Screen 畫面，相關設定 Register 請參考下表。

Table 6-26 Blank Screen Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTOON_TIME	0x5E[5:0]	RW	6	Blank Screen to Normal Screen Delay Time (based on VSYNC)	0x00
R_AUTOON_EN	0x5E[7]	RW	1	Blank Screen Function Enable 0: Disable 1: Enable	0
R_HLCK_SEL	0x5D[4:2]	RW	3	Signal Ready (For AUTOON Reference) 000: None 001: STD_READY 010: SYNC_READY 011: SYNC_READY & STD_READY 100: HLCK 101: HLCK & STD_READY 110: HLCK & SYNC_READY 111: HLCK & SYNC_READY & STD_READY	100
R_FIDTCHG_EN	0x5D[1]	RW	1	FIDT Enable(For AUTOON Reference) 0: Disable 1: Enable	0
R_SIGRDY_EN	0x5D[0]	RW	1	Signal Ready Enable (For AUTOON Reference) 0: Disable 1: Enable	1
R_AUTOON_RDY_O	0x7B[4]	R	1	Blank Screen Function Ready 0: No Ready 1: Ready	-

6.19 Output Data Path

BIT1605 可針對輸出的Data Bus分別做Invert和Rotate等等的處理，其相關設定Register請參考 **Table 6-27**，相對應方塊圖請參考 **Figure 6-12**, **Figure 6-13**, **Figure 6-14**, **Figure 6-15** 和 **Figure 6-16**。

Table 6-27 Output Data Path Register

Mnemonic	Address	R/W	Bits	Description	Default
R_HCLAMP_EN	0x65[0]	RW	1	HS Clamp 0:Disable 1:Enable(Y: 0x10~0xEB; CbCr: 0x10~0xF0)	0
R_VCLAMP_EN	0x65[1]	RW	1	VS Clamp 0:Disable 1:Enable(VS Blanking Y = 0x10, CbCr = 0x80)	0
R_CBCR_SEL	0x65[3:2]	RW	2	Cb and Cr data select 00: Delay 1 01: Delay 0 1x: UV average	01
R_HSHEAD_EN	0x65[6]	RW	1	HS Head Enable 0:Disable 1:Enable	0
R_ITU656_EN	0x65[7]	RW	1	ITU656 Enable	0

				0:Disable	
				1:Enable	
R_DLY_DAT	0x66[1:0]	RW	2	Data sequence Shift Control	
				00: No Shift	
				01: Shift 1 Clock	11
				10: Shift 2 Clocks	
				11: Shift 3 Clocks	
R_SEL_EVEN	0x66[5:4]	RW	2	EVEN/ODD Signal Select	
				00: ITU656-EVEN Signal	
				01: Invert	00
				10: Always 1	
				11: Always 0	
R_POL_OHS	0x67[0]	RW	1	HS Output Polarity	
				0: Normal	0
				1: Invert	
R_POL_OVS	0x67[1]	RW	1	VS Output Polarity	
				0: Normal	0
				1: Invert	
R_POL_OEVEN	0x67[2]	RW	1	EVEN Output Polarity	
				0: Normal	0
				1: Invert	
R_POL_DOUT	0x67[3]	RW	1	Data Output Polarity	
				0: Normal	0
				1: Invert	
R_ROL_DOUT	0x67[4]	RW	1	Data Output Rotation	
				0:Disable	0
				1:Enable	
R_POL_PREHS	0x67[6]	RW	1	Pre HS Polarity	
				0: Normal	0
				1: Invert	
R_POL_PREVS	0x67[7]	RW	1	Pre VS Polarity	
				0: Normal	0
				1: Invert	
R_DLY_IVS	0x68[7:0]	RW	8	Vertical Sync Delay	0x00
R_VS_ADJS	0x69[6:0]	RW	7	Display Window Vertical Start Position	0x04
R_VS_ADJE	0x6A[6:0]	RW	7	Display Window Vertical End Position	0x00
R_SAV_DLY	{0x69[7],0x6B[7:0]}	RW	9	Display Window Horizontal Start Position	0x000
R_EAV_DLY	{0x6A[7],0x6C[7:0]}	RW	9	Display Window Horizontal End Position	0x000
R_DISPCUT_MODE	0x60[6:4]	RW	3	Display Window Cut Mode	
				000: Black	
				001: Yellow	
				010: Cyan	
				011: Green	000
				100: Magenta	
				101: Red	
				110: Blue	
				111: White	
R_DISPCUT_EN	0x60[7]	RW	1	Display Window Cut	
				0:Disable	0
				1:Enable	
R_DISPCUT_VS	0x63[7:0]	RW	8	Display Cut Vertical Start Position	0x00
R_DISPCUT_VE	{0x60[0],0x64[7:0]}	RW	9	Display Cut Vertical End Position	0x000
R_DISPCUT_HS	{0x60[3],0x61[7:0]}	RW	9	Display Cut Horizontal Start Position	0x000
R_DISPCUT_HE	{0x60[2:1],0x62[7:0]}	RW	10	Display Cut Horizontal End Position	0x000
R_RAW_EN	0x7F[0]	RW	1	Raw Data Output Enable(For test only)	0

				0 : Disable	
				1 : Enable	
R_RAW_SEL	0x7F[3:1]	RW	3	Raw Data Select(For test only)	000
				000: ADC1 Data	
				001: ADC2 Data	
				010: Y Data	
				011: U Data	
				1xx: V Data	
R_ADC1_RAW	0x7F[4]	RW	1	ADC1 Data Select(For test only)	0
				0:From AGC1	
				1:From ADC1	
R_ADC2_RAW	0x7F[5]	RW	1	ADC2 Data Select(For test only)	0
				0:From AGC2	
				1:From ADC2	
R_FIELD_MODE	0x78[1:0]	R	2	EVEN/ODD Mode Detection	-
				01: Always ODD Field	
				10: Always EVEN Field	
				00: VS != VS Delay	
R_STD_FIELD	0x78[2]	R	1	EVEN/ODD Signal Detection	-
				0: Non Standard	
				1: Standard	

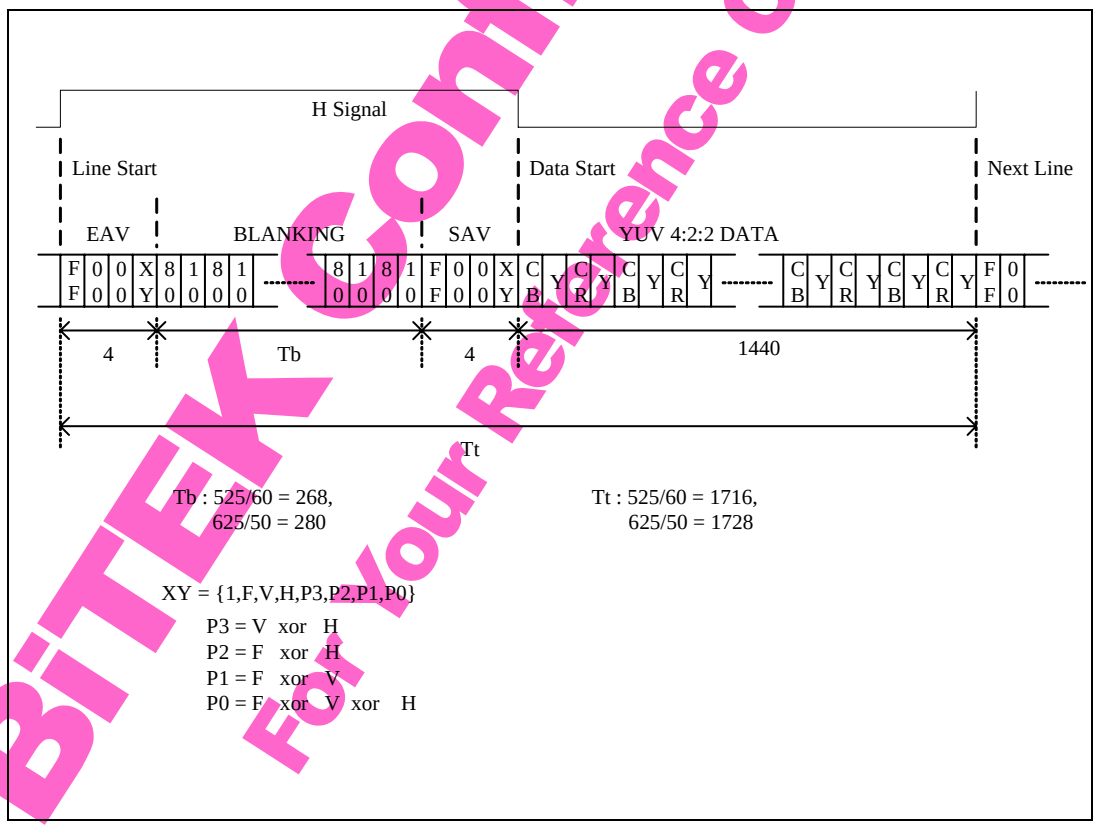
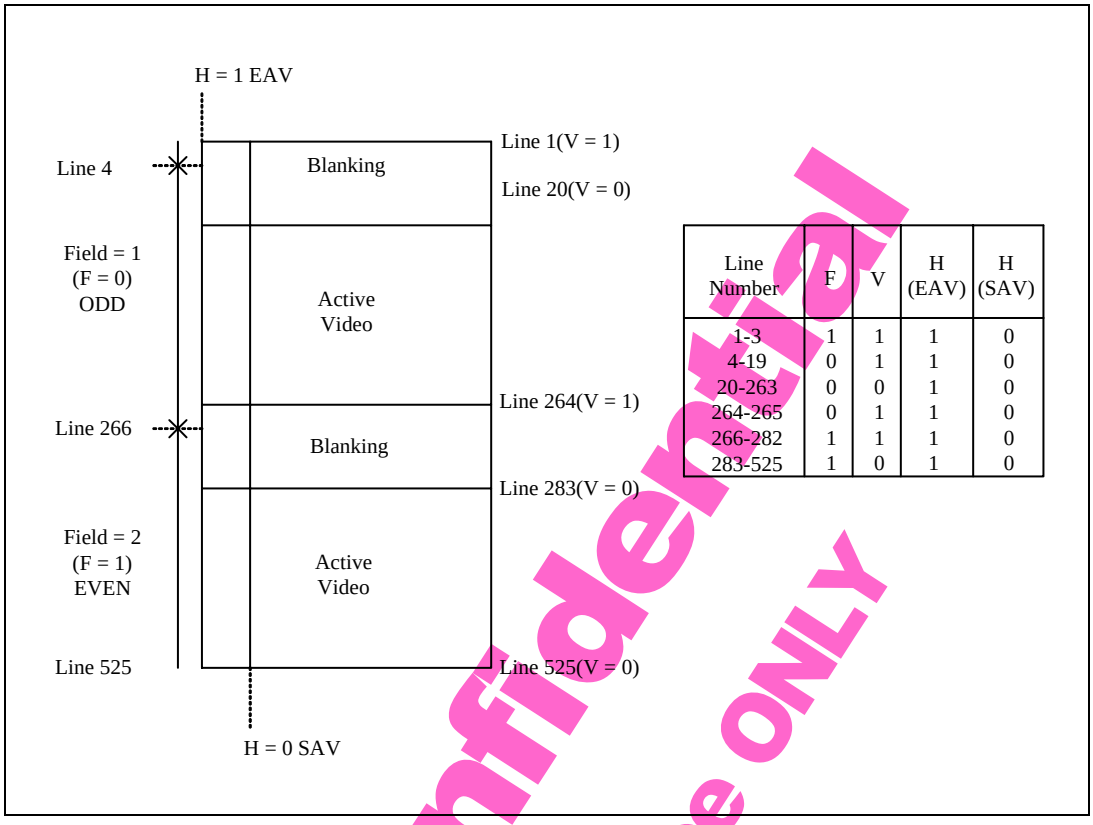
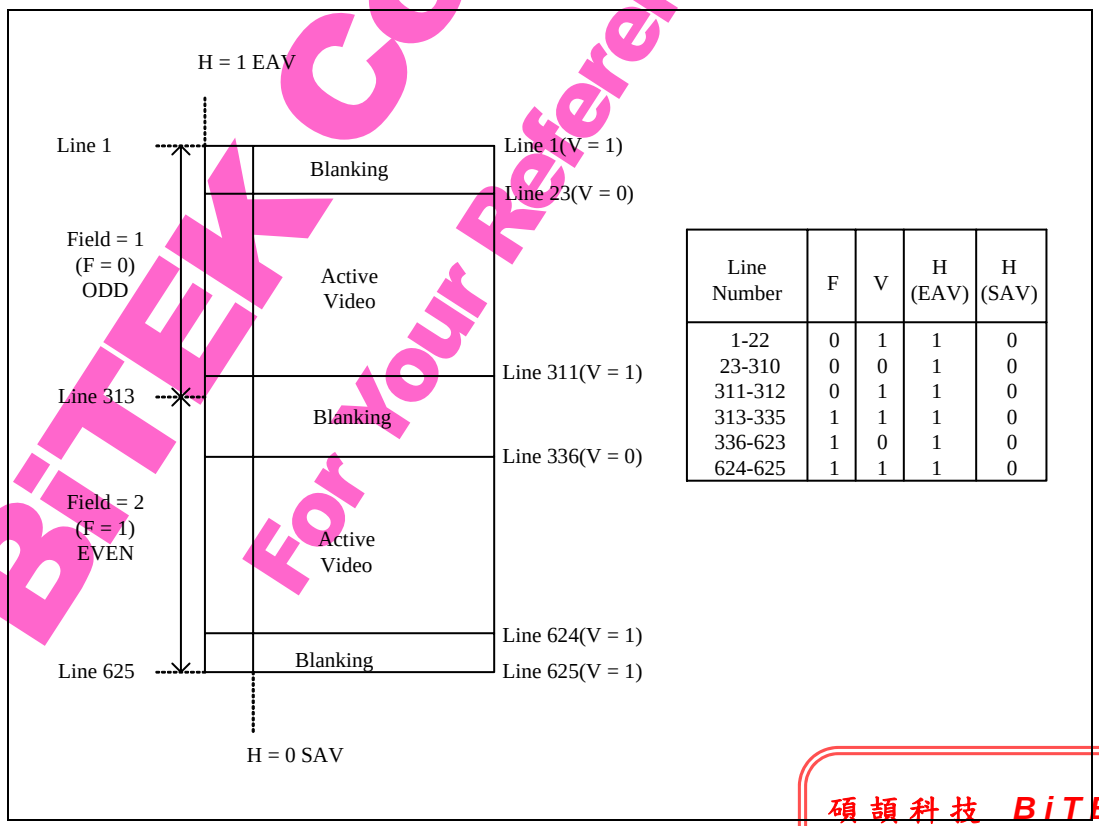


Figure 6-12 YUV Data Format
(Horizontal Timing; When R_SAV_DLY = 0x000, R_EAV_DLY = 0x000)



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-19	0	1	1	0
20-263	0	0	1	0
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

Figure 6-13 YUV Data Format
(525/60 Vertical Timing; When R_VS_ADJS = 0x04, R_VS_ADJE = 0x00)



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

Figure 6-14 YUV Data Format
(625/50 Vertical Timing;When R_VS_ADJS = 0x04, R_VS_ADJE = 0x00)

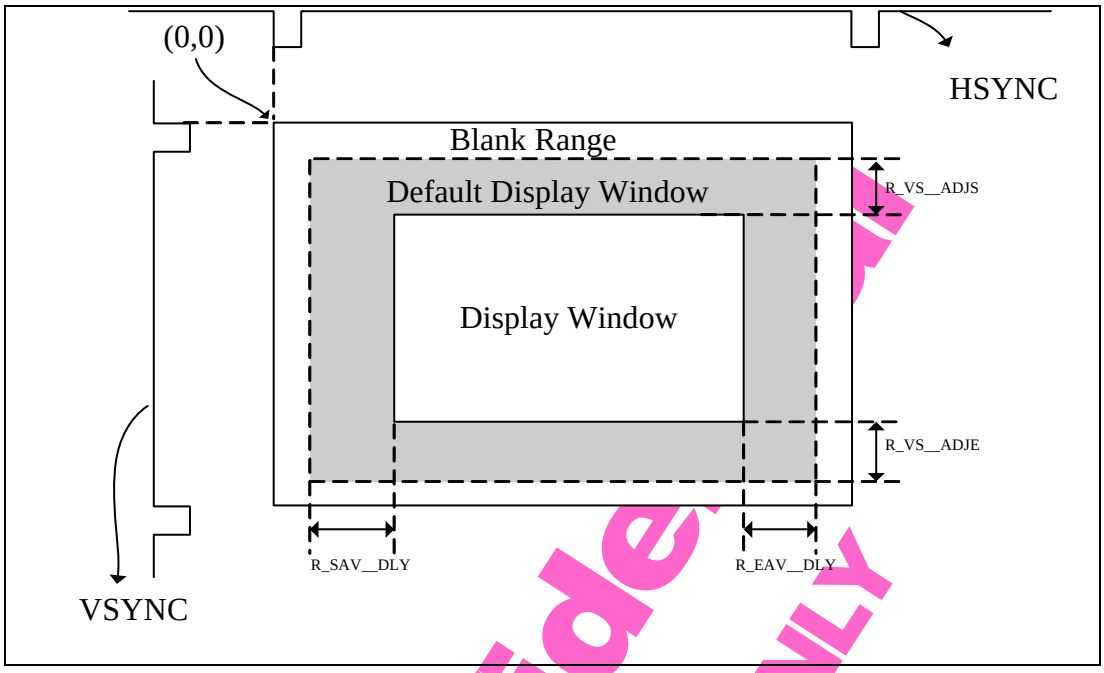


Figure 6-15 Display Window

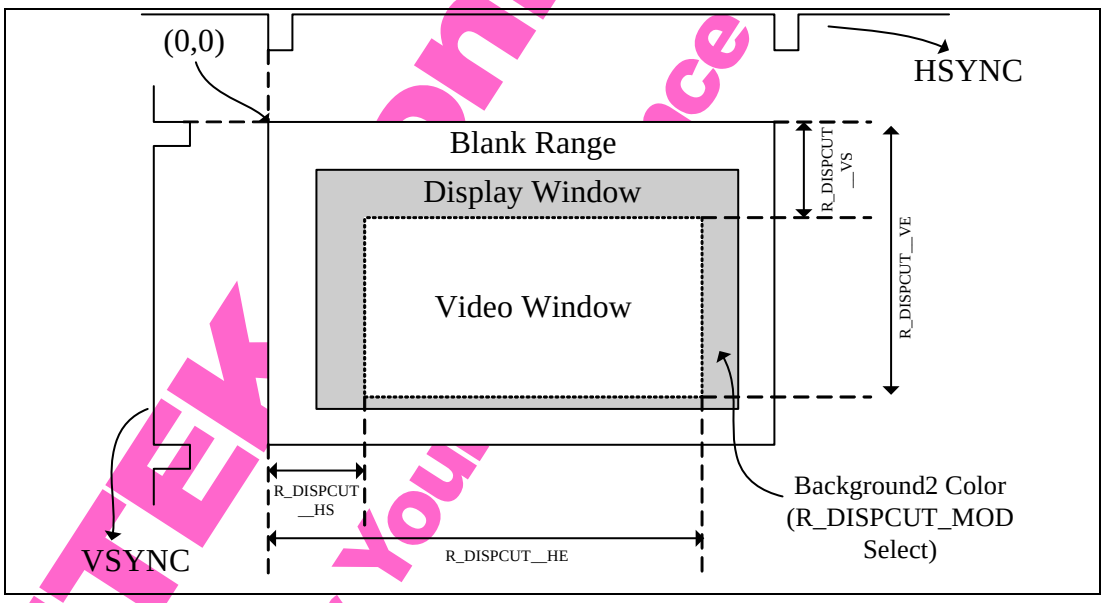


Figure 6-16 Display Window Cut Setup

6.20 Special Output Setup

BIT1605 提供 4 組Special Output Pads (RTS0(Pin 14)、RTS1(Pin 13) 、RTS2(Pin 10)和RTS3 (Pin 9))，可經由Register分別設定特定輸出功能，其相關設定Register及其意義請參考 **Table 6-28**。

Table 6-28 Special Output Pads Setup Register

Mnemonic	Address	R/W	Bits	Description	Default
R_RTS0_SEL	0x6E[3:0]	RW	4	0000: Output HSYNC Signal	0000
				0001: Output VSYNC Signal	
				0010: Output HREF Signal	
				0011: Output VREF Signal	
				0100: Output EVEN/ODD Signal	
				0101: Output INT Signal	
				0110: General Output Port Bit [0] (R_GPO_REG[0])	
				0111: Tri-State Output	
				1000: Output Auto On Signal(For test only)	
				1001: Output HSY Signal(For test only)	
				1010: Output HC Signal(For test only)	
				1011: Output VSI Signal(For test only)	
				1100: Output HSI Signal(For test only)	
				1101: Output HLCK Signal(For test only)	
				1110: Output HLCK_SEL Signal(For test only)	
				1111: Output FIFO OVER Signal(For test only)	
R_RTS0_POL	0x6F[0]	RW	1	RTS0 Clock Polarity ➔ 0:normal 1:invert	0
R_RTS1_SEL	0x6E[7:4]	RW	4	0000: Output HSYNC Signal	0001
				0001: Output VSYNC Signal	
				0010: Output HREF Signal	
				0011: Output VREF Signal	
				0100: Output EVEN/ODD Signal	
				0101: Output INT Signal	
				0110: General Output Port Bit [1] (R_GPO_REG[1])	
				0111: Tri-State Output	
				1000: Output HREF & VREF Signal(For test only)	
				1001: Output HSY Signal(For test only)	
				1010: Output HC Signal(For test only)	
				1011: Output VSI Signal(For test only)	
				1100: Output HSI Signal(For test only)	
				1101: Output SYNC_READY Signal(For test only)	
				1110: Output SRC2_SEL Signal(For test only)	
				1111: Output FIFO UNDER Signal(For test only)	
R_RTS1_POL	0x6F[1]	RW	1	RTS1 Clock Polarity ➔ 0:normal 1:invert	0
R_RTS2_SEL	0x6D[3:0]	RW	4	0000: Output HSYNC Signal	0101
				0001: Output VSYNC Signal	
				0010: Output HREF Signal	
				0011: Output VREF Signal	
				0100: Output EVEN/ODD Signal	
				0101: Output INT Signal	
				0110: General Output Port Bit [2] (R_GPO_REG[2])	
				0111: Tri-State Output	
				1000: Output raw_data[0] Signal(For test only)	
				1001: Output HSY Signal(For test only)	
				1010: Output HC Signal(For test only)	
				1011: Output VSI Signal(For test only)	
				1100: Output HSI Signal(For test only)	
				1101: Output STD_READY Signal(For test only)	
				1110: Output SRC2 Signal(For test only)	

				1111: Output AGC1_READY Signal(For test only)	
R_RTS2_POL	0x6F[2]	RW	1	RTS2 Clock Polarity ➔ 0:normal 1:invert	0
R_RTS3_SEL	0x6D[7:4]	RW	4	0000: Output HSYNC Signal	0000
				0001: Output VSYNC Signal	
				0010: Output HREF Signal	
				0011: Output VREF Signal	
				0100: Output EVEN/ODD Signal	
				0101: Output INT Signal	
				0110: General Output Port Bit [3] (R_GPO_REG[3])	
				0111: Tri-State Output	
				1000: Output Raw Data[1] Signal(For test only)	
				1001: Output HSY Signal(For test only)	
				1010: Output HC Signal(For test only)	
				1011: Output VSI Signal(For test only)	
				1100: Output HSI Signal(For test only)	
				1101: Output FIDT Signal(For test only)	
				1110: Output SRC11 Signal(For test only)	
				1111: Output AGC2_READY Signal(For test only)	
R_RTS3_POL	0x6F[3]	RW	1	RTS3 Clock Polarity ➔ 0:normal 1:invert	0

6.21 FIFO Output Mode

BIT1605 針對 DVR 應用提供 FIFO Output Mode 功能可使得資料 Capture 的 Clock 採用與外部同步的模式，其相關設定 Register 及其意義請參考下表。

Table 6-29 FIFO Output Mode Register

Mnemonic	Address	R/W	Bits	Description	Default
R_OCLK_SEL	0x0A[3:2]	RW	2	OCLK Domain Polarity(FIFO output clock) must setup to 10 and FIFO output clock input from CLK27I(Pin27)	00
R_FIFO_RESET	0x6F[4]	RW	1	FIFO Controller Reset	0
				0: Normal running	
				1: Reset	
R_FIFO_RD	0x6F[5]	RW	1	FIFO Read Enable	1
				0: Stop Read from FIFO	
				1: Start Read from FIFO	
R_FIFO_WR	0x6F[6]	RW	1	FIFO Write Enable	1
				0: Stop Write to FIFO	
				1: Start Write to FIFO	
R_FIFO_UNDER	0x7C[2]	R	1	FIFO Mode Underflow Detection	-
R_FIFO_OVER	0x7C[3]	R	1	FIFO Mode Overflow Detection	-
				0: No Error	
				1: Error Detection	

6.22 Status Register

BIT1605 提供 Read Only Register 可供讀取 BIT1605 內部 Status，相關 Register 請參考下表。

Table 6-30 Video Decoder Status Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DAGC1_OUT	0x70[7:0]	R	8	Digital AGC1 tracer value	-
R_DCLAMP1_OUT	0x71[7:0]	R	8	Digital Clamp1 tracer value	-
R_DAGC2_OUT	0x72[7:0]	R	8	Digital AGC2 tracer value	-
R_DCLAMP2_OUT	0x73[7:0]	R	8	Digital Clamp2 tracer value	-
R_AAGC1_OUT	0x74[1:0]	R	2	Analog AGC1 tracer value	-
R_AAGC2_OUT	0x74[3:2]	R	2	Analog AGC2 tracer value	-
R_CHROMA_GAINOUT	{0x74[7:4],0x75[7:0]}	R	12	Chroma GAIN tracer value	-

R_INCCHRO_O	{0x78[3],0x76[7:0],0x77[7:0]}	R	17	PLL tracer value	-
R_FIELD_MODE	0x78[1:0]	R	2	EVEN/ODD Mode Detection	-
				01: Always ODD Field	
				10: Always EVEN Field	-
				00: VS != VS Delay	
R_STD_FIELD	0x78[2]	R	1	EVEN/ODD Signal Detection	
				0: Non Standard	-
				1: Standard	
R_STD_FREQ	0x78[5:4]	R	2	Color Burst Detection	
				00: 3.57MHz	
				01: 4.2MHz	-
				10: 4.3 MHz	
				11: Non-standard	
R_COLOR_STANDARD	0x79[2:0]	R	3	Color Standard Detection Result	
				000: PAL	
				001: PAL_N	
				010: SECAM	
				011: PAL_M	-
				100: NTSC_4.43_50Hz	
				101: NTSC_M / NTSC_J	
				110: NTSC_4.43_60Hz	
				111: B&W (Black & White)	
R_COLORDET	0x79[3]	R	1	Color detection result	
				0: No color or low color	-
				1: Color source	
R_SQP_COUNT	0x79[7:4]	R	4	Burst phase detect	-
R_FIDT_O	0x7A[0]	R	1	50/60Hz detect	
				0: 50Hz	-
				1: 60Hz	
R_HLCK_O	0x7A[1]	R	1	H-LOCK Ready	
				0: Not Ready	-
				1: Ready	
R_SYNC_READY_O	0x7A[2]	R	1	Auto Sync Detect Ready	-
R_STD_READY_O	0x7A[3]	R	1	Auto Color Standard Detect Ready	-
R_DAGC1_READY	0x7A[4]	R	1	AGC1 tracer ready	-
R_DAGC2_READY	0x7A[5]	R	1	AGC2 tracer ready	
				0: Not ready	-
				1: Ready	
R_SRC2	0x7B[0]	R	1	Source detection result for AIN2	-
R_SRC12	0x7B[1]	R	1	Source detection result for AIN12	-
R_SRC11	0x7B[2]	R	1	Source detection result for AIN11	-
				0: No signal toggle	-
				1: Signal toggle	-
R_STD_PHASE	0x7B[3]	R	1	Burst Phase detection	
				0: 0 – 180 – 0	-
				1: 0 – 90 – 180 – 270 – 0	
R_AUTOON_RDY_O	0x7B[4]	R	1	Blank Screen Function Ready	
				0: No Ready	-
				1: Ready	
R_CC_INT	0x7C[0]	R	1	Data Slicer Interrupt	
				0: No CC data	-
				1: CC data ready	
R_CC_ERROR	0x7C[1]	R	1	Data Slicer Error	-
				0: Normal	

				1: Error	
R_FIFO_UNDER	0x7C[2]	R	1	FIFO Mode underflow detection	-
R_FIFO_OVER	0x7C[3]	R	1	FIFO Mode overflow detection 0: No error 1: Error detection	-
R_MV_DET_SYNC	0x7C[4]	R	1	MV source detect 0: Not MV source 1: MV Source	-
R_MV_DET_CHROMA	0x7C[5]	R	1	MV source on Chroma 0: Not MV Source 1: MV Source	-
R_MV_TYPE_CHROMA	0x7C[6]	R	1	MV type on Chroma 0: type2 1: type3	-
R_CC_DATA1	0x7D[7:0]	R	8	Data Slicer First Byte	-
R_CC_DATA2	0x7E[7:0]	R	8	Data Slicer Second Byte	-

7 User Interface

7-1 Option Pins

BIT1605 使用 2 根外部PIN(INF1 和INF0)來做位址的選擇，外部的MCU可以由PIN SCL、SDA經由Two Wire Serial Interface (TWSI) 控制BIT1605。定義及使用方法請參考下表，其示意圖可參考 **Figure 7-1**。

Table 7-1 Option Pins Setup

INF1	INF0	SCL	SDA	Slave Address
0	0	SCL	SDA	0x40~0x41
0	1	SCL	SDA	0x44~0x45
1	0	SCL	SDA	0x48~0x49
1	1	SCL	SDA	0x4C~0x4D

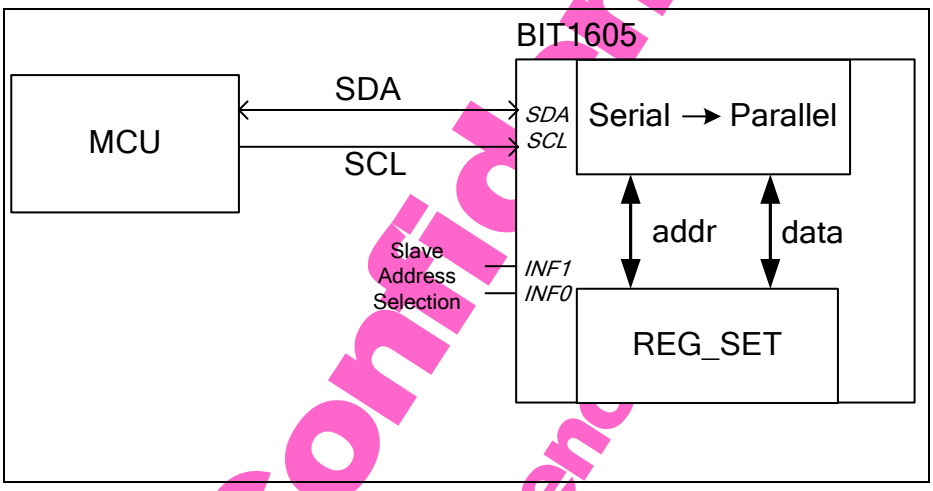


Figure 7-1 Slave Mode

7-2 Two-Wire Serial Interface Protocol

BIT1605 Two-Wire Serial Interface (TWSI) Protocol 須在送出 Start Bit 之後送出 8 Bits Device Address (slave address)，並可由外部 PIN(INF1、INF0)決定其 Device Address 的 Bit3 and Bit2 位址。相關設定請參考下表。

Table 7-2 TWSI Protocol Device Address

Internal Register Address	Write Device Address	Read Device Address
0x000~0x07F (Register Bank)	0x40(PIN35= 0、PIN34= 0) 0x44(PIN35= 0、PIN34= 1) 0x48(PIN35= 1、PIN34= 0) 0x4C(PIN35= 1、PIN34= 1)	0x41(PIN35= 0、PIN34= 0) 0x45(PIN35= 0、PIN34= 1) 0x49(PIN35= 1、PIN34= 0) 0x4D(PIN35= 1、PIN34= 1)

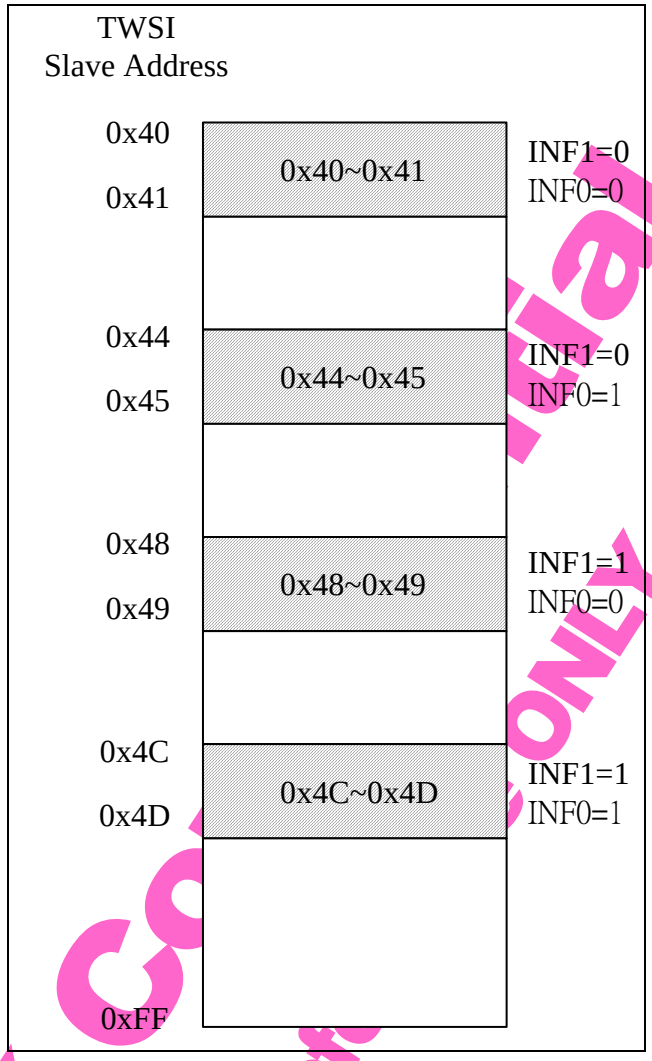


Figure 7-2 TWSI Slave Mapping Address

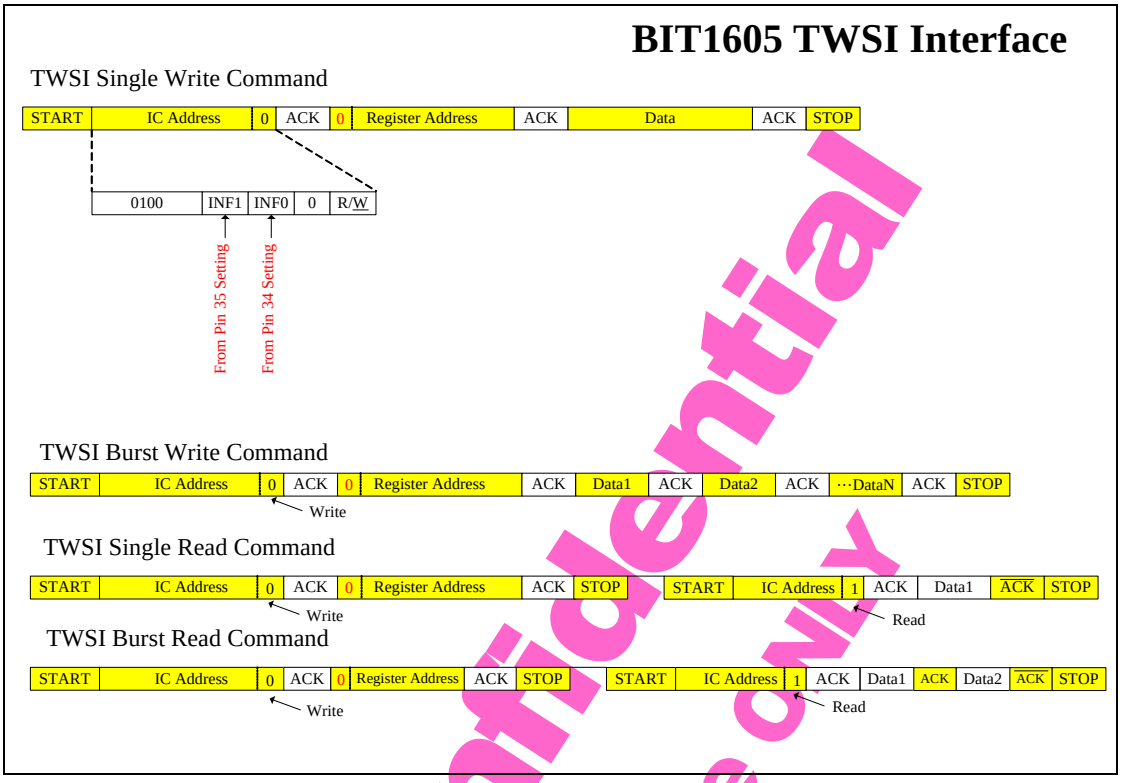
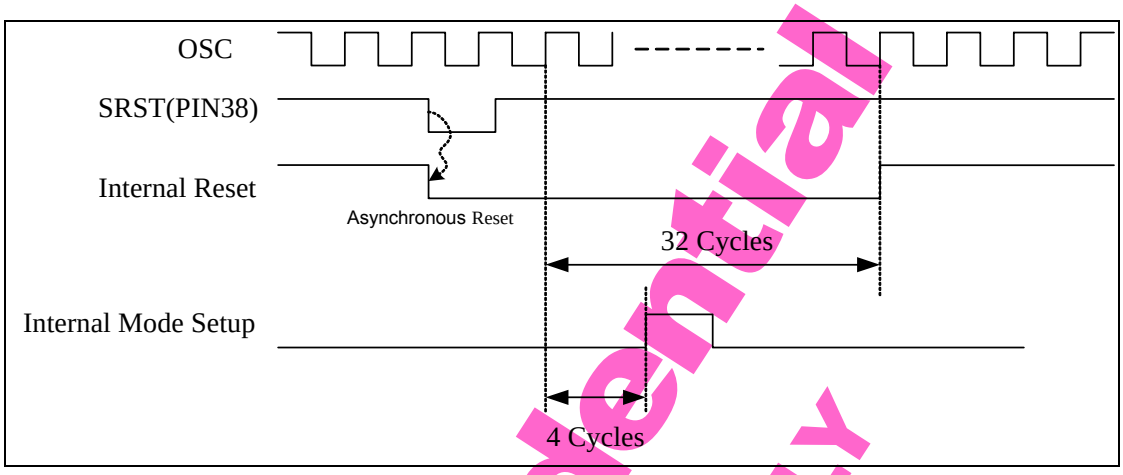


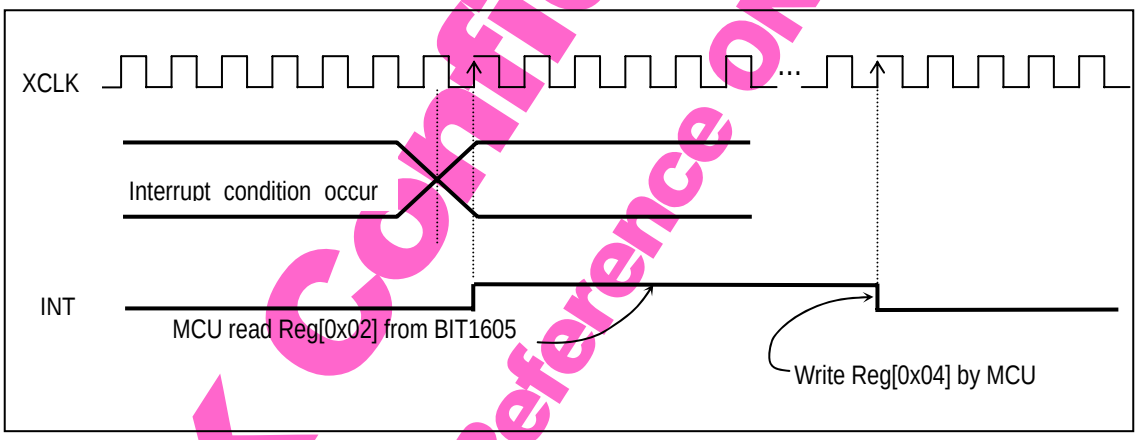
Figure 7-3 TWSI Read/Write Mode

8 Timing Diagram

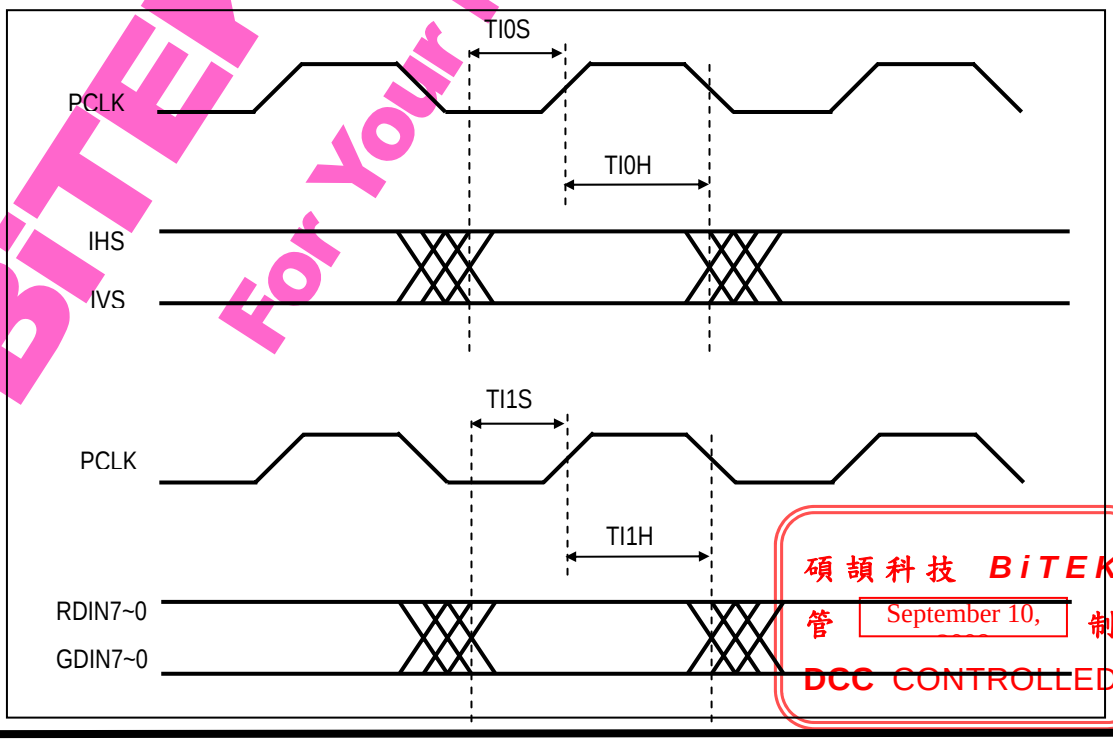
8-1 Hardware Reset:



8-2 Clock and Interrupt:

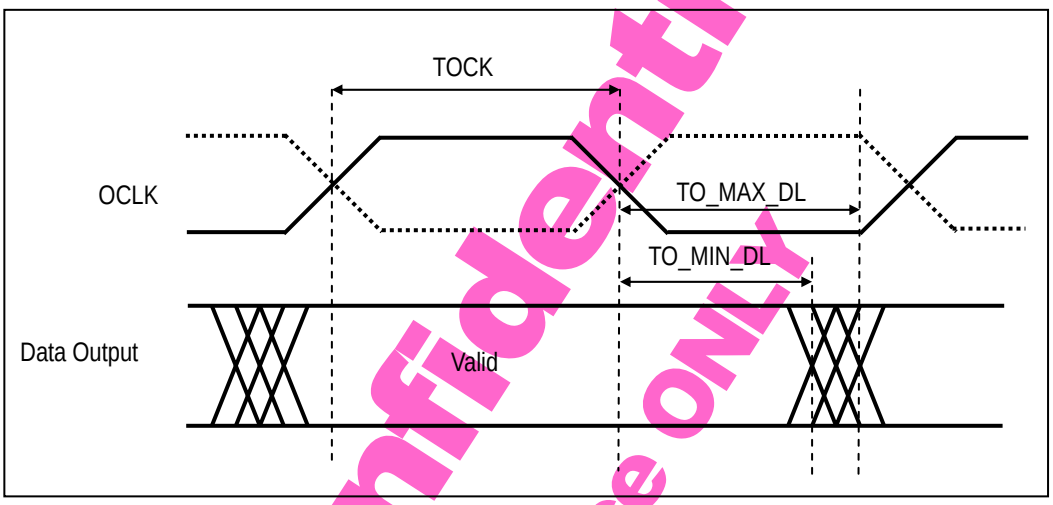


8-3 Input Signal:



Symbol	Describe	Max.	Min.	Unit
TI0S,TI1S	Input Setup time		2	Ns
TI0H,TI1H	Input Hold time		2	Ns

8-4 Output Signal:



Symbol	Describe	Timing	Unit
TOCK	Output clock half period		ns
TO_MAX_DL	Output signal Max delay	TOCK - 1	ns
TO_MIN_DL	Output signal Min delay	TOCK - 4	ns

9 Electrical Characteristic

9-1 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	-0.5		3.6	V
VDD18	Supply Voltage for Digital Core	- 0.5		2.5	V
V_{IN}	Input Voltage for Digital Core (5V Tolerant)	- 0.5		6	V
T_{STG}	Storage Temperature	- 40		125	℃

9-2 Recommend Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	3.0	3.3	3.6	V
VDD18	Supply Voltage for Digital Core	1.62	1.8	1.98	V
VDD33	Supply Voltage for I/O Pad	3.0	3.3	3.6	V
T_{OPR}	Operating Temperature	-20		85	℃

9-3 DC Electrical Characters

(under Recommend Operating Condition and T_J =0℃ to 115℃)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	No pull-up nor pull-down			10	uA
I_{OZ}	Tri-state Leakage Current				10	uA
V_{IL}	Input Low Voltage	CMOS	-0.3		0.8	V
V_{IH}	Input High Voltage	CMOS	2.0		5.5	V
V_{OL}	Output Low Voltage	I_{OL}= 4,8,16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= 4,8, 16 mA	2.4			V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	0.89	0.94	0.99	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	1.44	1.50	1.56	V
Rpu	Pull-up Resistance		39	65	116	KΩ
Rpd	Pull-down Resistance		40	56	108	KΩ

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance about 0.5pF and the package capacitance.

10 Soldering Information

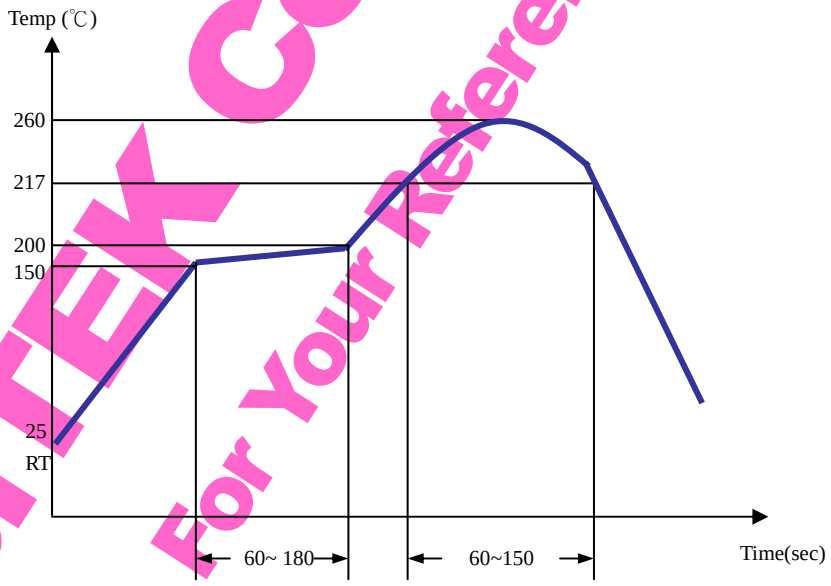
10-1 Reflow Soldering

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



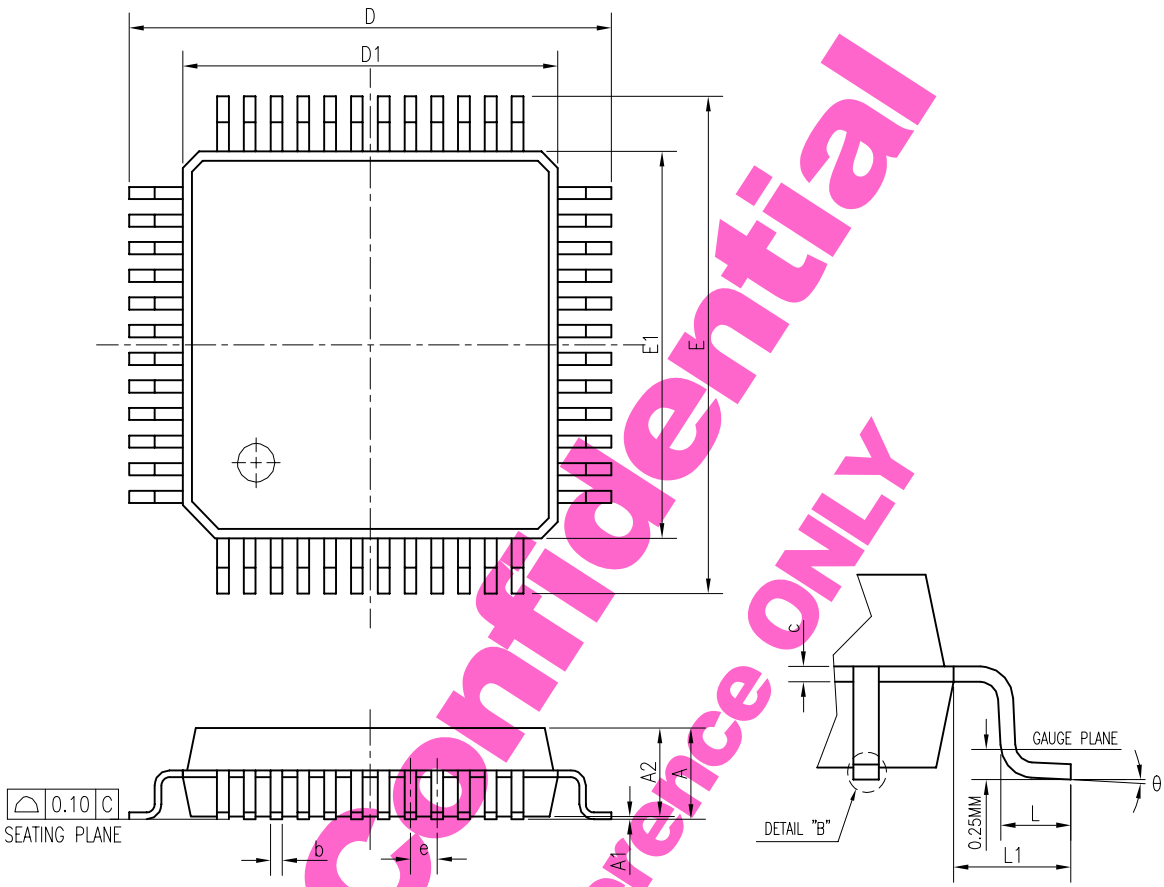
10-2 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

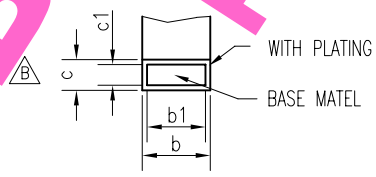
10-3 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11 Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



DETAIL "B"

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
48L	0.17	0.22	0.27	0.17	0.20	0.23		0.50 BSC.		MS-026 BBC

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