Data Sheet

BIT1612

10-Bit Digital Video Decoder
with
OSD and T-CON

Version: A0

在接觸此份文件之任何內容以前，請詳細閱讀下開聲明。一旦此份文件揭露予接收者，該接收者即被推定爲同意下開聲明。

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1 General Description

BIT1612 是結合 T-CON 與 OSD 的一個高性能單晶片數字式視訊解碼器。視訊解碼器解譯普遍使用的 NTSC/PAL/SECAM 影像內容。投向 BIT1612 的信號包括類比視訊 CVBS 和 Y/C、數字式 CCIR601/656 和數字式 RGB 格式。類比/數字轉換器的自動增益控制 (AGC) 功能加強了處理微弱和失真信號的能力。卓越的 2D 梳型濾波器和先進的 CTI 和 Skin-Tone 處理使顯示顏色更加清楚，圖像更加自然。可編程序的時序控制 (TCON) 讓 BIT1612 系統 (解析度可達 800xRGBx600) 可使用大多數普及的 LCD 屏。可編程序的亮度、對比和色飽和度以及內含的伽瑪校正讓用戶自由地調整顯示的顏色。嵌入式 OSD 使系統設計師非常容易開發出簡單易用使用者介面。先進的顯示格式控制器能非常順利地轉換 4:3 顯示成 16:9。BIT1612 可以用在一臺傳統手持式 LCD 顯示器。以其卓越的影像處理表現，使用在車用 TV/導航系統和便攜式的 AV 系統也是適當的。

2 Features

General:

- No external memory required
- Two 10-bit video CMOS Analog-to-Digital Converters (ADCs) in differential CMOS style for best S/N-performance
- Fully programmable static gain or automatic gain control (AGC) the selected CVBS or Y/C channel : 0~12db (Analog) and 0~18db (Digital)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- On-chip clock generator
- L-lock system clock frequencies
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal (24.576 MHz) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Accepts NTSC (J, M, 4.43), PAL (60, B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video signal
- User programmable luminance peaking or aperture correction
- Adaptive 3/5-line comb filter for two dimensional chrominance/luminance separation
- PAL delay line for correcting PAL phase errors
- Multi-standard VBI-data slicer including closed caption
- MV copy protection detection
- YUV to RGB color space converting
- Fully programmable zoom-out arbitrary ratio in both horizontal and vertical
- Anamorphic zoom for 4:3 video input to 16:9 display converting
- Embedded brightness, contrast, sharpness and gamma correction
- Embedded Skin-Tone and CTI
- Embedded programmable OSD for user Interface
- Embedded programmable TCON (Timing-Control) generator for LCD interface
- Embedded 3 PWM (Pulse Width Modulation) generators for general purpose control
- Embedded IR remote control decoder

Input:

- 3 analog inputs, internal analog source selectors, e.g. CVBS x 3 or Y/C x 1 or (Y/C x 1 and CVBS x 1) or YPbPr (480i or 576i)
- 3 of 8-bit digital video input ports (R,G,B)
- HSYNC/VSYNC Input x 1
- Clock Input x 2
- 24-bit RGB/YUV input up to 85MHz
- 16-bit RGB (RGB 5:6:5) input
- 8-bit Serial RGB Data format
- ITU-R BT.601(16-bit) (CCIR 601)
- ITU-R BT.656(8-bit) (CCIR 656)
- Built-in YUV to RGB color space converter

- Programmable RGB input port order and pin order
- 5V tolerance input pads support 5V/3.3V interface

Output:

- 4x8 Bits digital output ports (R,G,B,T)
- Programmable RGB output port order and pin order
- Maximum output pixel frequency 85MHz@ digital output
- Support inverse and frequency adjustment for LCD panel clock
- Support programmable H/V sync. for LCD panel
- Support programmable TCON for LCD panel
- Support Delta and Stripe types LCD panel
- Free-run Synchronization mode if sync signal disappeared

Interface:

- Support Two-wire BiTEKBus interface
- Support Two-Wire Serial Interface (TWSI) Bus interface
- Support 24Cxx serial EEPROM Script controller

OSD:

- Built-in OSD generator with 128 ROM fonts, 512 mix color
- 3 windows support overlay function
- 48 user download fonts
- 9 sizes of zooming font (1/2, x1, x2, x3, x4, x5, x6, x7, x8)
- Flashing font attribute
- Fringe font attribute
- Transparent overlay for OSD windows
- Support external OSD interface

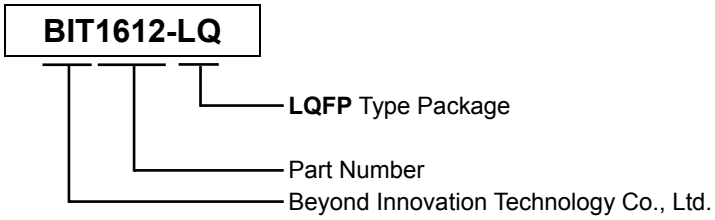
Power Management:

- 1.8V power source for core,
- 3.3V power source for output pads
- Power Consumption less than 300 mW

Package:

- LQFP 128 pins

3 Order Information



4 Block Diagram

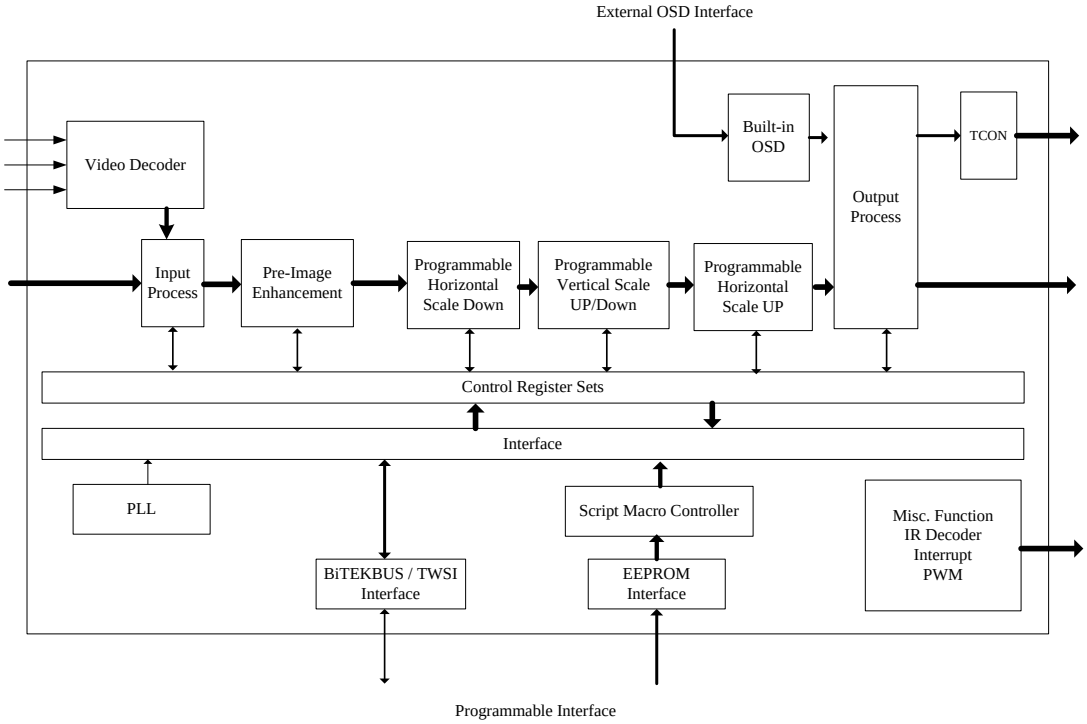


Figure 4-1 BIT1612 Architecture

5 Pin Definition

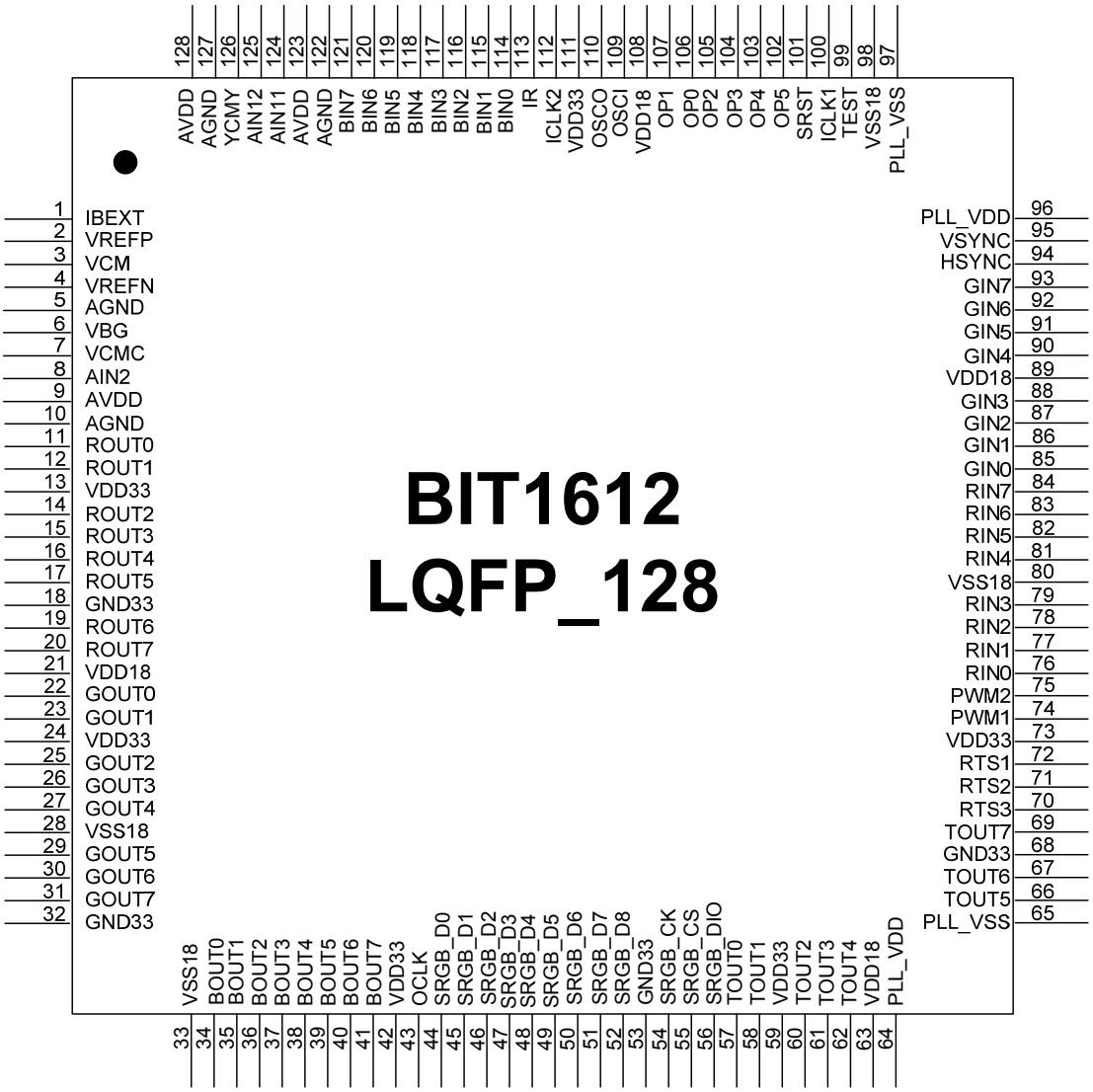


Figure 5-1 Pin Configuration

Table 5-1 BIT1612 Pin Definition

Pin Name	Pin #	Pin Type	Function Description	Pad Type
IBEXT	1	AIO	Monitor Internal Bias Current Generation or External Bypass for Use with Some Test Mode	
VREFP	2	AIO	Output for Decoupling or Bypass of Positive Internal Reference Voltage	
VCM	3	AIO	Output for Decoupling or Bypass Common Mode Voltage	
VREFN	4	AIO	Output for Decoupling or Bypass of Negative Internal Reference Voltage	
AGND	5	AG33	Analog Ground and Reference Generators	
VBG	6	AIO	Output for Decoupling or Bypass of Band-Gap Voltage	
VCMC	7	AI	Chroma Channel PGA Negative Reference Input	
AIN2	8	AI	ADC 2 Input (Y / CVBS)	
AVDD	9	AP33	AFE ADC Power (3.3V)	
AGND	10	AG33	AFE ADC GND (3.3V)	

ROUT0	11	O	ROUT[1] / ~VCOM / Raw Data[0] / GPO[0]	POT8
ROUT1	12	O	ROUT[2] / ~Q2H / Raw Data[1] / GPO[1]	POT8
VDD33	13	P33	IO Power (3.3V)	
ROUT2	14	O	ROUT[3] / STV2 / Raw Data[2]	POT8
ROUT3	15	O	ROUT[4] / STV1 / Raw Data[3]	POT8
ROUT4	16	O	ROUT[5] / CKV / Raw Data[4]	POT8
ROUT5	17	O	ROUT[6] / FRP / Raw Data[5]	POT8
GND33	18	G33	IO GND (3.3V)	
ROUT6	19	O	ROUT[7] / LD / Raw Data[6]	POT8
ROUT7	20	O	ROUT[8] / VCOM / Raw Data[7]	POT8
VDD18	21	P18	Core Power (1.8V)	
GOUT0	22	O	GOUT[1] / ~STV / Raw Data[8] / GPO[2]	POT8
GOUT1	23	O	GOUT[2] / ~STH / Raw Data[9] / GPO[3]	POT8
VDD33	24	P33	IO Power (3.3V)	
GOUT2	25	O	GOUT[3] / OEH / Raw Data[10]	POT8
GOUT3	26	O	GOUT[4] / STH2 / Raw Data[11]	POT8
GOUT4	27	O	GOUT[5] / STH1 / Raw Data[12]	POT8
VSS18	28	G18	Core GND (1.8V)	
GOUT5	29	O	GOUT[6] / Raw Data[13] / CPH1	POT8
GOUT6	30	O	GOUT[7] / Raw Data[14] / CPH2	POT8
GOUT7	31	O	GOUT[8] / Raw Data[15] / CPH3	POT8
GND33	32	G33	IO GND (3.3V)	
VSS18	33	G18	Core GND (1.8V)	
BOUT0	34	O	BOUT[1] / UD / Raw Data[16] / GPO[4]	POT8
BOUT1	35	O	BOUT[2] / RL / Raw Data[17] / GPO[5]	POT8
BOUT2	36	O	BOUT[3] / VCOM_SEL / Raw Data[18]	POT8
BOUT3	37	O	BOUT[4] / Raw Data[19] / SPI_CS	POT8
BOUT4	38	O	BOUT[5] / Raw Data[20] / SPI_DO	POT8
BOUT5	39	O	BOUT[6] / ~OEH / Raw Data[21] / SPI_CK	POT8
BOUT6	40	O	BOUT[7] / ~CKV / Raw Data[22]	POT8
BOUT7	41	O	BOUT[8] / ~LD / Raw Data[23]	POT8
VDD33	42	P33	IO Power (3.3V)	
OCLK	43	O	Clock Output	POT16
SRGB_D0	44	O	Serial RGB[0] / GPO[0]	POT4
SRGB_D1	45	O	Serial RGB[1] / GPO[1]	POT4
SRGB_D2	46	O	Serial RGB[2] / GPO[2]	POT4
SRGB_D3	47	O	Serial RGB[3] / GPO[3]	POT4
SRGB_D4	48	O	Serial RGB[4] / GPO[4]	POT4
SRGB_D5	49	O	Serial RGB[5] / GPO[5]	POT4
SRGB_D6	50	O	Serial RGB[6] / PWM2	POT4
SRGB_D7	51	O	Serial RGB[7] / PWM3	POT4
SRGB_D8	52	O	Serial RGB[8] / SPI_CK	POT4
GND33	53	G33	IO Power (3.3V)	
SRGB_CLK	54	O	DAC CLOCK	POT4
SRGB_CS	55	O	BIT1690_INF.CS / SPI_CS	POT4
SRGB_DIO	56	IO	BIT1690_INF.DIO / SPI_DO	PB4
TOUT0	57	I/O	KEY[0] / STH2 / Raw Data[24]	PBCU8
TOUT1	58	I/O	KEY[1] / STH1 / Raw Data[25]	PBCU8
VDD33	59	P33	IO Power (3.3V)	
TOUT2	60	I/O	KEY[2] / STV2 / Raw Data[26]	PBCU8
TOUT3	61	I/O	KEY[3] / STV1 / Raw Data[27]	PBCU8
TOUT4	62	I/O	KEY[4] / VCOM_SEL / Raw Data[28]	PBCU8
VDD18	63	P18	Core Power (1.8V)	
PLLAVDD	64	AP18	PLL Power (1.8V) – Panel Clock PLL	
PLLAVSS	65	AG18	PLL GND (1.8V) – Panel Clock PLL	

TOUT5	66	I/O	KEY[5] / CKV / Raw Data[29]	PBCU8
TOUT6	67	I/O	KEY[6] / LD / Raw Data[30]	PBCU8
GND33	68	G33	IO GND (3.3V)	
TOUT7	69	I/O	KEY[7] / OEH / Raw Data[31]	PBCU8
RTS3	70	O	Multi – Function Output	POT8
RTS2	71	O	Multi – Function Output	POT8
RTS1	72	O	Multi – Function Output	POT8
VDD33	73	P33	IO Power (3.3V)	
PWM1	74	O	PWM1 / GPO[6]	POT16
PWM2	75	O	PWM2 / GPO[7]	POT16
RIN0	76	I	RIN[1] / KEY[0]	PICD
RIN1	77	I	RIN[2] / KEY[1]	PICD
RIN2	78	I	RIN[3] / KEY[2]	PICD
RIN3	79	I	RIN[4] / KEY[3]	PICD
VSS18	80	G18	Core GND (1.8V)	
RIN4	81	I	RIN[5] / KEY[4]	PICD
RIN5	82	I	RIN[6] / KEY[5]	PICD
RIN6	83	I	RIN[7] / KEY[6]	PICD
RIN7	84	I	RIN[8] / KEY[7]	PICD
GIN0	85	I	GIN[0] / EXT_OSD_R	PICD
GIN1	86	I	GIN[1] / EXT_OSD_G	PICD
GIN2	87	I	GIN[2] / EXT_OSD_B	PICD
GIN3	88	I	GIN[3] / EXT_OSD_Blank	PICD
VDD18	89	P18	Core Power (1.8V)	
GIN4	90	IO	GIN[4] / EXT_OSD_HS	PBCD4
GIN5	91	IO	GIN[5] / EXT_OSD_VS	PBCD4
GIN6	92	IO	GIN[6] / EXT_OSD_CLK	PBCD4
GIN7	93	I	GIN[7] / VPG_In	PICD
HSYNC	94	I	HSYNC Input / KEY[1]	PICD
VSYNC	95	I	VSYNC Input / KEY[0]	PICD
PLLAVDD	96	AP18	PLL Power (1.8V) – AFE PLL	
PLLAVSS	97	AG18	PLL GND (1.8V) – AFE PLL	
VSS18	98	G18	Core GND (1.8V)	
TEST	99	I	Test Mode	PID
ICLK1	100	I	Clock 1 Input	PIS
SRST	101	I	System Reset, Low Active	PIU
OP5	102	I	Option[5]	PIU
OP4	103	I	Option[4]	PID
OP3	104	IO	SDA2 / Slave Address[1]	PB4
OP2	105	IO	SCL2 / Slave Address[0]	PB4
OP0	106	IO	SDA (Master and Slave)	PB4
OP1	107	IO	SCL (Master and Slave)	PB4
VDD18	108	G18	Core Power (1.8V)	
OSCI	109	I	Oscillator Input	
OSCO	110	O	Oscillator Output	
VDD33	111	P33	IO Power (3.3V)	
ICLK2	112	I	Clock 2 Input	PIS
IR	113	I	Infrared Decoder Input	PICU
BIN0	114	I	BIN[0] / KEY_IN[0]	PICU
BIN1	115	I	BIN[1] / KEY_IN[1]	PICU
BIN2	116	I	BIN[2] / KEY_IN[2]	PICU
BIN3	117	I	BIN[3] / KEY_IN[3]	PICU
BIN4	118	I	BIN[4] / KEY_IN[4]	PICU
BIN5	119	I	BIN[5] / KEY_IN[5]	PICU
BIN6	120	I	BIN[6] / KEY_IN[6]	PICU

BIN7	121	I	BIN[7] / KEY_IN[7]	PICU
AGND	122	AG33	AFE GND (3.3V)	
AVDD	123	AP33	AFE Power (3.3V)	
AIN11	124	AI	ADC 1 Channel 1 (Pb / CVBS)	
AIN12	125	AI	ADC 1 Channel 2 (Pr / CVBS)	
VCMY	126	AI	Luma Composite Channel PGA Negative Reference Input	
AGND	127	AG33	AFE Band Gap GND (3.3V)	
AVDD	128	AP33	AFE Band Gap Power (3.3V)	

Table 5-2 PAD Type Definition

Pad Type	Function
POT4	Controllable Tri-state and 4mA Output Pad Type
POT8	Controllable Tri-state and 8mA Output Pad Type
POT16	Controllable Tri-state and 16mA Output Pad Type
PICD	Controllable Pull-Down Input Pad Type
PB4	No Pull-Up and Pull-Down Input and 4mA Output Bidirectional Pad Type
PIU	Pull-Up Input Pad Type
PID	Pull-Down Input Pad Type
PIS	Schmitt Trigger Input Pad Type
PBCU4	Controllable Pull-Up Input and 4mA Output Bidirectional Pad Type
PBCU4	Controllable Pull-Up Input and 8mA Output Bidirectional Pad Type
PBCD4	Controllable Pull-Down Input and 4mA Output Bidirectional Pad Type

6 Functional Description

6.1 Version Control

BIT1612 內部提供硬體版本資訊及軟體版本資訊，兩組 Register 作爲版本控管使用，相關 Register 請參考下表。

Table 6-1 Version Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_HW_VER	0x000	R	8	[1:0] Product version [4:2] Product Number [7:5] Product Group	0xAC
R_SW_VER	0x001	RW	8	Software Version Control	0x00

6.2 Interrupt Function

BIT1612 Interrupt Function提供INT Pin (共有Pin 72、 Pin 71 和Pin 70，R_RTSx_SEL = 0x0B) 作爲Interrupt Trigger Output (請參考"6.10 Special Output Setup"小節的說明)，經由Register可設定爲Edge or Level trigger output。當Level Trigger時並可設定爲High or Low Active，若爲Edge Trigger時則可設定爲Falling or Rising Active。其Interrupt架構採用三層架構 (FLAG、ACK and MASK)，架構請參考Figure 6-1。BIT1612 提供 8 個Interrupt Flags 和 12 個 Interrupt Sources請參考下表 Table 6-2，相關Registers設定請參考 Table 6-3 和 Table 6-4。

Table 6-2 Interrupt Source and Flags

Interrupt Source	Bit	Function		
R_HASSIG_FLAG	0	R_INTSIGIN_SEL (0x0FB[5]) = 0		Active when Input HSYNC Has Some Changes in 2047 XCLKs
		R_INTSIGIN_SEL (0x0FB[5]) = 1		Active when Video Decoder Lock Selected Source (HLCK & SYNC_RDY & STD_RDY & AGC1_RDY & AGC2_RDY) (see Table 6-4)
R_NOSIG_FLAG	1	R_INTSIGIN_SEL (0x0FB[5]) = 0		Active when Input HSYNC Has No Change in 2047 XCLKs
		R_INTSIGIN_SEL (0x0FB[5]) = 1		Active when Video Decoder Un-Lock Selected Source (HLCK & SYNC_RDY & STD_RDY & AGC1_RDY & AGC2_RDY) (see Table 6-4)
R_MODE_FLAG	2	R_INTMODECHG_SEL (0x0FB[6]) = 0		Active when Input VSYNC Variation Larger than 8 HSYNCs
		R_INTMODECHG_SEL (0x0FB[6]) = 1		Active when Video Decoder FIDT (50Hz/60Hz) Changes
R_VSYNC_FLAG	3	Active when Selected VSYNC Falling Edge Occurs		
		R_INTVS_POL (0x005[4]) = 0		VSYNC Normal
		R_INTVS_POL (0x005[4]) = 1		VSYNC Invert
R_ERROR1_FLAG	4	R_INT_ERRSEL (0x006[4]) = 0		Active when Timer 0 Overflow
		R_INT_ERRSEL (0x006[4]) = 1		Active when Line Buffer Error Type 1 Occurs
R_ERROR2_FLAG	5	VP	R_INT_ERRSEL (0x006[4]) = 0	Active when Timer 1 Overflow
			R_INT_ERRSEL (0x006[4]) = 1	Active when Line Buffer Error Type 2 Occurs
		VD	From SRC2 (AIN2) or SRC12 (AIN12) or SRC11 (AIN11) (see Table 6-4)	
R_MVCC_FLAG	6	MV or CC Detection (see Table 6-4)		
R_IRKEY_FLAG	7	Active when IR Remote Control Detection is Ready or Active when GPI (General Purpose Input) Status Changes		

Table 6-3 Interrupt Controller Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_INT_FLAG	0x002[7:0]	R	8	Interrupt Flag 0: Nothing 1: Interrupt Event Occurs	-
R_INT_MASK	0x003[7:0]	RW	8	Interrupt MASK (see Figure 6-1) 0: Interrupt Mask Off (Enable Interrupt) 1: Interrupt Mask On (Disable Interrupt)	0x00
R_INT_ACK	0x004[7:0]	RW	8	Interrupt ACK (see Figure 6-1) 0: Clear Interrupt Flag and Disable Interrupt 1: Enable Interrupt	0x00
R_INT_TYPE	0x005[0]	RW	1	Interrupt TYPE 0: Level Type 1: Edge Type	0
R_POL_INT	0x005[1]	RW	1	Interrupt Polarity 0: High Level Active (Level Type) 0: Rising Edge Active (Edge Type) 1: Low Level Active (Level Type) 1: Falling Edge Active (Edge Type)	0
R_INTSIGIN_SEL	0x0FB[5]	RW	1	Interrupt Vector[0] and Vector[1] Source Selection 0: From VP 1: From VD	0
R_INTMODECHG_SEL	0x0FB[6]	RW	1	Interrupt Vector[2] Source Selection 0: From VP 1: From VD	0
R_INT_VSSE	0x005[3:2]	RW	2	Interrupt Vector[3] Source Selection 00: VSYNC from Input VSYNC Source 01: VSYNC from Output VSYNC Source 10: VSYNC from VD VSYNC Source 11: VSYNC Source Active when TWSI Detection Occurs.	00
R_INTVS_POL	0x005[4]	RW	1	Interrupt Vector[3] Polarity Selection 0: Normal 1: Invert	0
R_VP_ERR2_EN	0x006[3]	RW	1	Interrupt Vector[5] VP Error Source Enable 0: Disable 1: Enable	0
R_INT_ERRSEL	0x006[4]	RW	1	Interrupt Vector[4] and Vector[5] Source Selection 0: From Timer Overflow 1: From Line Buffer Error	0
R_ERROR_TYPE	0x006[5]	RW	1	Line Buffer Error Detection Selection 0: ODD Field 1: EVEN Field	0
R_IHSPS_SEL	0x04D[7]	RW	1	IHS Pulse Width Selection 0: Type 0 1: Type 1	0

Table 6-4 Video Decoder Lock Source for Interrupt Selection					
Mnemonic	Address	R/W	Bits	Description	Default
R_INTHLCK_EN	0x0FB[0]	RW	1	HLCK Detection Enable 0: Disable 1: Enable	0

R_INTSYNCRDY_EN	0x0FB[1]	RW	1	Sync Ready Detection Enable 0: Disable 1: Enable	0
R_INTSTDRDY_EN	0x0FB[2]	RW	1	Standard Ready Detection Enable 0: Disable 1: Enable	0
R_INTAGC1_EN	0x0FB[3]	RW	1	AGC1 Ready Detection Enable 0: Disable 1: Enable	0
R_INTAGC2_EN	0x0FB[4]	RW	1	AGC2 Ready Detection Enable 0: Disable 1: Enable	0
R_INTSRC2_EN	0x006[0]	RW	1	SRC2 (AIN2) Detection Enable 0: Disable 1: Enable	0
R_INTSRC12_EN	0x006[1]	RW	1	SRC12 (AIN12) Detection Enable 0: Disable 1: Enable	0
R_INTSRC11_EN	0x006[2]	RW	1	SRC11 (AIN11) Detection Enable 0: Disable 1: Enable	0
R_INTMV_EN	0x006[6]	RW	1	MV Detection Enable 0: Disable 1: Enable	0
R_INTCC_EN	0x006[7]	RW	1	CC Detection Enable 0: Disable 1: Enable	0

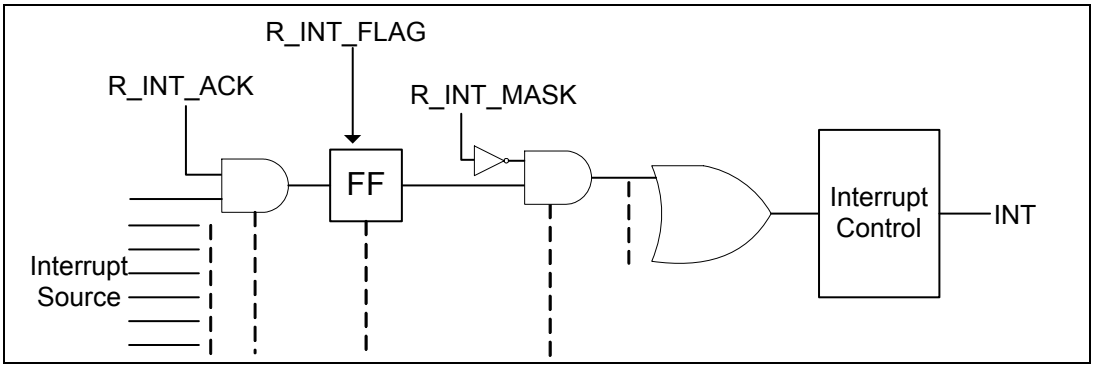


Figure 6-1 Interrupt Function Block

6.3 Double Buffer

BIT1612 在Scaling Factor (0x05F~0x061,0x067) 和Display Windows Setup (0x052~0x057) 提供Double Buffer Register，提供給使用者針對這些Registers可以做Parallel Update，其相關架構請參考 Figure 6-2，相關Registers設定請參考 Table 6-5。

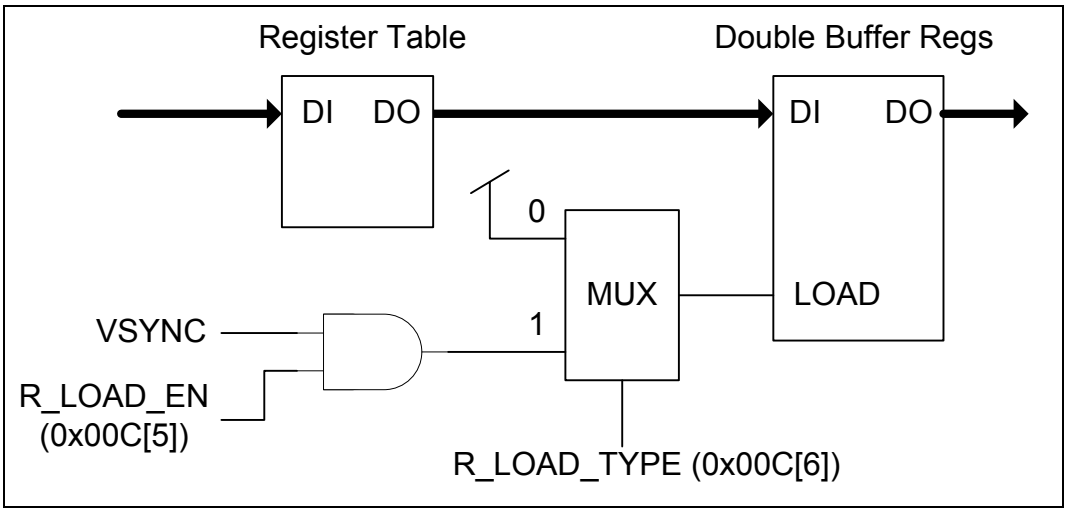


Figure 6-2 Double Buffer Function

Table 6-5 Double Buffer Register

Mnemonic	Address	R/W	Bits	Description	Default
R_LOAD_EN	0x00C[5]	RW	1	Double Buffer Load Enable 0: Nothing 1: Load	1
R_LOAD_TYPE	0x00C[6]	RW	1	Double Buffer Register Update Type 0: Immediately 1: Control by R_LOAD_EN	0

6.4 Pad Type Setup

BIT1612 輸出的 PAD 可設定爲 Tri-State 輸出，而輸入的 PAD 尚可控制其內建之 Pull-Up or Pull-Down 電阻導通或關閉，相關 Registers 設定請參考下表。

Table 6-6 Output Tri-State Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ROUT_TRI	0x007[0]	RW	1	ROUT Port Tri-State Enable	1
R_GOUT_TRI	0x007[1]	RW	1	GOUT Port Tri-State Enable	1
R_BOUT_TRI	0x007[2]	RW	1	BOUT Port Tri-State Enable	1
R_TOUT_TRI	0x007[3]	RW	1	TOUT Port Tri-State Enable	1
R_OCLK_TRI	0x007[4]	RW	1	OCLK (43) Pin Tri-State Enable	1
R_PWM1_TRI	0x007[5]	RW	1	PWM1 (74) Pin Tri-State Enable	1
R_PWM2_TRI	0x007[6]	RW	1	PWM2 (75) Pin Tri-State Enable	1
R_SRGB_TRI	0x007[7]	RW	1	SRGB Port Tri-State Enable 1 ➔ Tri-State, 0 ➔Normal	0

Table 6-7 Pad Pull Up or Down Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BIN_REN	0x0FD[7:0]	RW	8	BIN[7:0] Port Pull-Down Resistance On/Off	0x00
R_TOUT_REN	0x0FE[7:0]	RW	8	TOUT[7:0] Port Pull-Up Resistance On/Off	0xFF
R_RIN_REN	0x0FF[0]	RW	1	RIN[7:0] Port Pull-Down Resistance On/Off	0
R_GIN_REN	0x0FF[1]	RW	1	GIN[7] Pin Pull-Down Resistance On/Off	0
R_GIN1_REN	0x0FF[2]	RW	1	GIN[6:0] Port Pull-Down Resistance On/Off	0
R_SYNC_REN	0x0FF[3]	RW	1	HSYNC/VSYNC Pins Pull-Down Resistance On/Off	0
R_IR_REN	0x0FF[4]	RW	1	IR (Pin 113) Pin Pull-Down Resistance On/Off 1 ➔ Off, 0 ➔On	0

6.5 GPO (General Purpose Output) Function

BIT1612 內部提供 8 個GPO Register control輸出、其可分別規劃爲High Level、Low Level、Tri-State和Status 四種狀態。其相關Registers設定請參考 Table 6-8 和 Table 6-9。

Table 6-8 General Purpose Output Register

Mnemonic	Address	R/W	Bits	Description	Default
R_GPO_SEL	0x008[7:0]	RW	8	GPO Port Enable 0: Disable 1: Enable	0x00
R_GPO_TYPE	0x009[7:0]	RW	8	GPO Port Type 0: Normal 1: Tri-State	0xFF
R_GPO_REG	0x00A[7:0]	RW	8	GPO Port Value 0: Low Level 1: High Level	0x00

Table 6-9 General Purpose Output Pads Setup Table

GPO Pin Name/ No.	Output Pin	Register Recommended Setting
GPO[0]	SRGB_D0(44)	R_GPO_OUT (0x13C[5]) = 1
GPO[1]	SRGB_D1(45)	R_GPO_OUT (0x13C[5]) = 1
GPO[2]	SRGB_D2(46)	R_GPO_OUT (0x13C[5]) = 1
GPO[3]	SRGB_D3(47)	R_GPO_OUT (0x13C[5]) = 1
GPO[4]	SRGB_D4(48)	R_GPO_OUT (0x13C[5]) = 1
GPO[5]	SRGB_D5(49)	R_GPO_OUT (0x13C[5]) = 1
GPO[6]	PWM1(74)	R_GPO_SEL[6] = 1
GPO[7]	PWM2(75)	R_GPO_SEL[7] = 1
GPO[0]	ROUT[0](11)	R_GPO_SEL[0] = 1
GPO[1]	ROUT[1](12)	R_GPO_SEL[1] = 1
GPO[2]	GOUT[0](22)	R_GPO_SEL[2] = 1
GPO[3]	GOUT[1](23)	R_GPO_SEL[3] = 1
GPO[4]	BOUT[0](34)	R_GPO_SEL[4] = 1
GPO[5]	BOUT[1](35)	R_GPO_SEL[5] = 1

6.6 System Enable and Reset

BIT1612 可以從外部SRST PIN (Pin 101) 輸入一個大於 16 個XCLK Cycles的Low訊號，BIT1612 將被強制 Reset 回到Power On 時的狀態。相關波形請參考 Figure 6-3。

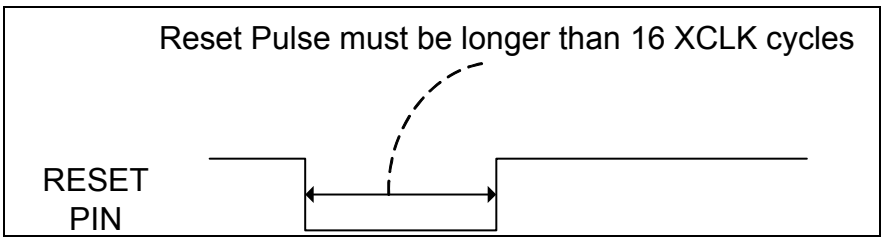


Figure 6-3 Hardware Reset Waveform

6.7 Clock Domain Systems

BIT1612 內部存在五個 Clock Domain：

1. PCLK Domain: Source Clock
2. LCLK Domain: Output Clock
3. XCLK Domain: System Clock
4. MCLK Domain: Image Clock
5. TCLK Domain: Panel Clock

相關Registers設定請參考 Table 6-10。

注意事項：XCLK Domain 頻率必須比 LCLK Domain 低。

Table 6-10 Clock Domain System Register

Mnemonic	Address	R/W	Bits	Description	Default
R_XCLK_SEL	0x00B[6:4]	RW	3	XCLK Domain Clock Source Selection XCLK = OSCCLK / (2^R_XCLK_SEL)	000
R_TCLK_SEL	0x00C[2:0]	RW	3	TCLK Domain Clock Source Selection 000: PLLCLK 001: OSCCLK 010: ICLK1 011: ICLK2 1xx: VDCLK	001
R_TCLK_POL	0x00C[3]	RW	1	TCLK Domain Polarity 0: Normal. 1: Invert.	0
R_TCLK_EN	0x00C[4]	RW	1	TCLK Domain Enable 0: Disable. 1: Enable.	1
R_LCLK_SEL	0x00D[5:4]	RW	2	LCLK Domain Clock Source Selection 00: Normal Clock (Freq. equals to LCLK) 01: Phase 1 Clock (Freq. equals to LCLK/3) 10: Phase 2 Clock (Freq. equals to LCLK/3) 11: Phase 3 Clock (Freq. equals to LCLK/3)	10
R_LCLK_POL	0x00D[6]	RW	1	LCLK Domain Polarity 0: Normal 1: Invert	0
R_LCLK_EN	0x00D[7]	RW	1	LCLK Domain Enable 0: Disable 1: Enable	1
R_MCLK_SEL	0x00E[1:0]	RW	2	MCLK Domain Clock Source Selection MCLK = PCLK / (R_MCLK_MODE+1)	01
R_MCLK_POL	0x00E[2]	RW	1	MCLK Domain Polarity 0: Normal 1: Invert	1
R_MCLK_EN	0x00E[3]	RW	1	MCLK Domain Enable 0: Disable 1: Enable	1
R_PCLK_SEL	0x00E[5:4]	RW	2	PCLK Domain Clock Source Selection 00: ICLK1 01: ICLK2 1x: VDCLK	00
R_PCLK_POL	0x00E[6]	RW	1	PCLK Domain Polarity 0: Normal 1: Invert	1
R_PCLK_EN	0x00E[7]	RW	1	PCLK Domain Enable 0: Disable	1

				1: Enable	
R_DACCLK_EN	0x00B[2]	RW	1	DAC Clock Domain Enable 0: Disable 1: Enable	1
R_DACCLK_POL	0x00B[3]	RW	1	DAC Clock Domain Polarity 0: Normal 1: Invert	1
R_LCLK_4X	0x00B[7]	RW	1	LCLK x 4 Enable 0: Disable 1: Enable	0
R_LINEBUF_CKEN	0x00D[1]	RW	1	LINEBUF Clock Enable 0: Disable 1: Enable	1
R_REGS_CKEN	0x00D[2]	RW	1	Registers set Clock Enable 0: Disable 1: Enable	1
R_VDCLK_SEL	0x00D[3]	RW	1	VD Clock Domain Clock Source Selection 0: From 27MHz 1: From 13.5MHz	1
R_AFEBUF_SEL	0x00F[6]	RW	1	AFE Buffer Clock Domain Clock Source Selection 0: From DVPCLK. 1: From AFECLK	1
R_AFEBUF_POL	0x00F[7]	RW	1	AFE Buffer Clock Domain Polarity 0: Normal 1: Invert	1
R_AFECLK_SEL	0x00F[4]	RW	1	AFE Clock Domain Clock Source Selection 0: From 27MHz 1: From 13.5MHz	0
R_AFECLK_POL	0x00F[5]	RW	1	AFE Clock Domain Polarity 0: Normal 1: Invert	1
R_AFECLK_EN	0x00F[3]	RW	1	AFE Clock Domain Enable 0: Disable 1: Enable	1
R_DVPCLK_SEL	0x00F[1]	RW	1	DVP Clock Domain Clock Source Selection 0: From PLL 1: From OSC	0
R_DVPCLK_POL	0x00F[2]	RW	1	DVP Clock Domain Polarity 0: Normal 1: Invert	1
R_DVPCLK_EN	0x00F[0]	RW	1	DVP Clock Domain Enable 0: Disable 1: Enable	1
R_CLK27_POL	0x0EF[0]	RW	1	CLK27 Domain Polarity 0: Normal 1: Invert	0
R_CLK27_EN	0x0EF[1]	RW	1	CLK27 Domain Enable 0: Disable 1: Enable	1
R_LN5CLK_POL	0x0F7[4]	RW	1	Line Buffer Clock 5 Polarity 0: Normal 1: Invert	0
R_LN4CLK_POL	0x0F7[3]	RW	1	Line Buffer Clock 4 Polarity 0: Normal 1: Invert	0

R_LN3CLK_POL	0x0F7[2]	RW	1	Line Buffer Clock 3 Polarity 0: Normal 1: Invert	0
R_LN2CLK_POL	0x0F7[1]	RW	1	Line Buffer Clock 2 Polarity 0: Normal 1: Invert	0
R_LN1CLK_POL	0x0F7[0]	RW	1	Line Buffer Clock 1 Polarity 0: Normal 1: Invert	0

6.8 Panel Timing Setup

BIT1612 可分別針對Auto Switch所設定的顯示模式，分爲Mode 0/1 兩組自動切換Panel Timing設定值，其相關設定Register請參考 Table 6-11 所列，相對應之輸出波形請參考 Figure 6-4。

Table 6-11 Panel Timing Setup Register

Mnemonic	Address	R/W	Bits	Description	Default
R_OS_XP	0x013[0], 0x010[7:0]	RW	9	HSYNC Pulse Width	0x010
R_OS_XS	0x013[1], 0x011[7:0]	RW	9	Active Window Horizontal Start Position	0x020
R_OS_XW	0x013[6:4], 0x012[7:0]	RW	11	Active Window Horizontal End Position	0x200
R_OS_XT_M0	0x016[2:0], 0x014[7:0]	RW	11	Horizontal Total Length on Auto Switch Mode 0	0x326
R_OS_XT_M1	0x016[6:4], 0x015[7:0]	RW	11	Horizontal Total Length on Auto Switch Mode 1	0x29D
R_OS_YP	0x017[7:0]	RW	8	VSYNC Pulse Width	0x02
R_OS_YS	0x018[7:0]	RW	8	Active Window Vertical Start Position	0x05
R_OS_YW	0x01B[1:0], 0x019[7:0]	RW	10	Active Window Vertical End Position	0x0F0
R_OS_YT	0x01B[3:2], 0x01A [7:0]	RW	10	Vertical Total Length	0x0F4

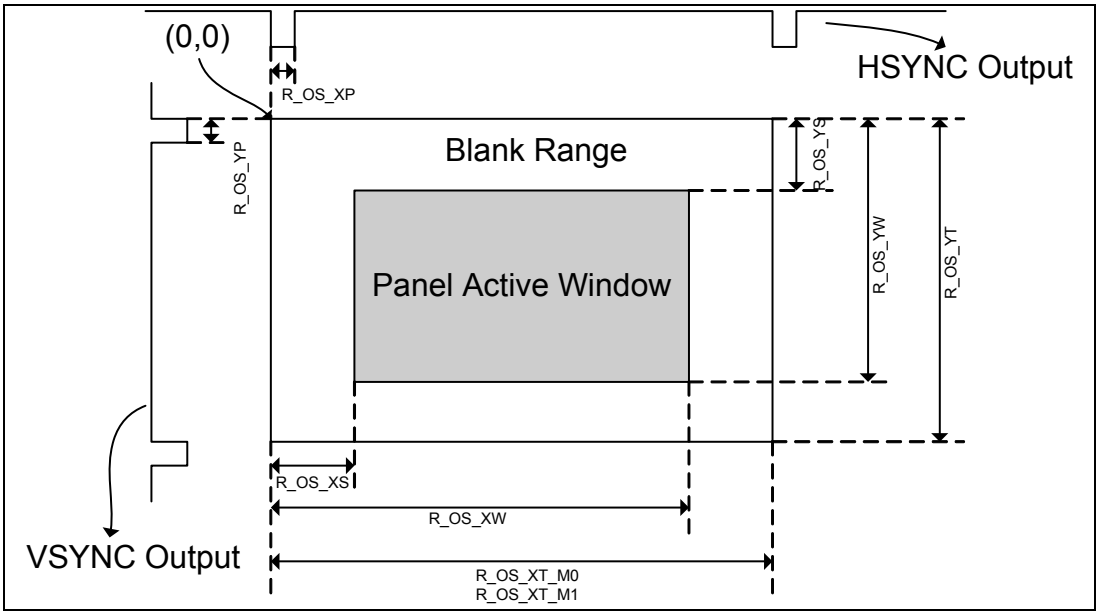


Figure 6-4 Panel Timing Setup

6.9 Output Data Path

BIT1612 可針對輸出的Data Bus分別做Invert、Rotate和Swap的處理，其相關Registers設定請參考 Table 6-12，相對應方塊圖請參考 Figure 6-5。

Table 6-12 Output Data Path Register

Mnemonic	Address	R/W	Bits	Description	Default
R_POL_ROUT	0x01C[0]	RW	1	R Data Output Polarity ➔ 0: Normal 1: Invert	0
R_POL_GOUT	0x01C[1]	RW	1	G Data Output Polarity ➔ 0: Normal 1: Invert	0
R_POL_BOUT	0x01C[2]	RW	1	B Data Output Polarity ➔ 0: Normal 1: Invert	0
R_POL_OCLK	0x01C[3]	RW	1	Output Clock Polarity ➔ 0: Normal 1: Invert	0
R_ROL_ROUT	0x01C[4]	RW	1	R Data Rotate ➔ 0: Disable 1: Enable	0
R_ROL_GOUT	0x01C[5]	RW	1	G Data Rotate ➔ 0: Disable 1: Enable	0
R_ROL_BOUT	0x01C[6]	RW	1	B Data Rotate ➔ 0: Disable 1: Enable	0
R_DLYE_OR	0x01D[0]	RW	1	R Channel Output Delay 1 Clock on Swap Source = 0	0
R_DLYE_OG	0x01D[1]	RW	1	G Channel Output Delay 1 Clock on Swap Source = 0	0
R_DLYE_OB	0x01D[2]	RW	1	B Channel Output Delay 1 Clock on Swap Source = 0	0
R_ZERO2_EN	0x01D[3]	RW	1	Data Tie to Zero after Gamma 0: Disable 1: Enable	0
R_DLYO_OR	0x01D[4]	RW	1	R Channel Output Delay 1 Clock on Swap Source = 1	0
R_DLYO_OG	0x01D[5]	RW	1	G Channel Output Delay 1 Clock on Swap Source = 1	0
R_DLYO_OB	0x01D[6]	RW	1	B Channel Output Delay 1 Clock on Swap Source = 1 0: Disable 1: Enable	0
R_6BITS_EN	0x01D[7]	RW	1	Data Bus Rotate Mode 0: 8 Bits 1: 6 Bits	0
R_SWAPE_OGB	0x01E[0]	RW	1	G Data Output Swap with B Data Output on Swap Source = 0 0: Swap Disable 1: Swap Enable	1
R_SWAPE_ORG	0x01E[1]	RW	1	R Data Output Swap with G Data Output on Swap Source = 0 0: Swap Disable 1: Swap Enable	0
R_SWAPE_ORB	0x01E[2]	RW	1	R Data Output Swap with B Data Output on Swap Source = 0 0: Swap Disable 1: Swap Enable	1
R_ZERO1_EN	0x01E[3]	RW	1	Data Tie to Zero before Gamma 0: Disable 1: Enable	0
R_SWAPO_ORB	0x01E[6]	RW	1	R Data Output Swap with B Data Output on Swap Source = 1 0: Swap Disable 1: Swap Enable	0
R_SWAPO_ORG	0x01E[5]	RW	1	R Data Output Swap with G data Output on Swap Source = 1 0: Swap Disable 1: Swap Enable	0
R_SWAPO_OGB	0x01E[4]	RW	1	G Data Output Swap with B Data Output on Swap Source = 1 0: Swap Disable 1: Swap Enable	0
R_SWAP_SRC	0x01E[7]	RW	1	Even / Odd Swap Source 0: Q2H 1: VCOM	0

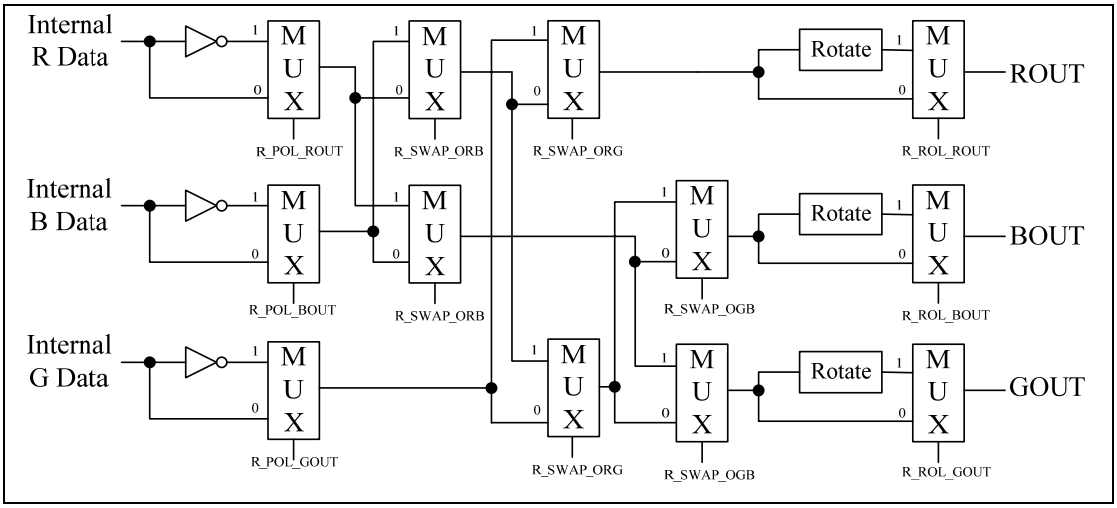


Figure 6-5 Output Data Path Selection

6.10 Special Output Setup

BIT1612 提供 3 組Special Output Pads (RTS1 (Pin 72)、RTS2 (Pin 71) 和RTS3 (Pin 70))，可經由Register分別設定特定輸出功能，其相關Registers設定及其意義請參考 Table 6-13。

R_RTS1_SEL = { 0x020[4], 0x01F[3:0] }, Default = 0x0F.

R_RTS2_SEL = { 0x020[5], 0x01F[7:4] }, Default = 0x0F.

R_RTS3_SEL = { 0x020[6], 0x020[3:0] }, Default = 0x0F.

Table 6-13 Special Output Setup

Mnemonic	R/W	Bits	Description	
R_RTSx_SEL	RW	5	0_0000: Output HSYNC Signal	1_0000: Inverse (HSYNC)
			0_0001: Output HREF Signal	1_0001: Inverse (HREF)
			0_0010: Output VSYNC Signal	1_0010: Inverse (VSYNC)
			0_0011: Output VREF Signal	1_0011: Inverse (VREF)
			0_0100: Output Data Enable Signal	1_0100: Inverse (DE)
			0_0101: Output EVEN/ODD Signal	1_0101: Inverse (EVEN/ODD)
			0_0110: STH	1_0110: Inverse (STH)
			0_0111: STV	1_0111: Inverse (STV)
			0_1000: Mode Type	1_1000: Inverse (Mode Type)
			0_1001: Auto-On	1_1001: Inverse (Auto-On)
			0_1010: Write Protect	1_1010: Inverse (Write Protect)
			0_1011: INT_O	1_1011: Inverse (INT_O)
			0_1100: GPO[7]	1_1100: Inverse (GPO[7])
			0_1101: PWMx	1_1101: Inverse (PWMx)
			0_1110: GND	1_1110: VDD
			0_1111: Tri-State	1_1111: Tri-State

6.11 Special Timing Adjustment

BIT1612 可針對不同的 Panel Timing 做微調設定，在 Timing 調整上特別提供兩種模式設定，以符合各類 panel 的需求。

6.11.1 Synchronization Timing

在這個模式下的 VSYNC 輸出將會與輸入訊號 VSYNC 同步。

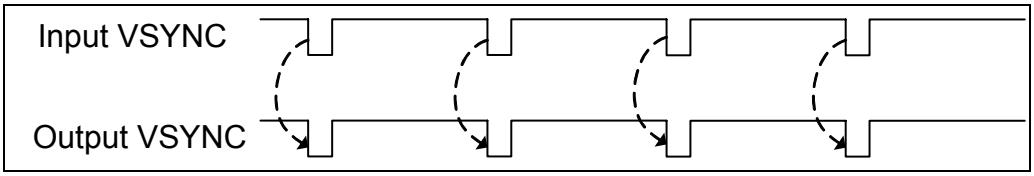


Figure 6-6 Synchronization Timing

6.11.2 Two-Fields Synchronization Timing

在這個模式下的 VSYNC 輸出，將同時受控於所設定欲同步之 EVEN 或 ODD Field VSYNC 和 R_OS_YT (0x01B[3:2], 0x01A[7:0])。

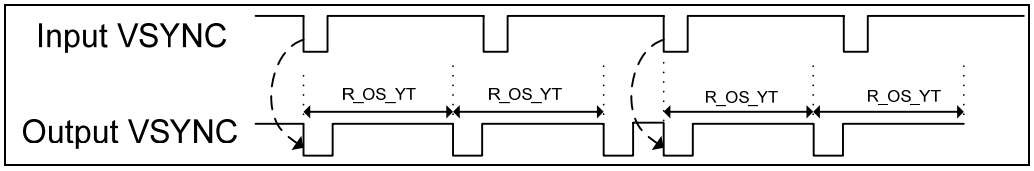


Figure 6-7 Two-Fields Synchronization Timing

其相關 Registers 設定及其意義請參考下表。

Table 6-14 Special Timing Adjust Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PROTECT_MODE	0x01B[4]	RW	1	Minimum Output Lines Protection 0: Disable 1: Enable	0
R_SYNCO_MODE	0x01B[5]	RW	1	Two-Field Synchronization Mode Selection 0: EVEN Field Synchronize 1: ODD Field Synchronize	0
R_SYNCO_EN	0x01B[6]	RW	1	Sync. With Input VSYNC Enable 0: Two-Field Synchronization Mode 1: Synchronization Mode	1

6.12 TCON Function

BIT1612 內建 Programmable TCON Function 將可經由 BIT1612 直接驅動 Analog Interface Panels，其相關 Registers 設定請參考下表。

Table 6-15 TCON Function Register

Mnemonic	Address	R/W	Bits	Description	Default
R_STH_START	0x023[6:4], 0x021[7:0]	RW	11	STH Signal Start	0x025
R_STH_END	0x023[2:0], 0x022[7:0]	RW	11	STH Signal End	0x026
R_LD_START	0x026[6:4], 0x024[7:0]	RW	11	LD Signal Start	0x001
R_LD_END	0x026[2:0], 0x025[7:0]	RW	11	LD Signal End	0x037
R_CKV_START	0x029[6:4], 0x027[7:0]	RW	11	CKV Signal Start	0x027
R_CKV_END	0x029[2:0], 0x028[7:0]	RW	11	CKV Signal End	0x051
R_OEH_START	0x02C[6:4], 0x02A[7:0]	RW	11	OEH Signal Start	0x014
R_OEH_END	0x02C[2:0], 0x02B[7:0]	RW	11	OEH Signal End	0x015
R_VCOM_SHIFT	0x030[6:4], 0x02D[7:0]	RW	11	VCOM Shift	0x014
R_STV_START	0x030[3:2], 0x02E[7:0]	RW	10	STV Signal Start	0x003
R_STV_END	0x030[1:0], 0x02F[7:0]	RW	10	STV Signal End	0x004
R_POL_CKV	0x031[0]	RW	1	CKV Output Polarity	0
R_POL_STV	0x031[1]	RW	1	STV Output Polarity	0
R_POL_STH	0x031[2]	RW	1	STH Output Polarity	0
R_POL_LD	0x031[3]	RW	1	LD Output Polarity	0
R_POL_FRP	0x031[4]	RW	1	FRP Output Polarity	0
R_POL_OEH	0x031[5]	RW	1	OEH Output Polarity 0: Normal 1: Invert	1
R_OEH_GATE	0x031[6]	RW	1	OEH gated with output data enable 0: Disable 1: Enable	0
R_TCON_EN	0x031[7]	RW	1	TCON Function Enable 0: Disable 1: Enable	1
R_STV_SEL	0x032[0]	RW	1	STV Output Selection 0: STV1 = OUT, STV2= IN 1: STV1 = IN, STV2 = OUT	0
R_STH_SEL	0x032[1]	RW	1	STH Output Selection 0: STH1 = OUT, STH2= IN 1: STH1 = IN, STH2 = OUT	1
R_TCON_UD	0x032[2]	RW	1	TCON U/D Signal 0: Low Level 1: High Level	0
R_TCON_RL	0x032[3]	RW	1	TCON R/L Signal 0: Low Level 1: High Level	1
R_POL_Q2H	0x032[4]	RW	1	Q2H Output Polarity 0: Normal	0

				1: Invert	
R_LTPS_MODE	0x032[5]	RW	1	LTPS Mode Selection 0: Normal Mode 1: LTPS TCON Mode	0
R_VCOM_SEL	0x032[7:6]	RW	2	VCOM Output Signal Selection 00: VCOM Signal 01: PREFRP Signal 10: FRP Signal 11: Q2H Signal	00
R_VCOM_TYPE	0x033[7:6]	RW	2	VCOM Signal TYPE 00: Always 0 01: Always 1 10: FRP Invert 11: FRP	11
R_BUS_INV	0x034[7:6]	RW	2	Data Bus Control on FRP 00: Disable 01: Follow Shift VCOM 10: Follow FRP 11: Follow Invert FRP	11
R_STV_SHIFT_E	0x0F8[6:4],0x0F9[7:0]	RW	11	STV Shift Start	0x000
R_STV_SHIFT_O	0x0F8[2:0],0x0FA[7:0]	RW	11	STV Shift End	0x000
R_STV_SHIFT_SRC	0x036[0]	RW	1	STV Output Selection 0: Type 0 1: Type 1	0
R_STV_SHIFT_TYPE	0x036[1]	RW	1	STV Output Type 0: Type 0 1: Type 1	0
R_STV_SHIFT_CUT	0x036[2]	RW	1	STV Line Cut 0: Disable 1: Enable	0

6.13 TCON Clock Mode

BIT1612 提供多種 TCON CPH Clock 模式，其相關 Registers 設定請參考下表。

Table 6-16 TCON Clock Mode Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CPH1E_CKSEL	0x033[1:0]	RW	2	CPH1 Clock Type Selection on Swap Source = 0	01
R_CPH2E_CKSEL	0x033[3:2]	RW	2	CPH2 Clock Type Selection on Swap Source = 0	01
R_CPH3E_CKSEL	0x033[5:4]	RW	2	CPH3 Clock Type Selection on Swap Source = 0	01
R_CPH1O_CKSEL	0x034[1:0]	RW	2	CPH1 Clock Type Selection on Swap Source = 1	01
R_CPH2O_CKSEL	0x034[3:2]	RW	2	CPH2 Clock Type Selection on Swap Source = 1	01
R_CPH3O_CKSEL	0x034[5:4]	RW	2	CPH3 Clock Type Selection on Swap Source = 1	01
R_CPH1_EN	0x035[0]	RW	1	CPH1 Output Enable	1
R_CPH2_EN	0x035[1]	RW	1	CPH2 Output Enable	1
R_CPH3_EN	0x035[2]	RW	1	CPH3 Output Enable 0: Disable 1: Enable	1
R_CPH_HALF	0x035[3]	RW	1	TCON Clock Output Mode 0: Normal Mode 1: Half Clock Mode	0
R_CPH1_POL	0x035[4]	RW	1	CPH1 Polarity	0
R_CPH2_POL	0x035[5]	RW	1	CPH2 Polarity	0
R_CPH3_POL	0x035[6]	RW	1	CPH3 Polarity	0

6.14 Display Layer

BIT1612 提供五層 Display Layer 以疊層架構顯示在 Panel 上，高優先權的 Layer 可覆蓋在低優先權的 Layer 相關說明請參考下圖。例如：Layer 5 優先權高於 Layer 4。

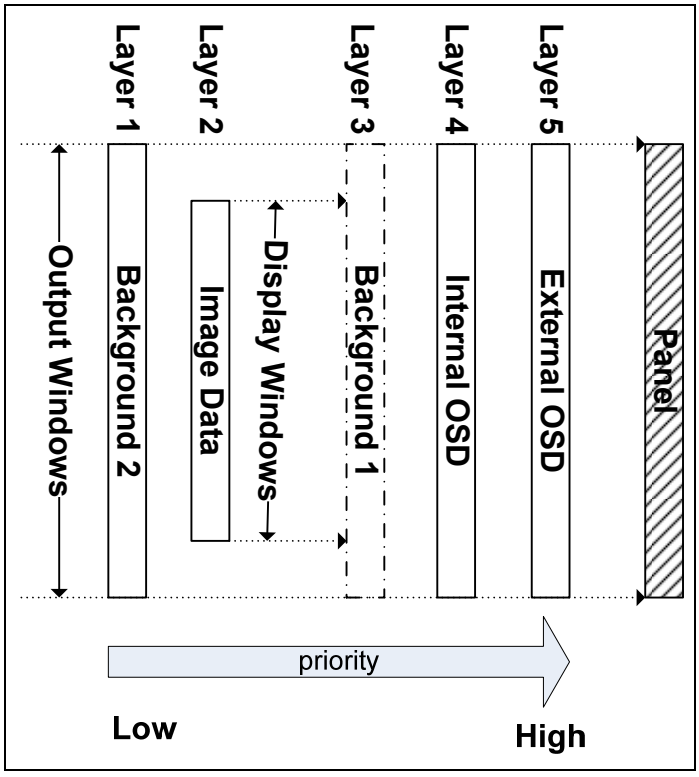


Figure 6-8 Display Layer

6.15 Background 2

BIT1612 內部提供 64 種背景色以提供在 4:3 模式下的邊框顯示，其相關Registers設定及其意義請參考 Table 6-17。

Table 6-17 Background 2 Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BG2_R	0x037[7:6]	RW	2	Background 2's R Color used for 4:3 display	00
R_BG2_G	0x038[7:6]	RW	2	Background 2's G Color used for 4:3 display	00
R_BG2_B	0x039[7:6]	RW	2	Background 2's B Color used for 4:3 display	00

6.16 Background 1 and Test Pattern Setup

BIT1612 內部提供 8 種內定Test Patterns，分別爲 262144 種純色、分隔線與漸層 (Ramp)，其相關Registers設定及其意義請參考 Table 6-18。

Table 6-18 Background and Test Pattern Register

Mnemonic	Address	R/W	Bits	Description	Default
R_TESTPAT_R	0x037[5:0]	RW	6	Test Pattern R Color Value	0x00
R_TESTPAT_G	0x038[5:0]	RW	6	Test Pattern G Color Value	0x00
R_TESTPAT_B	0x039[5:0]	RW	6	Test Pattern B Color Value	0x3F
R_TESTPAT_Q	0x03A[7:0]	RW	8	Test Pattern gradient ratio	0x00
R_TESTPAT_TYPE	0x03B[1:0]	RW	2	Test Pattern Type 00: 262144 純色 01: 漸層(Ramp) Ratio = 1 pixel 10: 分隔線(Grid) Ratio = 16 pixels 11: 漸層(Ramp) Ratio = 16 pixels	00
R_TESTPAT_DIR	0x03B[2]	RW	1	漸層的變化 0: Decrease 1: Increase	0
R_TESTPAT_HV	0x03B[3]	RW	1	漸層的方向 0: Vertical 1: Horizontal	0
R_BACKGROUND_EN	0x03B[6]	RW	1	Background Mode Enable 0: Disable 1: Enable	0
R_FREERUN_EN	0x03B[7]	RW	1	Free-Run Mode Enable 0: Disable 1: Enable	0

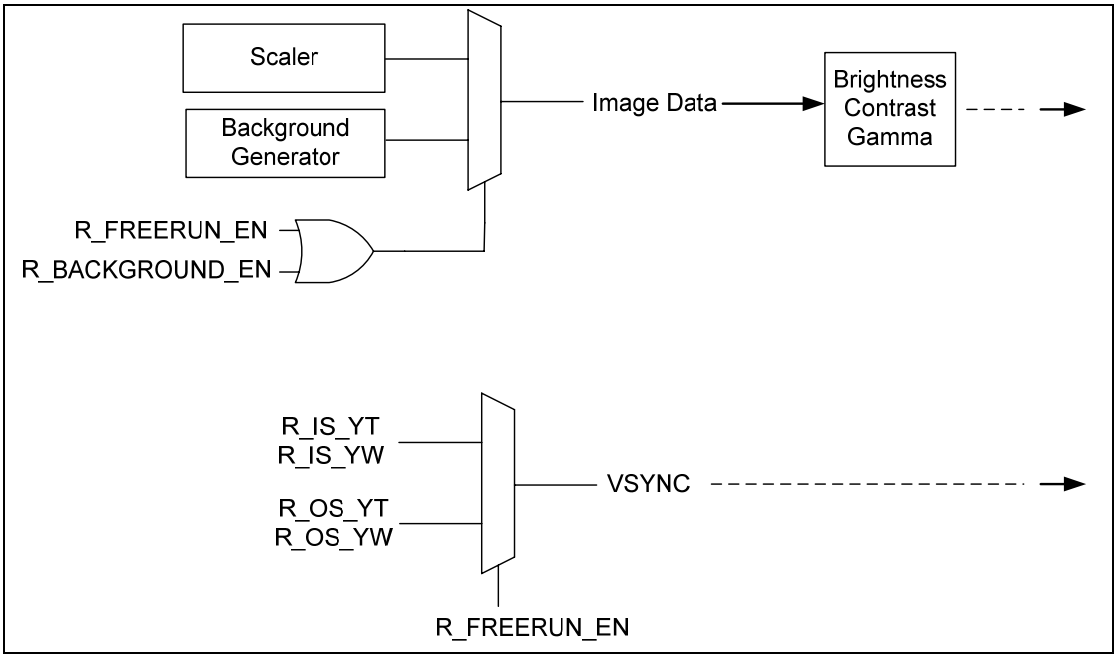


Figure 6-9 Free Run and Background

6.17 Auto Blank Screen

BIT1612 內建自動 Blank Screen Function，當訊號中斷或模式切換時將會自動啓動 Blank Screen 畫面，相關 Registers 設定請參考下表。

Table 6-19 Blank Screen Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTOON_TIME	0x03C[6:0]	RW	7	Blank Screen to Normal Screen Delay Times (Based on VSYNC)	0x0D
R_AUTOON_EN	0x03C[7]	RW	1	Blank Screen Function Enable 0: Disable 1: Enable	1
R_NOSIG_SEL	0x0FC[5]	RW	1	Blank Screen Function Signal Selection 0: From VP Signal 1: From VD Signal (R_HLCK_SEL)	0
R_HLCK_SEL	0x0FC[0]	RW	1	HLCK Detection Enable 0: Disable 1: Refer to HLCK	1
	0x0FC[1]	RW	1	Sync Ready Detection Enable 0: Disable 1: Refer to SYNC	1
	0x0FC[2]	RW	1	Standard Ready Detection Enable 0: Disable 1: Refer to STD	0
	0x0FC[3]	RW	1	AGC1 Ready Detection Enable 0: Disable 1: Refer to AGC1	0
	0x0FC[4]	RW	1	AGC2 Ready Detection Enable 0: Disable 1: Refer to AGC2	0

6.18 Input Image Window Setup

設定Input Image Window，BIT1612 將針對此區域內的資料進行Scaling運算。其相關Registers設定請參考 Table 6-20，相對應之示意圖請參考 Figure 6-10。

Table 6-20 Input Crop Register

Mnemonic	Address	R/W	Bits	Description	Default
Auto Switch Mode 0 Input Widows Setup					
R_IS_XS_M0	0x040[1:0], 0x03E[7:0]	RW	10	Input Window horizontal Start Position	0x09A
R_IS_XW_M0	0x040[7:4], 0x03F[7:0]	RW	12	Input Window horizontal End Position	0x346
R_IS_YS_M0	0x043[1:0], 0x041[7:0]	RW	10	Input Window vertical Start Position	0x018
R_IS_YW_M0	0x043[6:4], 0x042[7:0]	RW	11	Input Window vertical End Position	0x133
Auto Switch Mode 1 Input Windows Setup					
R_IS_XS_M1	0x046[1:0], 0x044[7:0]	RW	10	Input Window horizontal Start Position	0x08C
R_IS_XW_M1	0x046[7:4], 0x045[7:0]	RW	12	Input Window horizontal End Position	0x33C
R_IS_YS_M1	0x049[1:0], 0x047[7:0]	RW	10	Input Window vertical Start Position	0x015
R_IS_YW_M1	0x049[6:4], 0x048[7:0]	RW	11	Input Window vertical End Position	0x100

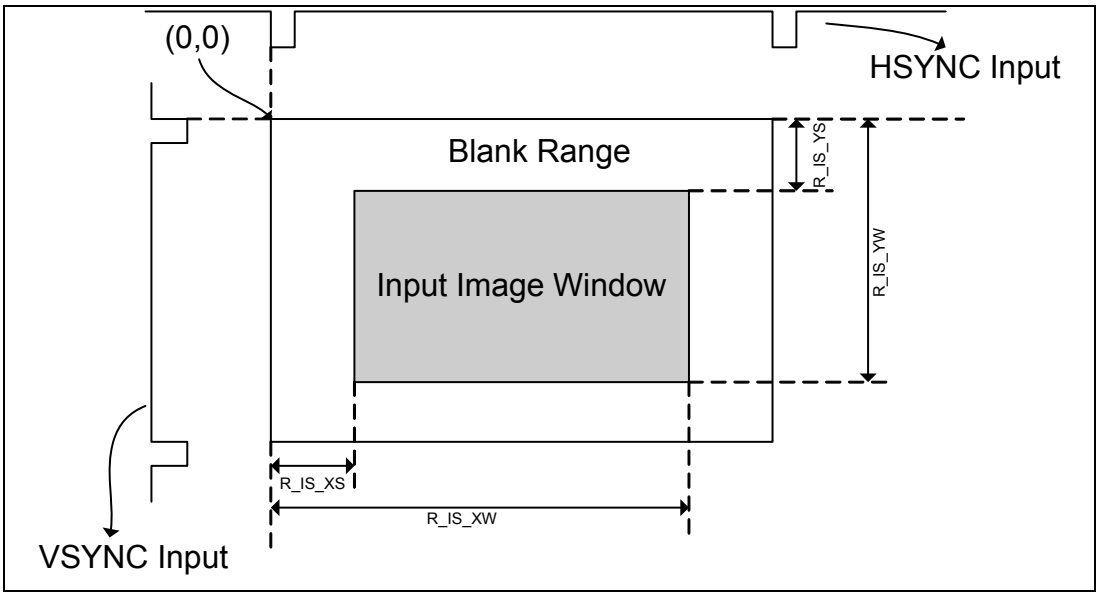


Figure 6-10 Input Window Setup

6.19 Input Data Path Setup

BIT1612 可針對輸入的Data Bus分別做Invert、Rotate 和 Swap 的處理，其相關Registers設定請參考 Table 6-21，相對應之方塊圖請參考 Figure 6-11。

Table 6-21 Input Data Path Register

Mnemonic	Address	R/W	Bits	Description	Default
R_POL_RIN	0x04A[0]	RW	1	R Data input Polarity ➔ 0: Normal 1: Invert	0
R_POL_GIN	0x04A[1]	RW	1	G Data input Polarity ➔ 0: Normal 1: Invert	0
R_POL_BIN	0x04A[2]	RW	1	B Data input Polarity ➔ 0: Normal 1: Invert	0

R_ROL_RIN	0x04A[3]	RW	1	R Data Rotate ➔ 0: Disable 1: Enable	0
R_ROL_GIN	0x04A[4]	RW	1	G Data Rotate ➔ 0: Disable 1: Enable	0
R_ROL_BIN	0x04A[5]	RW	1	B Data Rotate ➔ 0: Disable 1: Enable	0
R_ISWAP_RB	0x04C[0]	RW	1	R Data bus swap B Data bus ➔ 0: Disable 1: Enable	0
R_ISWAP_RG	0x04C[1]	RW	1	R Data bus swap G Data bus ➔ 0: Disable 1: Enable	0
R_ISWAP_GB	0x04C[2]	RW	1	G Data bus swap B Data bus ➔ 0: Disable 1: Enable	0
R_VD_PATH	0x04C[3]	RW	1	Bus Selection ➔0: External RGB Port; 1: Internal Video Decoder	0

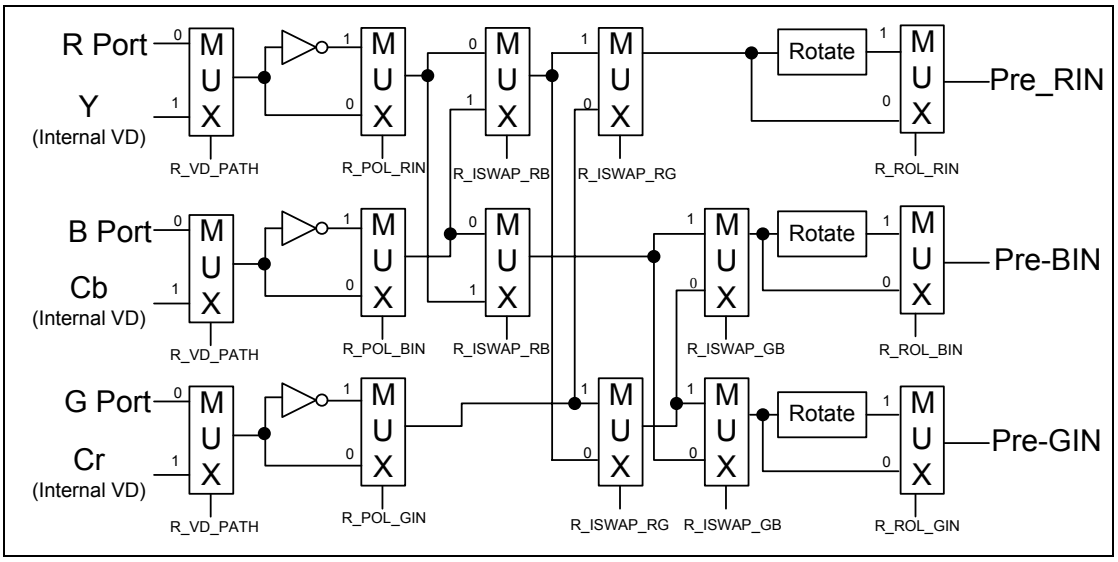


Figure 6-11 Input Data Path Setup

6.20 Input Format

BIT1612 支援七種輸入格式：ITU656、ITU656-Like、ITU601、RGB888、RGB565、Serial-RGB 和 YUV444。

6.20.1 ITU656

標準 8 Bits ITU656 (CCIR-656) 訊號格式，所有的 EVEN/ODD、HSYNC、VSYNC、YUV Data 將會由 8 Bits ITU656 Bus 解碼得到。(輸入頻率 27MHz)。

6.20.2 ITU656-Like

類標準 8 Bits ITU656 訊號格式，將會由 8 Bits ITU656 Bus 解碼得到 YUV Data，其餘 HSYNC、VSYNC 將由外部的 PAD 取得。(輸入頻率 27MHz)。

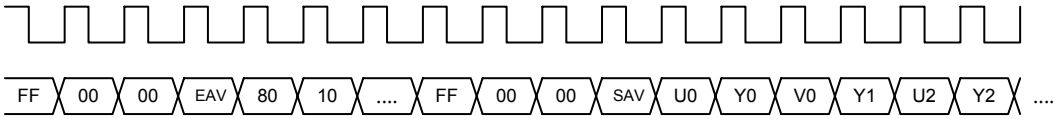


Figure 6-12 ITU656/656-Like (27MHz)

6.20.3 ITU601

16 Bits ITU601(CCIR-601) Video 訊號格式。(輸入頻率 13.5MHz)。

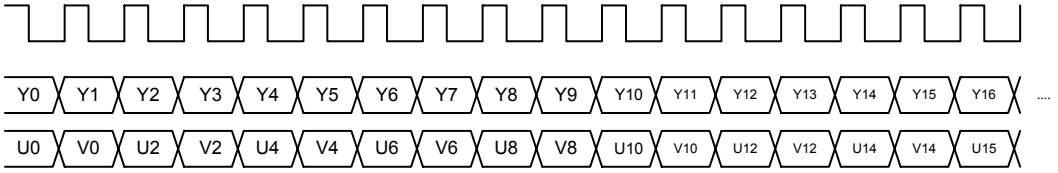


Figure 6-13 ITU601 (13.5MHz)

6.20.4 RGB888

RGB 8:8:8 訊號格式。BIT1612 在此模式下最大支援 1080i、720p 和 SXGA@60Hz 等解析度，在此模式下最大支援 100MHz Data Rate。

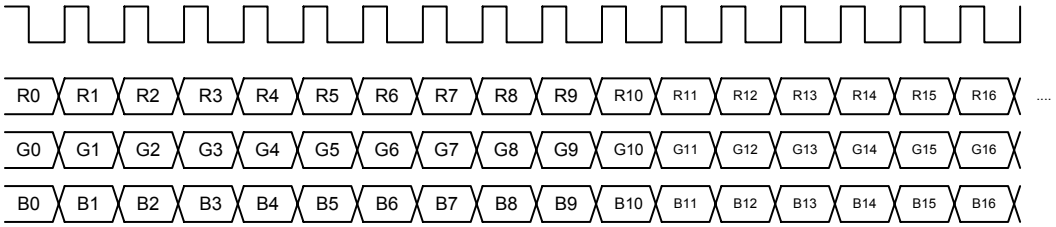


Figure 6-14 RGB 8:8:8 (Max. 100MHz)

6.20.5 Serial-RGB

BIT1612 提供 Serial-RGB Interface 訊號格式，在此模式下最大支援 40MHz Data Rate。

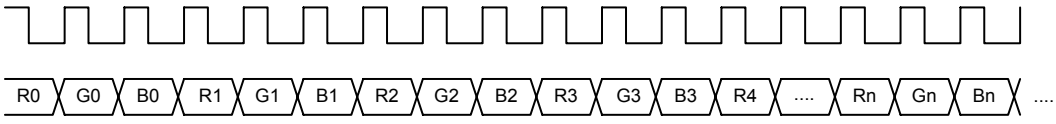


Figure 6-15 Serial-RGB (Max. 40MHz)

6.20.6 YUV444

YVU 4:4:4 訊號格式。BIT1612 針對 YUV Color Space Mode，BIT1612 在此模式下最大支援 1080i、720p 和 SXGA@60Hz 等解析度。在此模式下最大支援 100MHz Data Rate。

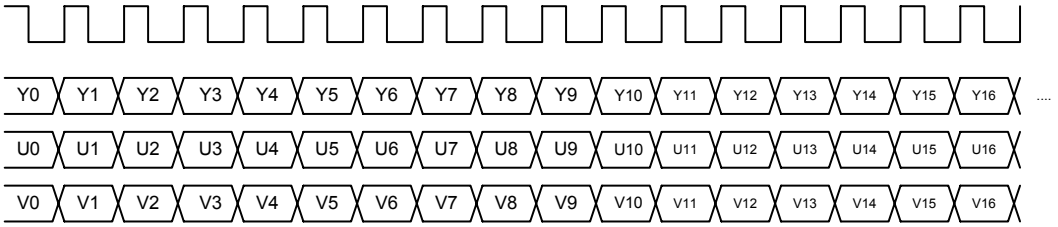


Figure 6-16 YUV 4:4:4 (Max.100MHz)

6.20.7 RGB565

RGB 5:6:5 訊號格式。BIT1612 在此模式下最大支援 1080i、720p 和 SXGA@60Hz 等解析度，在此模式下最大支援 100MHz Data Rate。

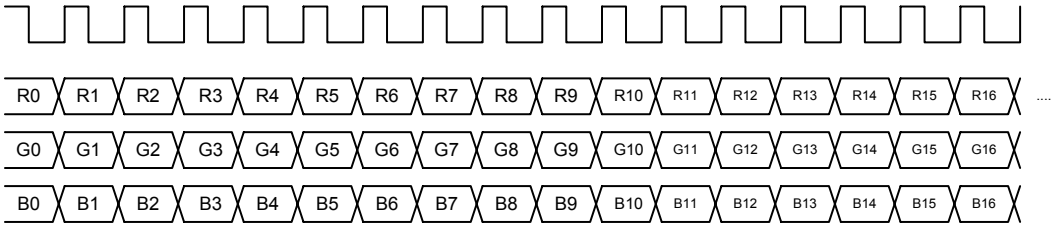


Figure 6-17 RGB 565 8:8:8 (Max. 100MHz)

RGB 5:6:5 Data Format 連線方式如下圖：

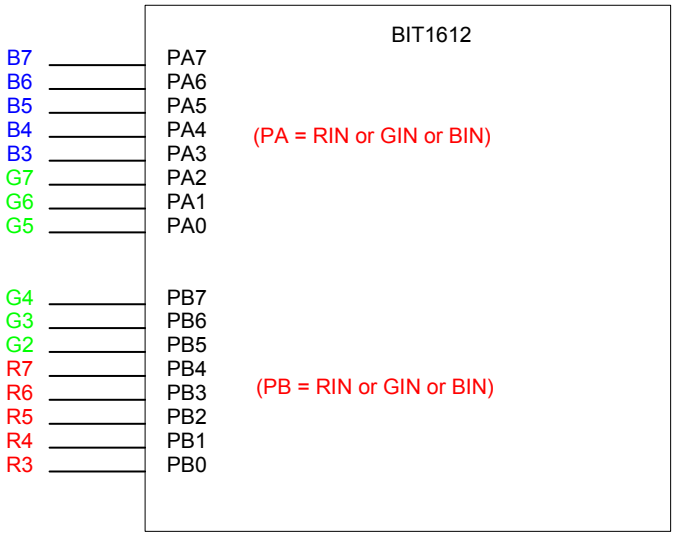


Figure 6-18 RGB 5:6:5 Setup

6.21 Input Mode Selection

BIT1612 經由Register設定決定輸入模式，其相關Registers設定，請參考下表，相對應之方塊圖請參考 Figure 6-19。

Table 6-22 Input Mode Selection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IHS_SEL	0x04B[0]	RW	1	External HSYNC Source Selection 0: External HSYNC Pin 1: Built-in Video Decoder HSYNC	0
R_IVS_SEL	0x04B[1]	RW	1	External VSYNC Source Selection 0: External VSYNC Pin 1: Built-in Video Decoder VSYNC	0
R_POL_IHS	0x04B[2]	RW	1	External HSYNC polarity ➔ 0: Normal, 1: Invert	0
R_POL_IVS	0x04B[3]	RW	1	External VSYNC polarity ➔ 0: Normal, 1: Invert	1
R_SEL_EVEN	0x04B[5:4]	RW	2	EVEN/ODD Signal Selection 00: ITU656-EVEN Signal 01: Visual EVEN/ODD Signal 10: Always EVEN Field 11: Always ODD Field	00
R_EXT_SYNC	0x04B[6]	RW	1	Sync Mode Selection 0: ITU656 Mode 1: From External Sync Pin or Built-In Video Decoder	0
R_SORT_656	0x04C[6:4]	RW	3	ITU656 / ITU601 Format ➔ Data Sequence Shift Control X00: No Shift X01: Shift 1 Clock X10: Shift 2 Clocks X11: Shift 3 Clocks Serial – RGB Format ➔ Serial-Bus Data Sort Control 000: Always 0 001: R-G-B 010: R-B-G 011: G-R-B 100: G-B-R 101: B-G-R 110: B-R-G 111: Always 1 RGB 5:6:5 Format ➔ Data Compensation Mode X0X: Compensate with R_SORT_656[0]. X1X: Compensate with LSB Data.	000
R_VISUAL_TYPE	0x04C[7]	RW	1	Visual EVEN/ODD Mode 0: Normal EVEN/ODD Mode 1: Always Change by VSYNC	0
R_SRC_SEL	0x04D[1:0]	RW	2	Source Format Selection RGB Domain Source ➔ R_IMODE= 1 00: Serial-RGB Format 01: RGB 5:6:5 Format 1x: RGB 8:8:8 Format YUV Domain Source ➔ R_IMODE = 0 00: ITU656 / ITU656-Like Format 01: ITU601 Format 1x: YUV 4:4:4 Format	00
R_SWAP_UV	0x04D[2]	RW	1	Swap U and V signal 0: Disable	0

				1: Enable	
R_IMODE	0x04D[3]	RW	1	Input Mode Selection 0: YUV Domain Source Input 1: RGB Domain Source Input	0
R_PCLK_BASE	0x04D[5:4]	RW	2	Input Active Pixel Mode 00: 1-Pixel Mode (RGB888、RGB565、YUV444、ITU601) 01: 2-Pixel Mode (ITU656/ITU656-Like) 10: 3-Pixel Mode (Serial RGB) 11: 4-Pixel Mode	01

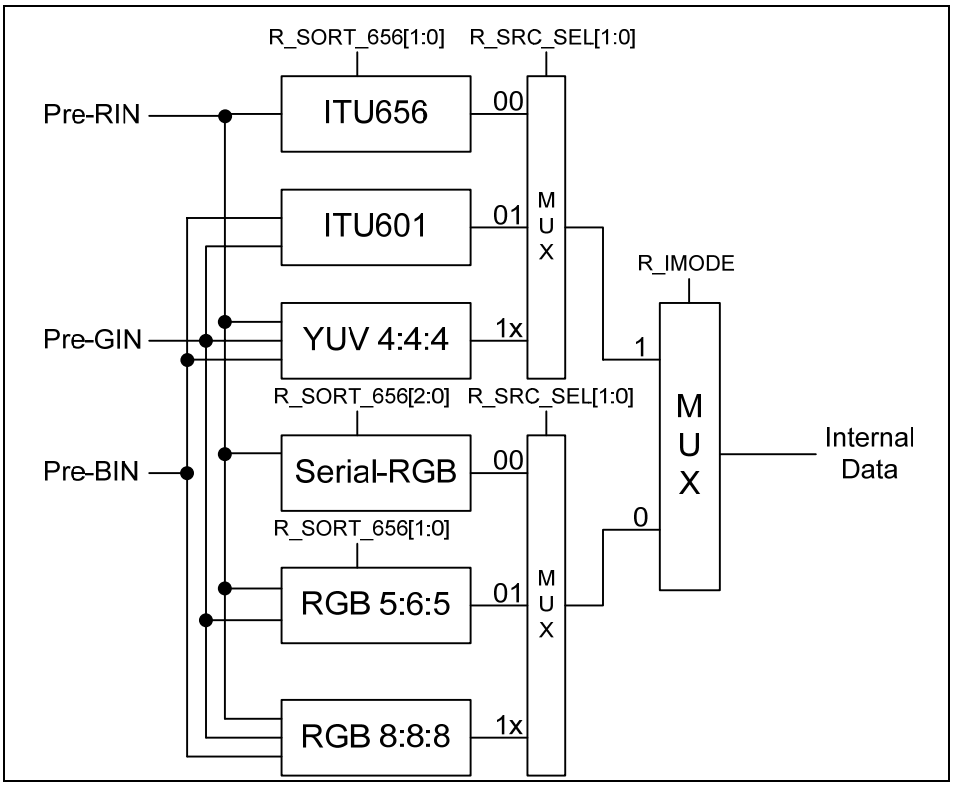


Figure 6-19 Input Mode Selection

6.22 Auto Switch

BIT1612 針對Input Windows、Scaling Factor和Timing setup提供兩組Register設定，可分別設定爲自動或手動切換模式，當在自動模式時BIT1612 將會判別輸入訊號爲 50Hz or 60Hz自動切換至相對應的Register群組，其相關Registers設定請參考 Table 6-23。

Table 6-23 Auto Switch Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTO_SWITCH	0x04A[6]	RW	1	Auto Switch Mode 0: Manual Mode 1: Auto Mode	1
R_SWITCH_MODE	0x04A[7]	RW	1	Manual Mode Selection 0: Select Mode 0 1: Select Mode 1	1

6.23 Display Window Setup

BIT1612 定義了一個Display Window的區域，將Scaling後的影像資料顯示於此區域內，因此在Timing許可下，可任意做上下左右Move (Pan) 和Resize的動作，其相關Registers設定請參考 Table 6-24，相對應之示意圖請參考 Figure 6-20。

Table 6-24 Display Windows Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PRDIS_ACTX	0x052[6:4], 0x04F[7:0]	RW	11	Display Window Pre-Scaling Active Horizontal Width	0x1E0
R_DIS_YS	0x052[1:0], 0x050[7:0]	RW	10	Display Window Vertical Start Position	0x005
R_DIS_YW	0x052[3:2], 0x051[7:0]	RW	10	Display Window Vertical End Position	0x0F0
R_DIS_XS	0x055[1:0], 0x053[7:0]	RW	10	Display Window Horizontal Start Position	0x020
R_DIS_XW	0x055[6:4], 0x054[7:0]	RW	11	Display Window Horizontal End Position	0x200
R_DIS_XW1	0x058[2:0], 0x056[7:0]	RW	11	Display Window Active Horizontal Width On Linear Mode: Define All Region On Anzoom Mode: Define 2 Region	0x320
R_DIS_XW2	0x058[6:4], 0x057[7:0]	RW	11	Display Window Active Horizontal Width On Linear Mode: No Active On Anzoom Mode: Define 1 and 3 Region	0x320

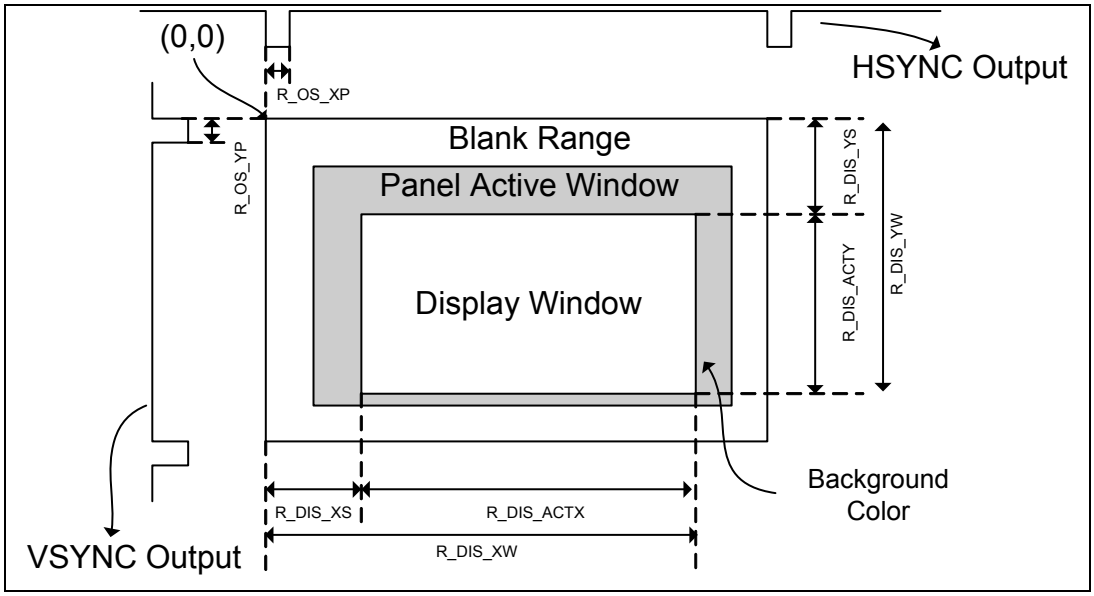


Figure 6-20 Display Window Setup

6.24 Scaling Engine

BIT1612 可分別針對垂直 (Vertical) 和水平 (Horizontal) 方向做 Scaling 處理，其相關設定及說明如下：

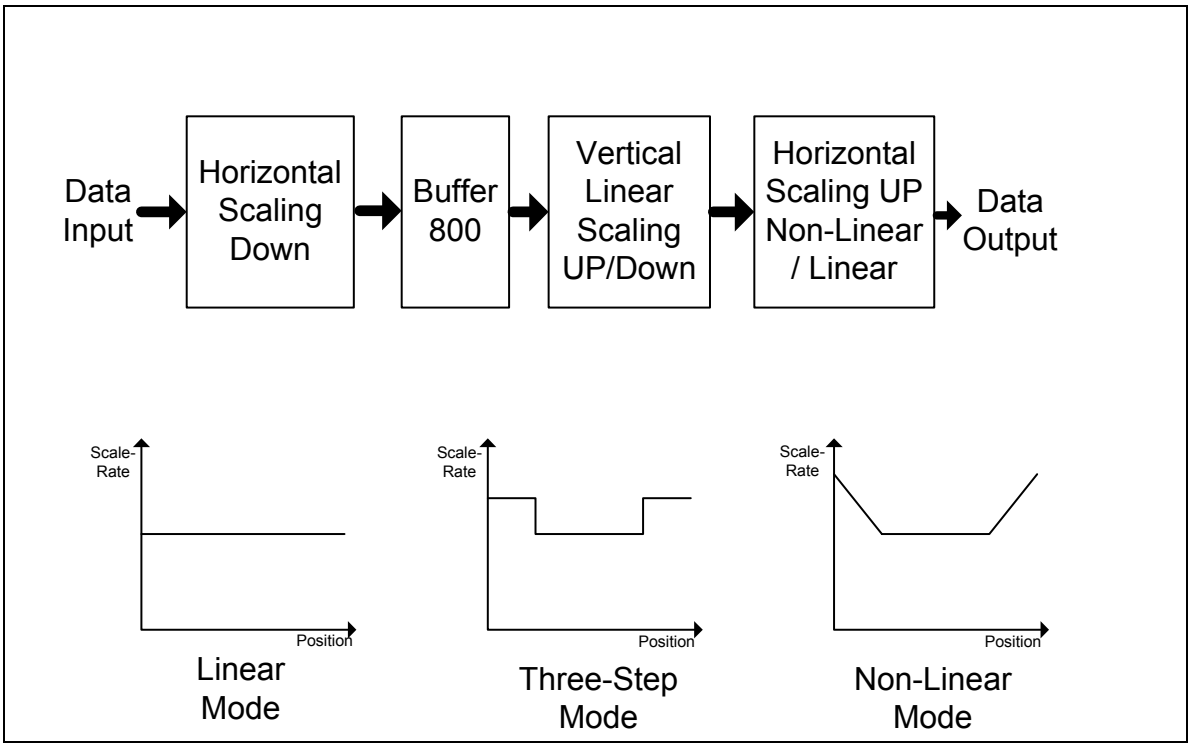


Figure 6-21 Scaling Function

6.24.1 Horizontal Scaling Down Engine

BIT1612 可針對水平方向預作縮小處理，以符合Buffer深度。其相關設定請參考 Table 6-25。

Table 6-25 Horizontal Scale Down Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PRESCX_START	0x05B[7:4], 0x059[7:0]	RW	12	Horizontal Scaling Down Start Value	0x0B5
R_PRESCX_SHIFT	0x05B[2:0], 0x05A[7:0]	RW	11	Horizontal Scaling Down Shift Value	0x16A
R_PRESCX_FIX	0x05C[5:4], 0x05D[7:0]	RW	10	Horizontal Scaling Down Fix Value	0x140
R_PRESCX_EN	0x05C[0]	RW	1	Horizontal Scaling Down Enable 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	1
R_PRESCX_FILTER_EN	0x05C[1]	RW	1	Horizontal Scaling Down Filter Enable 0: Disable (Bypass Mode) 1: Enable (Filter Mode)	1
R_PRESCX_FILTER	0x05C[2]	RW	1	Horizontal Scaling Down Filter Type 0: Bi-Linear Filter 1: Box Filter	0
R_PRE_FIX2_EN	0x05C[3]	RW	1	Scale Down Factor 2 Enable 0: Disable (Bypass Mode) 1: Enable (Scale Down 2 Mode)	0
R_PRESCX_OVER	0x05C[7]	RW	1	Scale Down Factor over 2 0: Disable (Factor under 2) 1: Enable (Factor over 2)	0

6.24.2 Horizontal Scaling UP Engine

BIT1612 可針對水平方向作放大處理，以符合Panel解析度。其相關設定請參考 Table 6-26。

Table 6-26 Horizontal Scale UP Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SCX_START	0x061[1:0], 0x05E[7:0]	RW	10	Horizontal Start Value	0x06C
R_SCX1_SHIFT	0x05F[7:0]	RW	8	Horizontal Zone 1 Shift Value	0xD8
R_SCX1_FIX	0x061[6:4], 0x060[7:0]	RW	11	Horizontal Zone 1 Fix Value	0x1E0
R_SCX2_SHIFT	0x062[7:0]	RW	8	Horizontal Zone 2 Shift Value	0x00
R_SCX2_FIX	0x066[2:0], 0x063[7:0]	RW	11	Horizontal Zone 2 Fix Value	0x000
R_SCX1_INC	0x066[5:4], 0x064[7:0]	RW	10	Non-Linear Increase Value	0x000
R_SCX2_DEC	0x066[7:6], 0x065[7:0]	RW	10	Non-Linear Decrease Value	0x000
R_SCX_EN	0x067[0]	RW	1	Horizontal Scaling Enable 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	0
R_SCX_FILTER	0x067[3:2]	RW	2	Horizontal Scaling Filter Type 11: Bypass Filter 10: Box Filter 01: Bi-Linear Filter 00: Catrom Filter	00
R_ANZOOM_TYPE	0x067[6]	RW	1	Wide Screen Type 0: 3-Zone Wide Screen 1: Non-Liner Wide Screen	0
R_ANZOOM_EN	0x067[7]	RW	1	Wide Screen Mode Enable 0: Disable 1: Enable	0

6.24.3 Vertical Scaling Engine

BIT1612 可依據Auto Switch Mode所選擇的模式 (Mode 0/Mode 1)，自動切換適合的參數，針對影像垂直方向分別做放大或縮小處理，以符合panel解析度。其相關設定請參考 Table 6-27。

Table 6-27 Vertical Scale-Down Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SCYE_START_M0	0x06C[1:0], 0x068[7:0]	RW	10	Vertical Start Value for EVEN Field on Switch Mode 0	0x07A
R_SCYO_START_M0	0x06C[3:2], 0x069[7:0]	RW	10	Vertical Start Value for ODD Field on Switch Mode 0	0x09E
R_SCY_SHIFT_M0	0x06C[4], 0x06A[7:0]	RW	9	Vertical Shift Value on Switch Mode 0	0x130
R_SCY_FIX_M0	0x06C[6:5], 0x06B[7:0]	RW	10	Vertical Fix Value on Switch Mode 0	0x000
R_UPDN_SEL_M0	0x06C[7]	RW	1	Vertical Scaling Mode 0: Scaling Down Mode 1: Scaling Up Mode	0
R_SCY_EN_M0	0x06D[0]	RW	1	Vertical Scaling Function Enable on Switch Mode 0 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	1
R_SCY_FILTER_EN_M0	0x06D[1]	RW	1	Vertical Scaling Filter Enable 0: Disable 1: Enable	1
R_SCY_FILTER_M0	0x06D[2]	RW	1	Vertical Scaling Filter Type on Switch Mode 0 0: Bi-Linear Filter 1: Box Filter	0
R_LINE_CUT_M0	0x06D[5]	RW	1	Vertical Pre-Scaling Down Enable on Auto Switch Mode 0 0: Disable 1: Enable	0
R_CUT_MODE_M0	0x06D[6]	RW	1	Vertical Pre-Scaling Down Mode on Auto Switch Mode 0 0: EVEN Line 1: ODD Line	0
R_CUT_AUTO_M0	0x06D[7]	RW	1	Vertical Pre-Scaling Change Mode on Auto Switch Mode 0 0: Manual (R_CUT_MODE) 1: Auto (EVEN/ODD)	0
R_SCYE_START_M1	0x072[1:0], 0x06E[7:0]	RW	10	Vertical Start Value for EVEN Field on Switch Mode 1	0x01B
R_SCYO_START_M1	0x072[3:2], 0x06F[7:0]	RW	10	Vertical Start Value for ODD Field on Switch Mode 1	0x01B
R_SCY_SHIFT_M1	0x072[4], 0x070[7:0]	RW	9	Vertical Shift Value on Switch Mode 1	0x0FF
R_SCY_FIX_M1	0x072[6:5], 0x071[7:0]	RW	10	Vertical Fix Value on Switch Mode 1	0x089
R_UPDN_SEL_M1	0x072[7]	RW	1	Vertical Scaling Mode on Switch Mode 1 0: Scaling Down Mode 1: Scaling Up Mode	0
R_SCY_EN_M1	0x073[0]	RW	1	Vertical Scaling Function Enable on Switch Mode 1 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	1

R_SCY_FILTER_EN_M1	0x073[1]	RW	1	Vertical Scaling Filter Enable 0: Disable 1: Enable	1
R_SCY_FILTER_M1	0x073[2]	RW	1	Vertical Scaling Filter Enable on Switch Mode 1 0: Bi-Linear Filter 1: Box Filter	0
R_LINE_CUT_M1	0x073[5]	RW	1	Vertical Pre-Scaling Down Enable on Auto Switch Mode 1 0: Disable 1: Enable	0
R_CUT_MODE_M1	0x073[6]	RW	1	Vertical Pre-Scaling Down Mode on Auto Switch Mode 1 0: EVEN Line 1: ODD Line	0
R_CUT_AUTO_M1	0x073[7]	RW	1	Vertical Pre-Scaling Change Mode on Auto Switch Mode 1 0: Manual (R_CUT_MODE) 1: Auto (EVEN/ODD)	0

6.25 Timing Adjustment

BIT1612 Timing 調整原則：

1. IVREF (t1) 總長度與OVREF (t2) 相近且小於OVREF (t2) (參考 Figure 6-22)。

2. 修正 Line Buffer 所產生的 Error (Overflow or Underflow)。

Table 6-28 Timing Adjust Register

Mnemonic	Address	R/W	Bits	Description	Default
R_MASTER_DLY_M0	0x074[7:0]	RW	8	Output VSYNC Synchronize Delay Time (Base on IHSYNC) on Switch Mode 0	0x16
R_DLYE_OCLK_M0	0x077[3:0], 0x075[7:0]	RW	12	Even Field Output VSYNC Synchronize Delay Time (Base on LCLK) on Switch Mode 0	0x075
R_DLYO_OCLK_M0	0x077[7:4], 0x076[7:0]	RW	12	Odd Field Output VSYNC Synchronize Delay Time (Base on LCLK) on Switch Mode 0	0x071
R_MASTER_DLY_M1	0x078[7:0]	RW	8	Output VSYNC Synchronize Delay Time (Base on IHSYNC) on Switch Mode 1	0x13
R_DLYE_OCLK_M1	0x07B[3:0], 0x079[7:0]	RW	12	Even Field Output VSYNC Synchronize Delay Time(Base on LCLK) on Switch Mode 1	0x266
R_DLYO_OCLK_M1	0x07B[7:4], 0x07A[7:0]	RW	12	Odd Field Output VSYNC Synchronize Delay Time(Base on LCLK) on Switch Mode 1	0x066
R_HCOUNT	0x169[6:0], 0x168[7:0]	R	15	Horizontal Counter	-

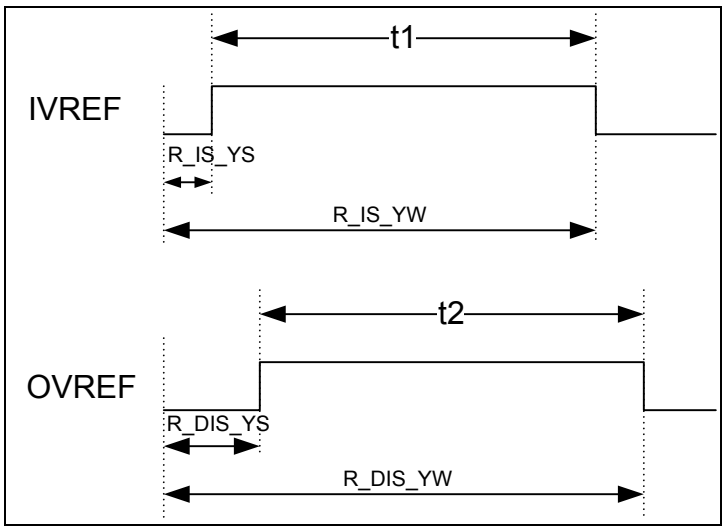


Figure 6-22 Timing Adjustment VREF Information

6.26 Image Enhancement

BIT1612 提供多樣的調整機制，使用者可依據需求針對影像作調整，以獲得最佳之顯示效果。處理單元包括 Scaler 之前的前置處理與 Scaler 之後的後置處理兩部份。相關架構請參考下圖。

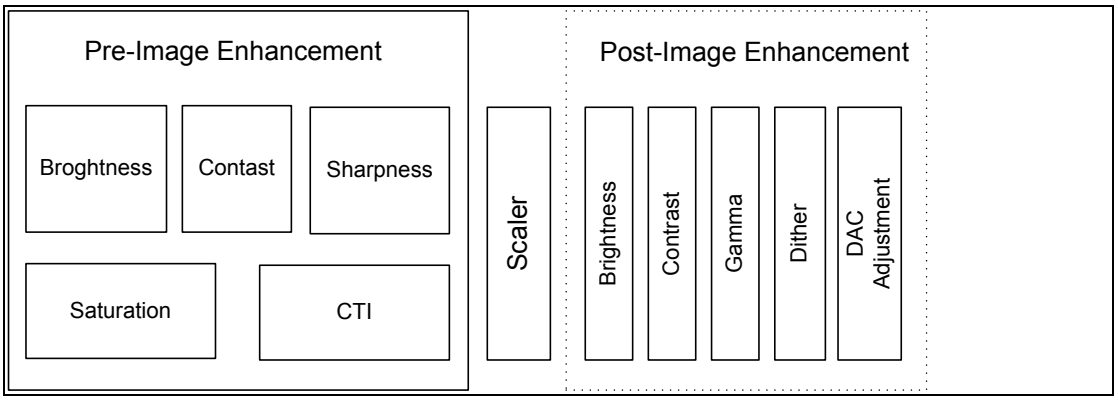


Figure 6-23 Image Enhancement

6.26.1 Post-Processing Brightness and Contrast

BIT1612 針對 RGB Domain 的個別 Channel，分別提供 Brightness 和 Contrast 調整。其架構及相對應設定如下所示。

Table 6-29 Color Adjustment Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BRIGHTNESS_R	0x07C[7:0]	RW	8	R Channel Brightness Value	0x80
R_BRIGHTNESS_G	0x07D[7:0]	RW	8	G Channel Brightness Value	0x80
R_BRIGHTNESS_B	0x07E[7:0]	RW	8	B Channel Brightness Value	0x80
R_CONTRAST_R	0x07F[7:0]	RW	8	R Channel Contrast Value	0x80
R_CONTRAST_G	0x080[7:0]	RW	8	G Channel Contrast Value	0x80
R_CONTRAST_B	0x081[7:0]	RW	8	B Channel Contrast Value	0x80
R_CONTRAST_TYPE	0x090[0]	RW	1	Contrast Adjust Type 0: Type 1 1: Type 2	0

6.26.2 Pre-Processing Brightness/Contrast Adjustment

BIT1612 針對 Y Domain 提供 Brightness 和 Contrast 的調整。其輸入對輸出曲線及相對應設定如下所示。

Table 6-30 Color Adjustment Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BRIGHTNESS	0x082[7:0]	RW	8	Brightness Value (-128 ~ +127) 0x00=-128, 0x80=0, 0xFF=+127	0x80
R_CONTRAST	0x083[7:0]	RW	8	Contrast Value for Middle Range Adjustment Range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80
R_WHITE_SLOPE	0x084[7:0]	RW	8	Contrast Value for White Range Adjustment Range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80
R_BLACK_SLOPE	0x085[7:0]	RW	8	Contrast Value for Black Range Adjustment Range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80
R_WHITE_START	0x086[4:0]	RW	5	White Range Start Position Range : 0xE0 ~ 0xFF 0x00=0xE0, 0x3F=0xFF	0x00
R_BLACK_START	0x087[4:0]	RW	5	Black Range Start Position Range : 0x00 ~ 0x1F 0x00=0x00, 0x1F=0x1F	0x00

6.26.3 Sharpness Process

BIT1612 針對 Y Domain Data 提供 Sharpness 處理可強化影像之銳利度，其相對應設定如下所示。

Table 6-31 Sharpness and Smoothness Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UNSHARP_VAL	0x08A[6:0]	RW	7	Sharpness Value (0~127) 0x00: Least Sharpness 0x7F: Most Sharpness	0x00
R_UNSHARP_EN	0x08A[7]	RW	1	Sharpness Enable 0: Disable 1: Enable	0
R_UNSHARP_THD	0x08B[5:0]	RW	6	Sharpness Threshold Value	0x00

6.26.4 Saturation and Kill Color Process

BIT1612 針對 UV Domain Data 提供 Saturation 和 Kill Color 的處理，可讓使用者依喜好調到較佳的色彩影像，其相對應設定如下所示。

Table 6-32 UV Domain Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SAT_U	0x08C[6:0]	RW	7	U Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_SAT_V	0x08D[6:0]	RW	7	V Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_SAT_MODE	0x08C[7]	RW	1	V Saturation Value Reference with R_SAT_U 0: Disable 1: Simultaneously Adjust R_SAT_U and R_SAT_V (From R_SAT_U)	1
R_KILL_COLOR	0x090[6]	RW	1	Control Kill Color Enable 0: Disable 1: Enable	0

6.26.5 Chroma Transient Improvement (CTI)

BIT1612 提供Chroma Transient Improvement (CTI)，相關Registers請參考 Table 6-33。

Table 6-33 Chroma Transient Improvement Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CTI_THD	0x08E[7:0]	RW	8	CTI Process Threshold Value	0x01
R_CTI_U_SEL	0x08F[2:0]	RW	3	CTI Level Selection for U Domain 000: Least CTI Enhancement 111: Most CTI Enhancement	111
R_CTI_V_SEL	0x08F[6:4]	RW	3	CTI Level Selection for V Domain 000: Least CTI Enhancement 111: Most CTI Enhancement	111
R_CTI_EN	0x08F[7]	RW	1	CTI Enable 0: Disable 1: Enable	0

6.26.6 Color Space Conversion

BIT1612 提供兩種 Color Space Conversion，用以轉換YUV Color Domain to RGB Color Domain相關Registers請參考 Table 6-34。

Table 6-34 Color Space Converter Register

Mnemonic	Address	R/W	Bits	Description	Default
R_Y2R_SEL	0x090[7]	RW	1	Color Space Conversion 0: No Gamma-Correction 1: Gamma-Correction	0

6.26.7 LUT Gamma Correction

BIT1612 內建LUT-base Gamma Correction Function，其相關記憶體對應爲 0x200~0x2FF，相關Registers請參考 Table 6-35。

Table 6-35 LUT Gamma Register

Mnemonic	Address	R/W	Bits	Description	Default
R_GAMMA_EN	0x090[2]	RW	1	GAMMA LUT Enable 0: Gamma RAM R/W Mode 1: Gamma Correction Mode	0
R_GAMMA_SEL	0x090[4:3]	RW	2	GAMMA LUT RAM R/W Selection 00: Red 01: Green 10: Blue 11: Write RGB, Read Forbiddance	00

6.26.8 Dither

BIT1612 內建 User Programmable Dither Function 能使 6 Bits Panel Display 得到更佳的顯示品質，相關 Registers 請參考下表。

Table 6-36 Dither Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DITHER_EN	0x090[1]	RW	1	Dither Function Enable 0: Disable 1: Enable	0
R_DITHER_EVEN	0x091[7:0]	RW	8	EVEN Field Dither Factor	0x87
R_DITHER_ODD	0x092[7:0]	RW	8	ODD Field Dither Factor	0x78
R_DITHER_MASK	0x090[5]	RW	1	OSD Area Dither Mask Enable 0: Disable 1: Enable	1

6.26.9 DAC Correction

BIT1612 有一 DAC 誤差修正演算法，可以修正 DAC 誤差，其相關 Registers 設定請參考下表。

Table 6-37 DAC Correction Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DAC_B	0x095[7:0]	RW	8	B Offset Factor	0x80
R_DAC_C	0x096[7:0]	RW	8	C Slope Factor	0x80
R_DAC_CEN	0x097[0]	RW	1	DAC Correct Function Enable 0: Disable 1: Enable	0
R_DAC_CTYPE	0x097[1]	RW	1	C Slope Type 0: Central Point Mode 1: Normal Mode	0

6.26.10 Clamp and Linear Mapping

BIT1612 有輸出範圍線性對映運算單元，並附帶箝位功能，其運算單元位於Gamma Correction的後級，可以對Gamma Correction後的RGB圖像再進行調整，其相關設定Registers請參考 Table 6-38。 當只需要輸出箝位功能時，只要將R_CLAMP_EN設爲 1，並由輸出最大值 MAX回推R_OUT_DACMAP_SPACE值，最小值MIN回推R_OUT_DACMAP_LB值，即可使RGB輸出值介於MAX到MIN之間。公式如下：

$$MAX = 256 + R\_OUT\_DACMAP\_SPACE \ (V)$$

$$MIN = R\_OUT\_DACMAP\_LB \quad (V)$$

當輸出需要線性對映功能時，則可以設定R_DACMAP_EN爲 1，且將R_CLAMP_EN設爲 0，其輸出範圍與上面公式相同，比較輸入與輸出線性關係，在R_CLAMP_EN爲 1 時，其輸入輸出轉換曲線斜率爲 1，而R_DACMAP_EN = 1 時，則可以透過R_OUT_DACMAP_LB與R_OUT_DACMAP_SPACE調整，其差別可以參考 Figure 6-24 及 Figure 6-25。

Table 6-38 Clamp and Linear Mapping Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CLAMP_EN	0x97[2]	RW	1	Clamp Function 0: Disable 1: Enable	0
R_DACMAP_EN	0x94[7]	RW	1	Linear Mapping Function 0: Disable (Bypass) 1: Enable	0
R_OUT_DACMAP_LB	0x094[6:0]	RW	7	Low Bound	0x67
R_OUT_DACMAP_SPACE	0x093[7:0]	RW	8	Up Bound – Low Bound	0x99

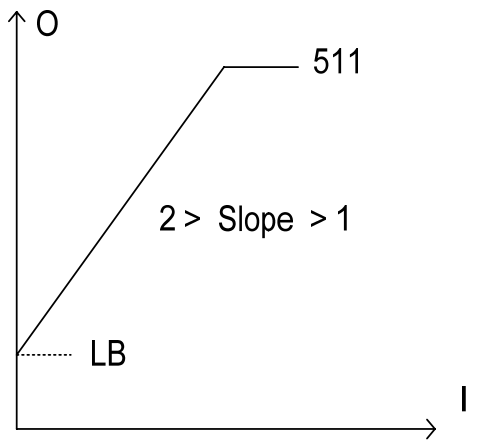


Figure 6-24 Linear Mapping

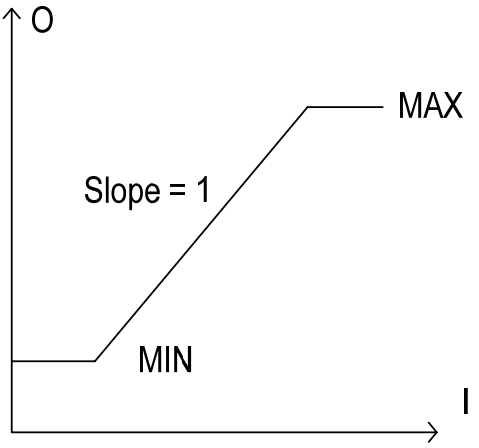


Figure 6-25 DAC Clamp

6.27 PWM Function

BIT1612 提供三組可獨立設定之PWM輸出，可藉此控制背光、聲音等裝置，其相關Registers設定請參考下表，相對應之示意圖請參考 Figure 6-26。

Table 6-39 PWM Function Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PWM1_FREQ	0x099[3:0], 0x098[7:0]	RW	12	PWM1 Output Cycles.	0x100
R_PWM1_REF	0x099[7:4]	RW	4	PWM1 Reference Cycles.	0x1
R_PWM1_DUTY	0x09B[3:0], 0x09A[7:0]	RW	12	PWM1 Output Duty Cycle	0x080
R_PWM1_EN	0x09C[0]	RW	1	PWM1 Function Enable 0: Disable 1: Enable	1
R_PWM1_POL	0x09C[1]	RW	1	PWM1 Output Polarity 0: Normal 1: Invert	0
R_PWM1_SYNC	0x09C[3:2]	RW	2	PWM1 Synchronized with VSYNC 11: Synchronized with Input VSYNC 10: Synchronized with Output VSYNC 0x: Not Synchronized with VSYNC	00
R_PWM1_INV	0x09C[4]	RW	1	PWM2 Output Selection 0: PWM2 Signal 1: Invert PWM1 Signal	0
R_PWM_OUT	0x09C[5]	RW	1	SRGB PWM Enable 0: Disable 1: Enable	0
R_PWM2_FREQ	0x09E[3:0], 0x09D[7:0]	RW	12	PWM2 Output Cycles.	0x200
R_PWM2_REF	0x09E[7:4]	RW	4	PWM2 Reference Cycles.	0x3
R_PWM2_DUTY	0x0A0[3:0], 0x09F[7:0]	RW	12	PWM2 Output Duty Cycle	0x100
R_PWM2_EN	0x0A1[0]	RW	1	PWM2 Function Enable 0: Disable 1: Enable	1
R_PWM2_POL	0x0A1[1]	RW	1	PWM2 Output Polarity 0: Normal 1: Invert	0
R_PWM2_SYNC	0x0A1[3:2]	RW	2	PWM2 Synchronized with VSYNC 11: Synchronized with Input VSYNC 10: Synchronized with Output VSYNC 0x: Not Synchronized with VSYNC	11
R_PWM3_FREQ	0x0A3[3:0], 0x0A2[7:0]	RW	12	PWM3 Output Cycles.	0x300
R_PWM3_REF	0x0A3[7:4]	RW	4	PWM3 Reference Cycles.	0x0
R_PWM3_DUTY	0x0A5[3:0], 0x0A4[7:0]	RW	12	PWM3 Output Duty Cycle	0x150
R_PWM3_EN	0x0A6[0]	RW	1	PWM3 Function Enable 0: Disable 1: Enable	1
R_PWM3_POL	0x0A6[1]	RW	1	PWM3 Output Polarity 0: Normal 1: Invert	0
R_PWM3_SYNC	0x0A6[3:2]	RW	2	PWM3 Synchronized with VSYNC 11: Synchronized with Input VSYNC	11

				10: Synchronized with Output VSYNC 0x: Not Synchronized with VSYNC	

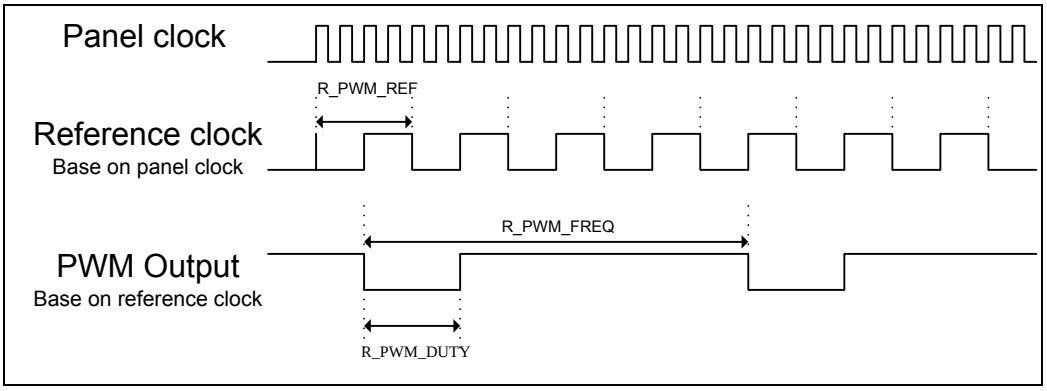


Figure 6-26 PWM Function

6.28 Video Decoder

6.28.1 Video Decoder Feature

- Three analog inputs, internal analog source selectors, e.g. CVBS x3 or Y/C x1 or (Y/C x1 and CVBS x1) or YPbPr (480i or 576i)
- Two 10-bit video CMOS Analog-to-Digital Converters (ADCs) in differential CMOS style for best S/N-performance
- Fully programmable static gain or automatic gain control (AGC) for the selected CVBS or Y/C channel : 0~12db (Analog) and 0~18db (Digital)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- On-chip clock generator
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal (24.576 MHz) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Accepts NTSC (J, M, 4.43), PAL (60, B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video signal
- User programmable luminance peaking or aperture correction
- Adaptive 3/5-line comb filter for two dimensional chrominance/luminance separation
- PAL delay line for correcting PAL phase errors
- Brightness Contrast Saturation (BCS) and Hue control on-chip
- Multi-standard VBI-data slicer decoding closed caption
- MV copy protection detection
- User programmable sharpness filter
- User programmable U/V Gain and CTI function

6.28.2 Video Decoder Architectures

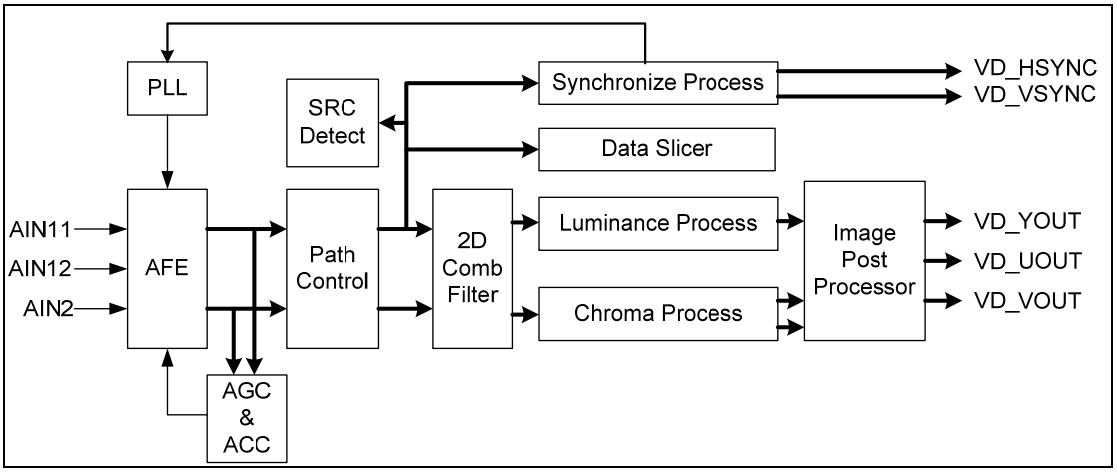


Figure 6-27 Video Decoder Block Diagram

6.28.3 Video Decoder Adjustment

BIT1612 針對內建之 Video Decoder 提供多樣的處理機制，使用者可依據需求針對影像作調整，以獲得最佳之顯示效果。相關架構請參考下列小節。

6.28.3.1 Brightness and Contrast

BIT1612 針對 Y Domain 做 Brightness 和 Contrast 的調整。其相對應設定如下所示。

Table 6-40 Color Adjustment Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BRIGHTNESS_VD	0x0A8[7:0]	RW	8	Brightness Value	0x8A
R_CONTRAST_VD	0x0A9[7:0]	RW	8	Contrast Value	0x71
R_BLACKLEVEL_VD	0x0AA[7:0]	RW	8	Black Level Value	0x80

6.28.3.2 Sharpness Process

BIT1612 針對 Y Domain Data 提供 Sharpness 處理，可強化影像之銳利度，其相對應設定如下所示。

Table 6-41 Sharpness and Smoothness Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UNSHARP_VAL_VD	0x0B1[6:0]	RW	7	Sharpness value (0~127) 0x00: Least sharpness 0x7F: Most sharpness	0x00
R_UNSHARP_EN_VD	0x0B1[7]	RW	1	Sharpness Enable 0: Disable 1: Enable	0
R_UNSHARP_THD_VD	0x0B2[5:0]	RW	6	Sharpness Threshold Value	0x00

6.28.3.3 UV Gain, Saturation and Kill Color

BIT1612 針對 UV Domain Data 提供 UV gain、Saturation、Hue 和 Kill Color 的處理，可讓使用者依喜好調到較佳的色彩影像，其相對應設定如下所示。

Table 6-42 UV Domain Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UGAIN_VD	0x0AC[7:0]	RW	8	U Gain Value Adjustment	0x80
R_VGAIN_VD	0x0AD[7:0]	RW	8	V Gain Value Adjustment	0x80
R_SAT_MODE_VD	0x0AE[7]	RW	1	SAT Adjust Control 0: Normal 1: Simultaneously adjust R_SAT_U_VD and R_SAT_V_VD (From R_SAT_U_VD)	1
R_SAT_U_VD	0x0AE[6:0]	RW	7	U Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_SAT_V_VD	0x0AF[6:0]	RW	7	V Saturation Value (0.0 ~ 1.9843) 0x00=0.0, 0x40=1.0, 0x7F=1.9843	0x40
R_CHROMA_HUE_VD	0x0AB[7:0]	RW	8	Chrominance HUE control 01111111: +178.6° 0000000: 0° 1000000: -180°	0x00
R_KILL_COLOR_VD	0x0B3[7]	RW	1	Control Kill Color enable 0: Disable 1: Enable	0
R_VDLY_VD	0x0B0[1:0]	RW	2	V Data Delay 00: Delay 0 01: Delay 1 10: Delay 2 11: Delay 3	01
R_UDLY_VD	0x0B0[3:2]	RW	2	U Data Delay 00: Delay 0 01: Delay 1 10: Delay 2 11: Delay 3	01

6.28.3.4 Chroma Transient Improvement (CTI)

BIT1612 提供Chroma Transient Improvement (CTI)，相關Registers請參考 Table 6-43。

Table 6-43 Chroma Transient Improvement Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CTI_THD_VD	0x0B4[7:0]	RW	8	CTI Process Threshold Value	0x10
R_CTI_EN_VD	0x0B3[0]	RW	1	CTI Enable 0: Disable 1: Enable	0
R_CTI_USEL_VD	0x0B3[3:1]	RW	3	CTI Level Selection for U Domain 000: Least CTI Enhancement 111: Most CTI Enhancement	001
R_CTI_VSEL_VD	0x0B3[6:4]	RW	3	CTI Level Selection for V Domain 000: Least CTI Enhancement 111: Most CTI Enhancement	001

6.28.4 Synchronization Process

Synchronization Process Block 從 Y/C 分離後的 Luminance 的信號中，分離解出 HSYNC 和 VSYNC 的信號。

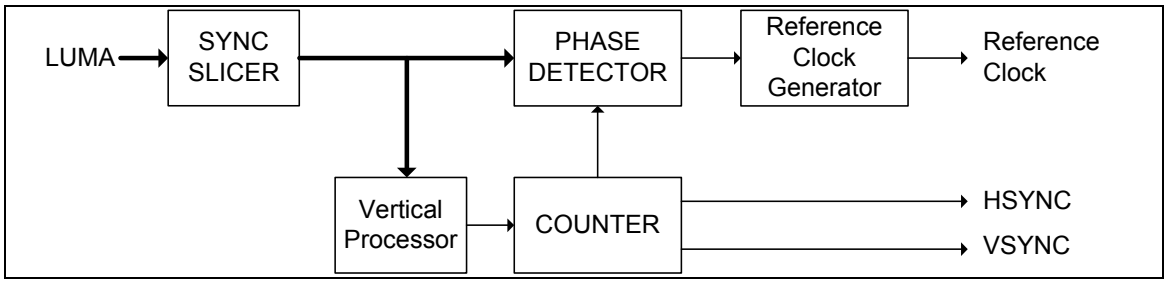


Figure 6-28 Synchronization Process

Table 6-44 Synchronization Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SYNC_IDEL	0x0B5[7:0]	RW	8	Horizontal Increment Delay	0x4A
R_SYNC_HSYS	0x0B6[7:0]	RW	8	Horizontal Sync Start	0x2F
R_SYNC_HSYE	0x0B7[7:0]	RW	8	Horizontal Sync End	0xFF
R_SYNC_HCS	0x0B8[7:0]	RW	8	Clamp Signal Start	0xF2
R_SYNC_HCE	0x0B9[7:0]	RW	8	Clamp Signal End	0xC0
R_SYNC_HSS	0x0BA[7:0]	RW	8	Horizontal Delay	0xFD
R_BGPU_POINT_N	0x0BB[7:0]	RW	8	Burst Start Point for 60Hz Signal	0x06
R_BGPU_POINT_P	0x0BC[7:0]	RW	8	Burst Start Point for 50Hz Signal	0x16
R_SLICER_THD	0x0BD[7:0]	RW	8	Sync-Slicer Threshold	0x00
R_VNOISE_MODE	0x0BE[1:0]	RW	2	VSYNC Noise Reduction Mode 00: Normal Mode 01: Fast Mode 10: Free-Run Mode 11: Bypass Mode	01
R_FIDT_THD	0x0BE[7:4]	RW	4	50/60Hz Detection Threshold	0x8
R_SYNC_LPADJ	0x0BF[1:0]	RW	2	Loop Filter Tracker Speed	11
R_SYNC_PDGAIN	0x0BF[3:2]	RW	2	Loop Filter Phase Tracker Factor	11
R_SYNC_LPLMT	0x0BF[4]	RW	1	Loop Filter Phase Adjustment Speed	0
R_SYNC_HPLL	0x0BF[6:5]	RW	2	PLL Free-Run Mode Enable 00: Free-Run on 23.928MHz 01: Disable (Normal) 10: Free-Run on 27MHz 11: Free-Run on 30.07MHz	01
R_VTRC	0x0BF[7]	RW	1	VCR Mode Enable 0: Disable 1: Enable	0

6.28.5 VBI Data Slicer

BIT1612 提供 Data Slicer 功能可依據針對所設定的 Lines 及 Even/Odd，分離出 16 Bits 的 Data，並且經由 Interrupt 及 Register 提供 MCU 做後續處理，相關的 Registers 請參考下表。

Table 6-45 VBI Data Slicer Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DATA_SLICER_THD	0x0C0[7:0]	RW	8	Data Slicer High/Low Threshold	0x26
R_DATA_SLICER_START	0x0C1[7:0]	RW	8	Data Slicer Start Point	0x99
R_DATA_SLICER_LINE_E	0x0C2[5:0]	RW	6	Data Slicer Line Selection for Even Field	0x11
R_DATA_SLICER_EN_E	0x0C2[7]	RW	1	Data Slicer Enable for Even Field 0: Disable 0: Enable	1
R_DATA_SLICER_LINE_O	0x0C3[5:0]	RW	6	Data Slicer Line Selection for Odd Field	0x10
R_DATA_SLICER_EN_O	0x0C3[7]	RW	1	Data Slicer Enable for Odd Field 0: Disable 0: Enable	1
R_CC_DATA_SEL	0x17C[7]	RW	1	Data Slicer Output (0x17A, 0x17B) Selection 0: Even Field 1: Odd Field	0
R_CC_DATA1	0x17A[7:0]	R	8	Data Slicer First Byte	-
R_CC_DATA2	0x17B[7:0]	R	8	Data Slicer Second Byte	-

6.28.6 Source Detection

BIT1612 提供 Source Detection 的功能可以自動偵測 AIN11 (SRC11)、AIN12 (SRC12)和 AIN2 (SRC2)何者輸入有信號的變化，偵測的結果將經由 Interrupt 提供系統使用，相關的 Registers 設定請參考下表。

Table 6-46 Source Detection Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CH2_THD	0x0C4[1:0]	RW	2	Signal detection threshold for AIN2	00
R_CH12_THD	0x0C4[3:2]	RW	2	Signal detection threshold for AIN12	00
R_CH11_THD	0x0C4[5:4]	RW	2	Signal detection threshold for AIN11	00
R_SRCDET_MODE	0x0C4[7]	RW	1	Source Detection Mode 0: Disable (Normal Mode) 1: Source Detection Mode	0
R_SRC2	0x178[4]	R	1	Source detection result for AIN2	-
R_SRC12	0x178[5]	R	1	Source detection result for AIN12	-
R_SRC11	0x178[6]	R	1	Source detection result for AIN11 0: No signal toggle 1: Signal toggle	-

6.28.7 Luminance Process

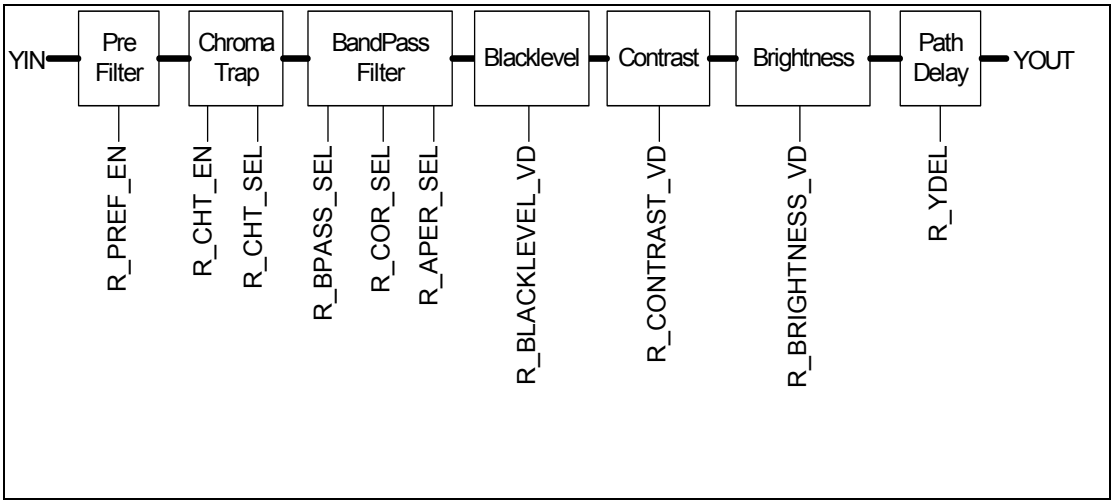


Figure 6-29 Luminance Process Block

Table 6-47 Luminance Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BPASS_SEL	0x0C5[1:0]	RW	2	Band Pass Frequency Selection 00: Frequency 1 01: Frequency 2 10: Frequency 3 11: Frequency 4	00
R_COR_SEL	0x0C5[3:2]	RW	2	Coring circuit amplitude value 00: Coring factor 1 01: Coring factor 2 10: Coring factor 3 11: Coring factor 4	00
R_APER_SEL	0x0C5[5:4]	RW	2	Aperture Factor 00: 0 01: 0.25 10: 0.5 11: 1.0	00
R_CHT_EN	0x0F0[5]	RW	1	Chroma Trap Enable 0: Disable 1: Enable	1
R_CHT_SEL	0x0C5[7]	RW	1	Chroma-Trap Control (Internal Test) 0: Type 1 1: Type 2	1
R_PREF_EN	0x0C5[6]	RW	1	Luma Pre-Filter Enable 0: Disable 1: Enable	0
R_YDEL	0x0C6[3:0]	RW	4	Y Data Path Delay 1111: Delay 16 Clocks 1000: Delay 0 Clock 0000: Delay -15 Clocks	0x8

6.28.8 Chroma Process

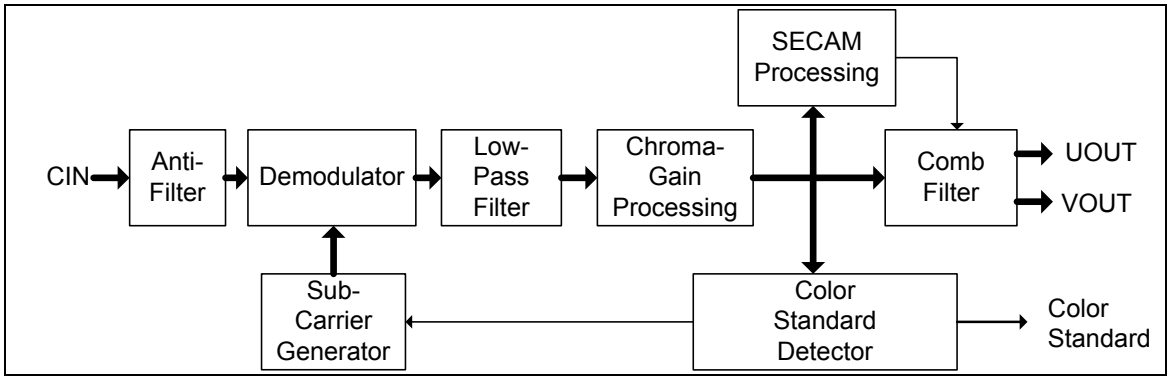


Figure 6-30 Chroma Process Function Block

Table 6-48 Chroma Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CHROMA_GAIN	0x0C7[6:0]	RW	7	Chroma Fixed-Gain Value 000000: Minimum Gain (0.25) 010000: Normal Gain (1.0) 111111: Maximum Gain (3.5)	0x21
R_CHROMA_GAIN_SEL	0x0C7[7]	RW	1	Chroma Gain Type Selection 0: Auto-Gain 1: Fixed-Gain (Defined on 0x609[6:0])	0
R_GAIN_CTL_VALUE	0x0C9[0], 0x0C8[7:0]	RW	9	Chroma Gain Reference Value	0x100
R_AUTO_KILL	0x0C9[1]	RW	1	Auto Color Kill From Color Detection 0: Disable 1: Enable (Auto Kill from Color Detection)	0
R_CDV_SEL	0x0C9[2]	RW	1	TV / VCR Mode Selection 0: Mode 1 1: Mode 2	0
R_CCIR_EN	0x0C9[3]	RW	1	CCIR Mode 0: Disable 1: Enable	0
R_GAIN_CTRL_SPEED	0x0C9[5:4]	RW	2	Auto Chroma Gain Loop Filter 00: Slow Time Constant 01: Medium Time Constant 10: Fast Time Constant 11: Frozen	00
R_SECAM_INVERT	0x0C9[6]	RW	1	SECAM Invert Enable 0: Disable 1: Enable	0
R_SXCR	0x0C9[7]	RW	1	SECAM Cross Color Reduction 0: Disable 1: Enable	1
R_THRESHOLD_SECAM	0x0CA[7:0]	RW	8	Color Killer Threshold for SECAM	0x80
R_THRESHOLD_QAM	0x0CB[7:0]	RW	8	Color Killer Threshold for PAL and NTSC	0x80
R_SECAM_SENSITIVE	0x0CC[7:0]	RW	8	SECAM Switch Sensitive Level	0x50
R_PAL_SENSITIVE	0x0CD[7:0]	RW	8	PAL Switch Sensitive Level	0x50
R_LOWER_BOUND	0x0CE[3:0]	RW	4	Color Standard Detection Threshold 1	0x4
R_UPPER_BOUND	0x0CE[7:4]	RW	4	Color Standard Detection Threshold 2	0xC
R_CHROMA_LPPI1	0x0CF[1:0]	RW	2	Chroma Low Pass Filter Factor 1	01
R_CHROMA_LPPI2	0x0CF[3:2]	RW	2	Chroma Low Pass Filter Factor 2	10
R_SQP_LMT	0x0CF[4]	RW	1	Sub-Carrier Frequency Selection	0

				0: Type 1 1: Type 2	
R_SQP_LPPI	0x0CF[6:5]	RW	2	Sub-Carrier Phase Detection Factor 1	01
R_SQP_SPUP	0x0CF[7]	RW	1	Sub-Carrier Phase Detection Factor 2	0
R_STD_COUNT	0x0D0[5:0]	RW	6	Color Standard Detect Ready Threshold	0x38
R_CHROMA_PHASE	0x0D0[6]	RW	1	Chroma Phase Detection Mode 0: Mode 1 1: Mode 2	0
R_STD_OFF00	0x0D1[7:0]	RW	8	Burst Freq. Offset for 3.57MHz	0x00
R_STD_OFF01	0x0D2[7:0]	RW	8	Burst Freq. Offset for 4.2MHz	0x08
R_STD_OFF10	0x0D3[7:0]	RW	8	Burst Freq. Offset for 4.43MHz	0x00

6.28.9 Comb Filter Process

BIT1612 Video Decoder 提供 NTSC 3-Line 和 PAL 5-Line 的 Adaptive Comb Filter 來做 Y/C 分離，其相關設定請參考下表。

Table 6-49 Comb Filter Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_COMB_EN	0x0F0[6]	RW	1	Comb Filter Enable 0: Disable 1: Enable	0
R_COMB_CTHD	0x0D4[6:0]	RW	7	C Threshold Value	0x20
R_COMB_YTHD12	0x0D5[7:0]	RW	8	Y Threshold Value for NTSC: Abs (Line0-Line1) or Abs (Line1-Line2) PAL: Abs (Line0-Line2) or Abs (Line2-Line4)	0x20
R_COMB_YTHD3	0x0D6[7:0]	RW	8	Y Threshold Value for NTSC: Abs (Line0-Line2) PAL: Abs (Line0-Line4)	0x10
R_LINE_THD1	0x0D7[7:0]	RW	8	Y Line Threshold1 Value	0x10
R_LINE_THD2	0x0D8[7:0]	RW	8	Y Line Threshold2 Value	0x0A
R_SECS_AUTOSW	0x0D9[0]	RW	1	SECAM Standard Control 0: Force 1 D 1: Auto	1
R_N44360_AUTOSW	0x0D9[1]	RW	1	NTSC_4.43MHz_60Hz Standard Control 0: Force 1 D 1: Auto	1
R_NOCOR_AUTOSW	0x0D9[2]	RW	1	No Color Burst Control 0: Force 1 D 1: Auto	1
R_OUT_SEL	0x0D9[5:4]	RW	2	Middle Filter Selection 00: Mode0 01: Mode1 10: Mode2 11: Mode3	00
R_Y_SEL	0x0DA[1:0]	RW	2	Y Domain Force 1D Filter Selection (when R_Y_AUTO = 0) 00: Notch Filter 01: Two-Line Filter (Mode 0) 10: Two-Line Filter (Mode 1) 11: Three-Line Filter	00
R_Y_AUTO	0x0DA[2]	RW	1	Y Domain Comb Filter Enable 0: Fixed Filter 1: Adaptive Comb Filter	1
R_Y1D_SEL	0x0DA[5:4]	RW	2	Y Domain Notch Filter Selection 00: Type 0 01: Type 1	00

				10: Type 2	
				11: Type 3	
R_CP90_SEL	0x0DB[2:0]	RW	3	C Domain Force 1D Filter Selection (Phase 90)	010
				000: High Pass Filter	
				001: Two-Line Filter (Mode 2)	
				01x: Two-Line Filter (Mode 0)	
				10x: Two-Line Filter (Mode 1)	
				11x: Three-Line Filter	
R_CP90_AUTO	0x0DB[3]	RW	1	C Domain Comb Filter Enable (Phase 90)	1
				0: Fixed Filter	
				1: Adaptive Comb Filter	
R_CP180_SEL	0x0DB[6:4]	RW	3	C Domain Force 1D Filter Selection (Phase 180)	010
				000: High Pass Filter	
				001: Two-Line Filter (Mode 2)	
				01x: Two-Line Filter (Mode 0)	
				10x: Two-Line Filter (Mode 1)	
				11x: Three-Line Filter	
R_CP180_AUTO	0x0DB[7]	RW	1	C Domain Comb Filter Enable (Phase 180)	1
				0: Fixed Filter	
				1: Adaptive Comb Filter	
R_CP90TAB_SEL	0x0DC[1:0]	RW	2	C Domain Filter Table Selection (Phase 90)	11
				00: Table 0	
				01: Table 1	
				10: Table 2	
				11: Table 3	
R_CREFY_EN	0x0DC[4]	RW	1	C Domain Refers to Y Domain	1
				0: Disable	
				1: Enable	
R_YREFC_EN	0x0DC[5]	RW	1	Y Domain Refers to C Domain	1
				0: Disable	
				1: Enable	
R_YP90REF13_EN	0x0DC[6]	RW	1	C Domain Refers to Line2 and Line4 (Phase 90)	1
				0: Disable	
				1: Enable	

6.28.10 AGC and ACC Process

BIT1612 提供 AGC (Auto Gain Control)功能以控制 Analog PGA 所提供 -6db、0db、6db 和 12db 四種的 Gain Value 及 Digital PGA 所提供+18db ~ -18db Linear Digital PGA，及提供 ACC (Auto Clamp Control)功能以控制 Analog Clamp 和 Digital Clamp。AGC 及 ACC 的控制可使輸入信號維持在正常的振幅及準位，使得輸出的結果不會隨著信號的漂移改變而有所變化，進而影響畫面的穩定度。相關的示意圖請參考下圖，相關的 Registers 設定請參考下表。

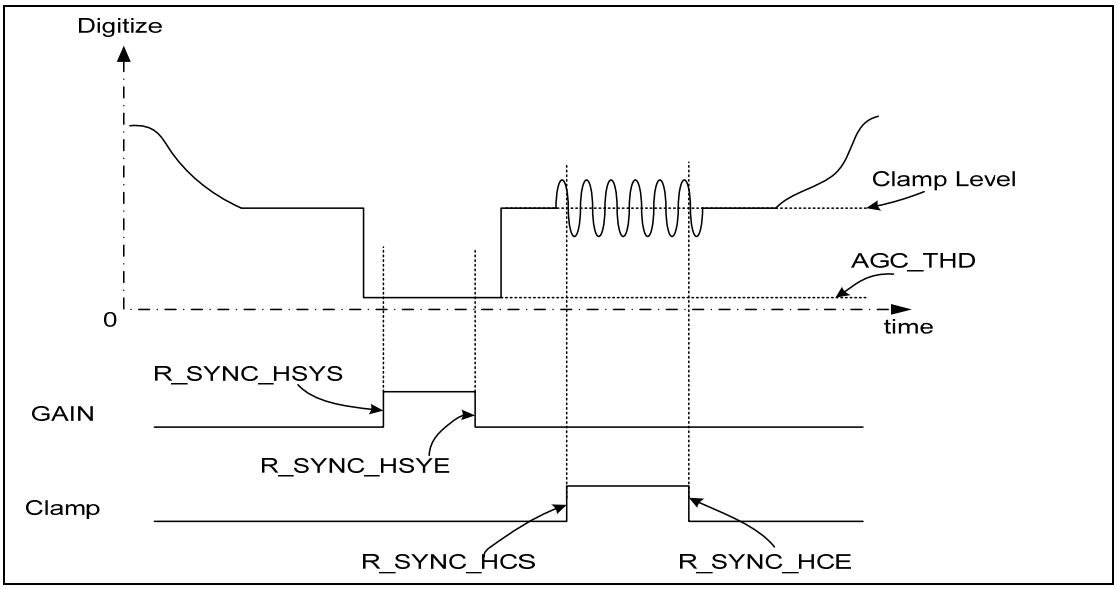


Figure 6-31 AGC and Clamp Pulse

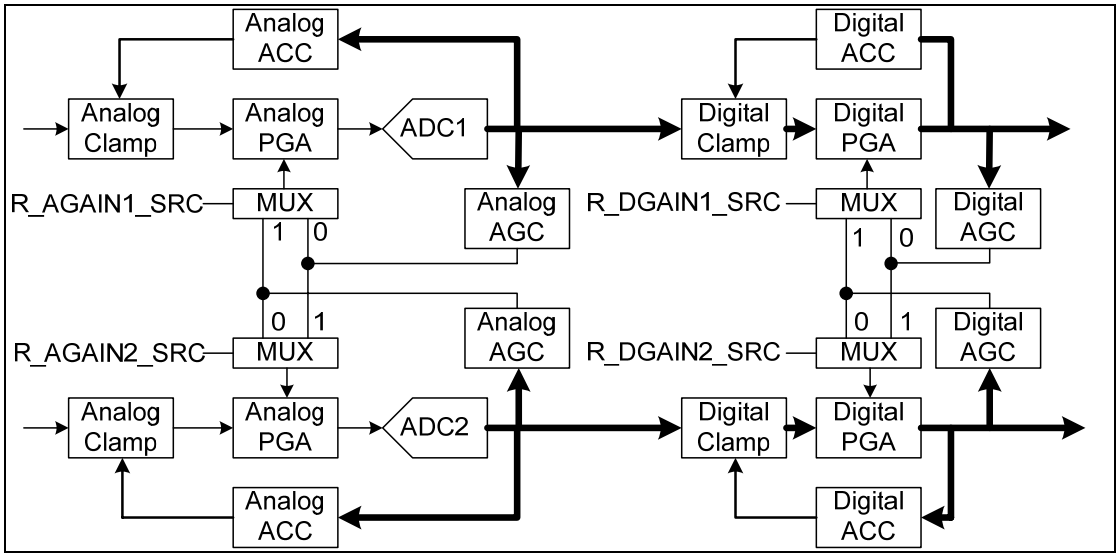


Figure 6-32 AGC Control Selection

Table 6-50 AGC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ACLAMP_SPEED	0x0DD[7:0]	RW	8	Analog Clamp Tracer Speed	0x18
R_ACLAMP1_LEVEL	0x0DE[7:0]	RW	8	Analog Clamp 1 Level	0x30
R_ACLAMP2_LEVEL	0x0DF[7:0]	RW	8	Analog Clamp 2 Level	0x80
R_AAGC1_EN	0x0E0[0]	RW	1	Analog AGC Enable for ADC1 0: Disable (R_AAGC1_VALUE) 1: Enable (Auto Tracer)	1

R_AAGC1_HOLD	0x0E0[1]	RW	1	Analog AGC Hold for ADC1 0: Disable (Tracer) 1: Enable (Hold)	0
R_AAGC1_VALUE	0x0E0[3:2]	RW	2	Analog PGA 1 Value when AGC Disable 00: -6 db (x0.5) 01: 0 db (x1) 10: 6 db (x2) 11: 12 db (x4)	10
R_ACLAMP1_EN	0x0E0[4]	RW	1	Analog Clamp 1 Enable 0: Disable (Turn Off Analog Clamp) 1: Enable	1
R_ACLAMP1_TYPE	0x0E0[5]	RW	1	Analog Clamp 1 Level Selection 0: R_ACLAMP1_LEVEL 1: Middle Level	0
R_SYNC1_CLAMP	0x0E0[6]	RW	1	Analog Clamp 1 Update Signal 0: VSYNC 1: HSYNC	1
R_AUTO1_HOLD	0x0E0[7]	RW	1	Auto ACC and AGC Hold when Tracer Stable for ADC 1 0: Disable 1: Enable	0
R_DAGC1_EN	0x0E1[0]	RW	1	Digital AGC Enable for ADC 1 0: Disable (R_DAGC1_VALUE) 1: Enable (Auto Tracer)	1
R_DAGC1_HOLD	0x0E1[1]	RW	1	Digital AGC Hold for ADC 1 0: Disable (Tracer) 1: Enable (Hold)	0
R_DCLAMP1_EN	0x0E1[2]	RW	1	Digital Clamp 1 Enable 0: Disable (R_DCLAMP1_VALUE) 1: Enable	1
R_DCLAMP1_HOLD	0x0E1[3]	RW	1	Digital ACC Hold for ADC1 0: Disable (Tracer) 1: Enable (Hold)	0
R_DAGC1_THD	0x0E1[7:4]	RW	4	Digital AGC 1 Tracer Level	0x1
R_DAGC1_VALUE	0x0E2[7:0]	RW	8	Manual Digital AGC 1 value	0x40
R_DCLAMP1_LEVEL	0x0E3[7:0]	RW	8	Digital Clamp 1 Level	0x3F
R_DCLAMP1_VALUE	0x0E4[7:0]	RW	8	Manual Digital Clamp 1 Value	0x00
R_DAGC1_SPEED	0x0E5[5:0]	RW	6	Digital AGC 1 Tracer Speed	0x04
R_DIFFGAIN1_THD	0x0E5[7:6]	RW	2	AGC and ACC Ready Threshold for ADC 1	00
R_DAGC1_VSUP	0x0EE[6]	RW	1	Digital AGC 1 Update Signal 0: HSYNC 1: VSYNC	1
R_DAGC2_VSUP	0x0EE[7]	RW	1	Digital AGC 2 Update Signal 0: HSYNC 1: VSYNC	1
R_AAGC2_EN	0x0E6[0]	RW	1	Analog AGC Enable for ADC 2 0: Disable (R_AAGC2_VALUE) 1: Enable (Auto Tracer)	1
R_AAGC2_HOLD	0x0E6[1]	RW	1	Analog AGC Hold for ADC 2 0: Disable (Tracer) 1: Enable (Hold)	0
R_AAGC2_VALUE	0x0E6[3:2]	RW	2	Analog PGA 2 Value when AGC Disable 00: -6 db (x0.5) 01: 0 db (x1) 10: 6 db (x2)	10

				11: 12 db (x4)	
R_ACLAMP2_EN	0x0E6[4]	RW	1	Analog Clamp 2 Enable 0: Disable (Turn Off Analog Clamp) 1: Enable	1
R_ACLAMP2_TYPE	0x0E6[5]	RW	1	Analog Clamp 2 Level Selection 0: R_ACLAMP2_LEVEL 1: Middle Level	1
R_SYNC2_CLAMP	0x0E6[6]	RW	1	Analog Clamp 2 Update Signal 0: VSYNC 1: HSYNC	1
R_AUTO2_HOLD	0x0E6[7]	RW	1	Auto ACC and AGC Hold when Tracer Stable for ADC 2 0: Disable 1: Enable	0
R_DAGC2_EN	0x0E7[0]	RW	1	Digital AGC Enable for ADC2 0: Disable (R_DAGC2_VALUE) 1: Enable (Auto Tracer)	1
R_DAGC2_HOLD	0x0E7[1]	RW	1	Digital AGC Hold for ADC2 0: Disable (Tracer) 1: Enable (Hold)	0
R_DCLAMP2_EN	0x0E7[2]	RW	1	Digital Clamp 2 Enable 0: Disable (R_DCLAMP2_VALUE) 1: Enable	1
R_DCLAMP2_HOLD	0x0E7[3]	RW	1	Digital ACC Hold for ADC 2 0: Disable (Tracer) 1: Enable (Hold)	0
R_DAGC2_THD	0x0E7[7:4]	RW	4	Digital AGC 2 Tracer Level	0x1
R_DAGC2_VALUE	0x0E8[7:0]	RW	8	Manual Digital AGC 2 Value	0x40
R_DCLAMP2_LEVEL	0x0E9[7:0]	RW	8	Digital Clamp 2 Level	0x80
R_DCLAMP2_VALUE	0x0EA[7:0]	RW	8	Manual Digital Clamp 2 Value	0x00
R_DAGC2_SPEED	0x0EB[5:0]	RW	6	Digital AGC 2 Tracer Speed	0x04
R_DIFFGAIN2_THD	0x0EB[7:6]	RW	2	AGC and ACC Ready Threshold for ADC 2	00

6.28.11 AFE and PLL Control

BIT1612 內建 AFE (Analog Front End) 設定參數，相關設定請參考下表。

Table 6-51 ADC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AFE_CS	0x0EC[1:0]	RW	2	AFE Clamp Current	00
R_AFE_CTRPH	0x0EC[3:2]	RW	2	AFE Phase Non-Overlap Time	00
R_AFE_CTRIB	0x0EC[6:4]	RW	3	AFE Bias Current Control	110
R_AFE_SH2VCM	0x0EC[7]	RW	1	AFE Internal Shortcut On both PGA	0
R_AFE_ENIB	0x0ED[0]	RW	1	AFE Bias Current Enable	1
R_AFE_ENREF	0x0ED[1]	RW	1	AFE Reference Generator Enable	1
R_AFE_ENVBG	0x0ED[2]	RW	1	AFE Bandgap Generator Enable	1
R_AFE_ENVCM	0x0ED[3]	RW	1	AFE Common Mode Voltage Generator Enable	1
R_AFE_ENAY	0x0ED[4]	RW	1	Power Down Input for ADC 1 0: Power Down 1: Normal Operation	1
R_AFE_ENAC	0x0ED[5]	RW	1	Power Down Input for ADC 2 0: Power Down 1: Normal Operation	1
R_AFE_BYP	0x0ED[6]	RW	1	Bypass PGA for ADC Test	0
R_AFE_DEC	0x0ED[7]	RW	1	Control Output Data Decimator by 8 or None (Dec = 0: Normal Operation)	0
R_PLL_POR	0x0EE[0]	RW	1	PLL Power On Reset 0: Disable 1: Reset	0
R_PLL_EAPLL	0x0EE[1]	RW	1	PLL Enable 0: Disable 1: Enable	1
R_PLL_ICP0	0x0EE[2]	RW	1	PLL Factor 0	0
R_PLL_ICP1	0x0EE[3]	RW	1	PLL Factor 1	0
R_PLLDTO_ROL	0x0EE[4]	RW	1	PLL DTO Rotate 0: Disable 1: Enable	0

6.28.12 Input Path Selection

BIT1612 Video Decoder內建兩組 10 Bits ADC，提供三組Analog信號輸入端，並可經由Register設定，以支援CVBS、Y/C及YPbPr (480i or 576i) 的信號輸入，其相關架構示意圖請參考下圖，相關Registers設定請參考 Table 6-52 及 Table 6-53。

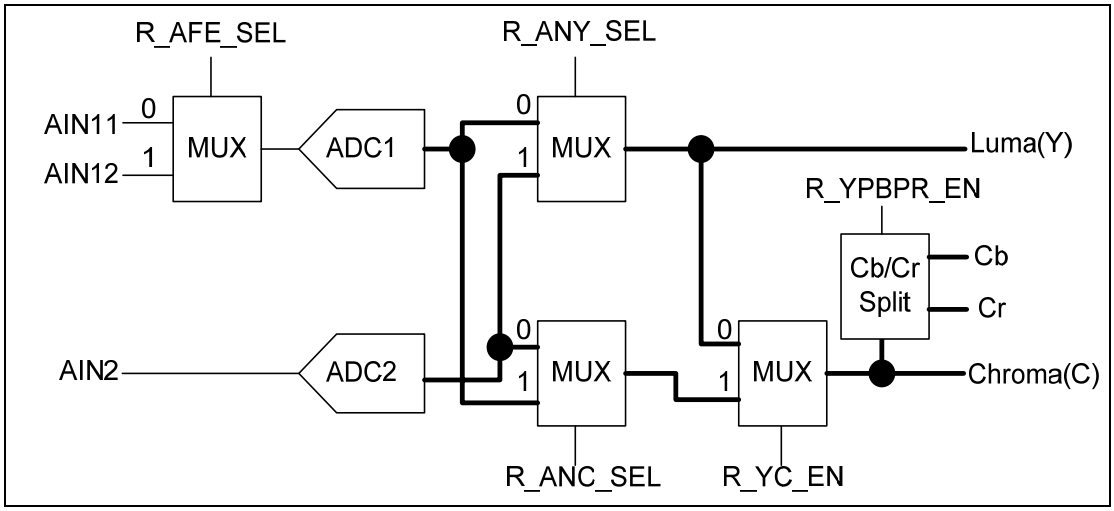


Figure 6-33 Input Path

Table 6-52 Analog Input Path Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_ANC_SEL	0x0F0[0]	RW	1	Chroma Path Selection 0: Data Source form ADC2 1: Data Source from ADC1	0
R_ANY_SEL	0x0F0[1]	RW	1	Luma Path Selection 0: Data Source from ADC1 1: Data Source from ADC2	0
R_AFE_SEL	0x0F0[2]	RW	1	Video MUX Switch for ADC1 0: ADC1 Signal from AIN11 Pin 1: ADC1 Signal from AIN12 Pin	0
R_YC_EN	0x0F0[3]	RW	1	Y/C Mode Enable 0: Disable 1: Enable	0
R_YPBPR_EN	0x0F0[4]	RW	1	YPbPr Mode Enable 0: Disable 1: Enable	0

Table 6-53 Analog Input Selection					
Mode	R_ANC_SEL	R_ANY_SEL	R_AFE_SEL	R_YC_EN	R_YPBPR_EN
CVBS Mode: Signal Input from AIN11	0/1	0	0	0	0
CVBS Mode: Signal Input from AIN12	0/1	0	1	0	0
CVBS Mode: Signal Input from AIN2	0/1	1	0/1	0	0
Y/C Mode: Y Signal Input from AIN11 C Signal Input from AIN2	0	0	0	1	0
Y/C Mode: Y Signal Input from AIN12 C Signal Input from AIN2	0	0	1	1	0

Y/C Mode: Y Signal Input from AIN2 C Signal Input from AIN11	1	1	0	1	0
Y/C Mode: Y Signal Input from AIN2 C Signal Input from AIN12	1	1	1	1	0
YPbPr Mode: Y Signal Input from AIN2 Pb Signal Input from AIN11 Pr Signal Input from AIN12	1	1	0/1	1	1

6.28.13 Standard Setting and Detection

BIT1612 可以針對PAL、PAL60、PAL-N、SECAM、PAL-M、NTSC-443-50、NTSC-M、NTSC-443-60和Black & White等Color Standard信號進行解碼，並提供自動、半自動和手動三種模式，以便使用者依據其實際環境進行設定。相關架構示意圖請參考下圖，相關Registers設定請參考 Table 6-54。

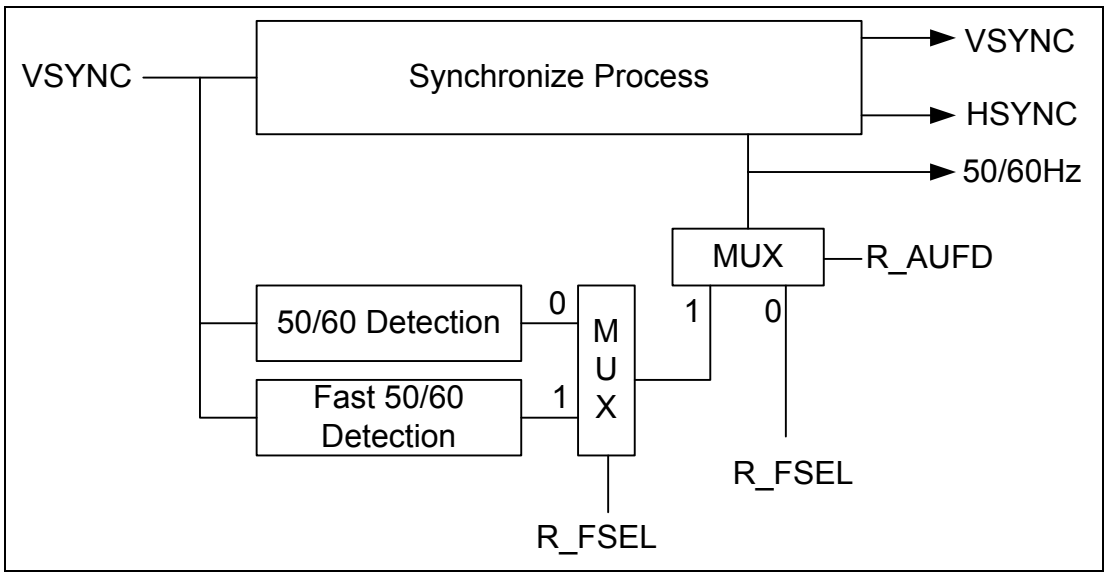


Figure 6-34 Field Type Selection

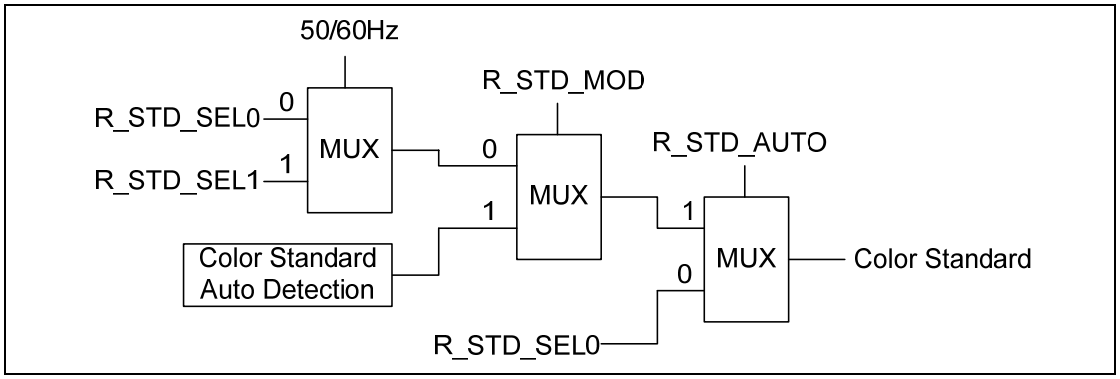


Figure 6-35 Color Standard Selection

Table 6-54 Standard Setting and Detection Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_AUFD	0x0F1[0]	RW	1	Auto 50/60Hz Detection 0: Manual 50/60Hz (Defined on 0x0F1[1]) 1: Auto 50/60Hz Detection	0
R_FSEL	0x0F1[1]	RW	1	Manual 50/60Hz Mode (R_AUFD=0)	0

				0: 50Hz 1: 60Hz Auto 50/60Hz Detection Mode (R_AUFD=1) 0: Normal Mode 1: Fast Mode	
R_STD_AUTO	0x0F1[2]	RW	1	Color Standard Detection 0: Manual Color Standard (Defined on 0x0F1[6:4]) 1: Auto Color Standard	0
R_STD_MOD	0x0F1[3]	RW	1	Auto Color Standard Detection Mode Selection 0: Semi-Auto Mode 1: Fully-Auto Mode	0
R_STD_SEL0	0x0F1[6:4]	RW	3	Color Standard Setup for Manual Setting and Semi-Auto on 50Hz	000
R_STD_SEL1	0x0F2[2:0]	RW	3	Color Standard Setup for Semi-Auto on 60Hz 000: PAL/PAL-60 001: PAL_N 010: SECAM 011: PAL_M 100: NTSC_4.43_50Hz 101: NTSC_M / NTSC_J 110: NTSC_4.43_60Hz 111: Black & White	101

6.29 Video Decoder Status Register

BIT1612 Built-In Video Decoder 提供下列 Read Only Registers，以便讀取 BIT1612 內部 Status，相關 Registers 請參考下表。

Table 6-55 Video Decoder Status Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DAGC1_OUT	0x16E[7:0]	R	8	Digital AGC1 Tracer Value	-
R_DCLAMP1_OUT	0x16F[7:0]	R	8	Digital Clamp1 Tracer Value	-
R_DAGC2_OUT	0x170[7:0]	R	8	Digital AGC2 Tracer Value	-
R_DCLAMP2_OUT	0x171[7:0]	R	8	Digital Clamp2 Tracer Value	-
R_AAGC1_OUT	0x172[1:0]	R	2	Analog ACG1 Tracer Value	-
R_AAGC2_OUT	0x172[3:2]	R	2	Analog AGC2 Tracer Value	-
R_CHROMA_GAINOUT	0x172[7:4], 0x173[7:0]	R	12	Chroma GAIN Tracer Value	-
R_COLOR_STANDARD	0x174[2:0]	R	3	Color Standard Detection Result 000: PAL 001: PAL_N 010: SECAM 011: PAL_M 100: NTSC_4.43_50Hz 101: NTSC_M / NTSC_J 110: NTSC_4.43_60Hz 111: Black & White	-
R_FIDT_O	0x174[3]	R	1	50/60Hz Detection 0: 50Hz 1: 60Hz	-
R_HLCK_O	0x174[4]	R	1	H-LOCK Ready 0: Not Ready 1: Ready	-
R_SYNC_READY_O	0x174[5]	R	1	Auto Sync Detection Ready	-
R_STD_READY_O	0x174[6]	R	1	Auto Color Standard Detection Ready	-
R_COLORDET	0x174[7]	R	1	Color Detection Result	-

				0: No Color or Low Color 1: Color Source	
R_SQP_COUNT	0x175[3:0]	R	4	Burst Phase Detection	
R_DAGC1_READY	0x175[4]	R	1	AGC1 Tracer Ready	-
R_DAGC2_READY	0x175[5]	R	1	AGC2 Tracer Ready 0: Not Ready 1: Ready	-
R_STD_FREQ	0x175[7:6]	R	2	Color Burst Detection 00: 3.57MHz 01: 4.2MHz 10: 4.3MHz 11: Non-Standard	-
R_INCCHRO_O	0x17C[0],0x177[7:0],0x176[7:0]	R	17	PLL Tracer Value	-
R_MV_DET_SYNC	0x178[0]	R	1	MV Source Detection 0: Not MV source 1: MV Source	-
R_MV_DET_CHROMA	0x178[1]	R	1	MV Source on Chroma 0: Not MV Source 1: MV Source	-
R_MV_TYPE_CHROMA	0x178[2]	R	1	MV Type on Chroma 0: Type 2 1: Type 3	-
R_STD_PHASE	0x178[3]	R	1	Burst Phase Detection 0: 0 – 180 – 0 1: 0 – 90 – 180 – 270 – 0	-
R_SRC2	0x178[4]	R	1	Source Detection Result for AIN2	-
R_SRC12	0x178[5]	R	1	Source Detection Result for AIN12	-
R_SRC11	0x178[6]	R	1	Source Detection Result for AIN11 0: No Signal Toggle 1: Signal Toggle	- - -
R_CC_INT	0x178[7]	R	1	Data Slicer Interrupt 0: No CC Data 1: Has CC Data	-
R_CC_DATA1	0x17A[7:0]	R	8	Data Slicer First Byte	-
R_CC_DATA2	0x17B[7:0]	R	8	Data Slicer Second Byte	-
R_CC_ERROR	0x17C[1]	R	1	Data Slicer Error 0: Normal 1: Error	-

6.30 Serial RGB Output

BIT1612 內建Serial RGB輸出介面，從可以SRGB[8:1] (Pin52~Pin45)輸出數位RGB信號，從RTSx輸出HSYNC、VSYNC、DE等信號，從SRGB_CLK(Pin 54) 輸出Clock信號，符合多種LCD Panel的Serial RGB輸入規格。詳細規格請參考 Table 6-56、Figure 6-36 及 Figure 6-37。

Table 6-56 Serial RGB Output Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SRGB_T_DLY	0x0F3[7:6]	RW	2	Hsync, Vsync, DE Latency Cycle (Tclk)	10
R_SRGB_L_DLY	0x0F3[5:4]	RW	2	Hsync, Vsync, DE Latency Cycle (Lclk)	00
R_SERIAL_DLY	0x0F3[2]	RW	1	Serial Data Delay	0
R_SRGB_4X	0x0F3[1]	RW	1	0: 3T Serial RGB (RGB) 1: 4T Serial RGB (RGBB)	0
R_SRGB_EN	0x0F3[0]	RW	1	Serial RGB Enable 0: Disable 1: Enable	1

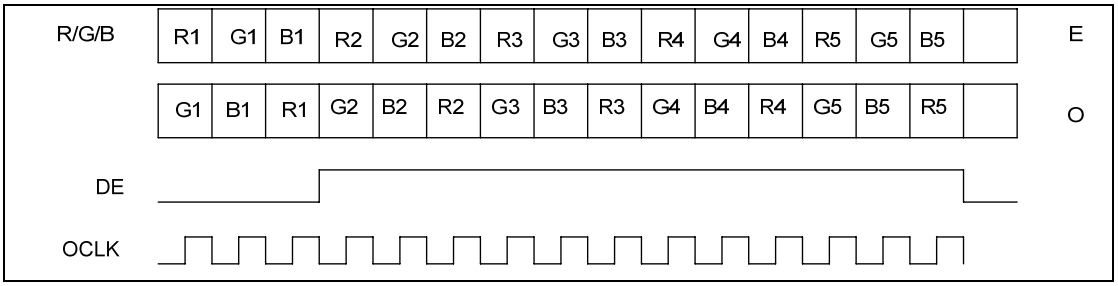


Figure 6-36 UPS051

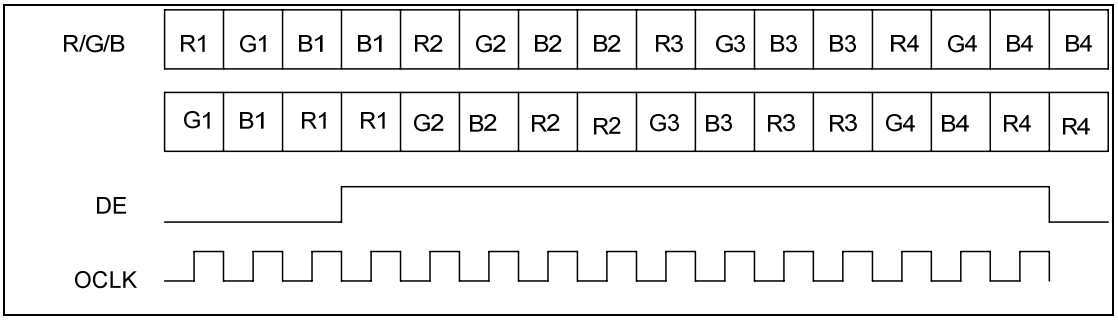


Figure 6-37 UPS052

6.31 BIT1690 Interface

BIT1690 爲 3-Channel Video DAC，可以驅動類比LCD Panel，BIT1612 內建與BIT1690 輸入相容的介面，透過BIT1612 的Register可以直接對BIT1690 進行控制。控制方式請參考 Table 6-57 及 Figure 6-38 和BIT1690 Data Sheet。需特別注意的是，在 0x0F5 的部份，只有當ADDR[2:0]的值有改變時，命令才有效。

Table 6-57 BIT1690 Interface Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SPI1690_DATA	0x0F4[7:0]	RW	8	Write Data	0x00
R_SPI1690_EN	0x0F5[7]	RW	1	BIT1690 Interface – Enable 0: Disable 1: Enable	0
R_SPI1690_RW	0x0F5[6]	RW	1	BIT1690 Interface – Write / Read 0: Write 1: Read	0
R_SPI1690_LSB	0x0F5[5]	RW	1	BIT1690 Interface – Write Data LSB	0

R_SPI1690_DESYNC	0x0F5[4]	RW	1	BIT1690 Interface – CMD Sync	0
R_SPI1690_CHECKER	0x0F5[3]	RW	1	BIT1690 Interface – CMD Checker	0
R_SPI1690_ADDR	0x0F5[2:0]	RW	3	BIT1690 Interface – ADDR	000

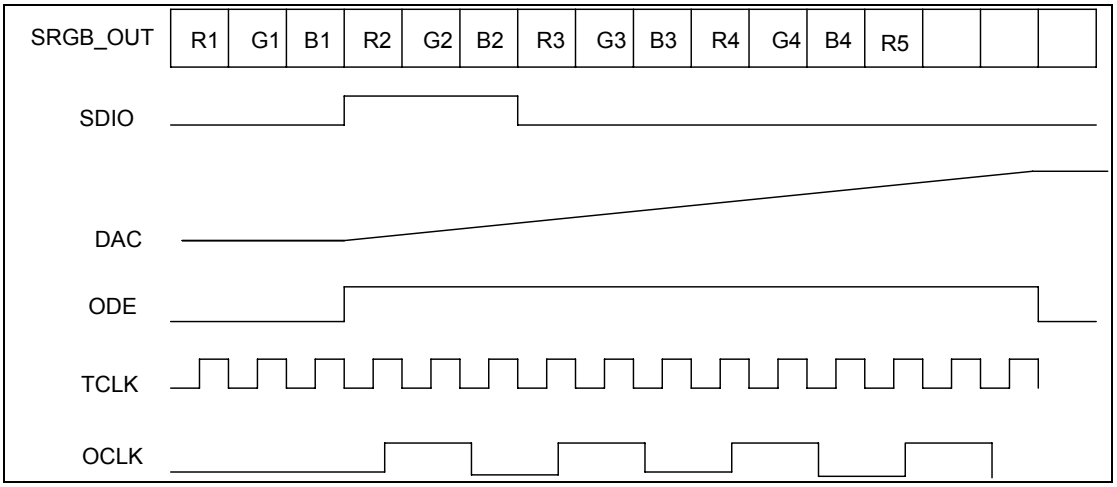


Figure 6-38 BIT1690 Interface

6.32 OSD Function

The embedded OSD supports the following features:

1. Three OSD Windows
2. 128 Fixed FONT ROM / 48 User Programmable FONT RAM
3. 16 Characters Color User Programmable FONT RAM
4. 256 Characters Display RAM
5. Index-Based Display RAM Memory Management
6. Independent Zoom Ratio x0.5~x16 for Horizontal Direction
7. Independent Zoom Ratio x0.5~x8 for Vertical Direction
8. Programmable Vertical Direction Line Space
9. Fade IN/OUT Effect
10. 16 Color Palette Items (64 Colors)
11. Blink Display Effect
12. Fringe Font Effect
13. Fringe Window Effect
14. Vertical and Horizontal Directions Window Overlap
15. External OSD interface

6.32.1 OSD Windows Function

With the embedded OSD, BIT1612 supports at most 3 OSD windows at the same time. Please refer to **Table 6-58** for related registers.

Table 6-58 OSD Windows Register

Mnemonic	Address	R/W	Bits	Description	Default
R_W0_X	0x104[2:0], 0x102[7:0]	RW	11	OSD0 Start X Position	0x196
R_W0_Y	0x104[5:4], 0x103[7:0]	RW	10	OSD0 Start Y Position	0x014
R_W0_W	0x105[6:0]	RW	7	OSD0 Width (in Characters)	0x06
R_W0_H	0x106[5:0]	RW	6	OSD0 Height (in Characters)	0x01
R_W1_X	0x114[2:0], 0x112[7:0]	RW	11	OSD1 Start X Position	0x033
R_W1_Y	0x114[5:4], 0x113[7:0]	RW	10	OSD1 Start Y Position	0x03F
R_W1_W	0x115[6:0]	RW	7	OSD1 Width (in Characters)	0x09
R_W1_H	0x116[5:0]	RW	6	OSD1 Height (in Characters)	0x06
R_W2_X	0x124[2:0], 0x122[7:0]	RW	11	OSD2 Start X Position	0x080

R_W2_Y	0x124[5:4], 0x123[7:0]	RW	10	OSD2 Start Y Position	0x0D2
R_W2_W	0x125[6:0]	RW	7	OSD2 Width (in Characters)	0x14
R_W2_H	0x126[5:0]	RW	6	OSD2 Height (in Characters)	0x00

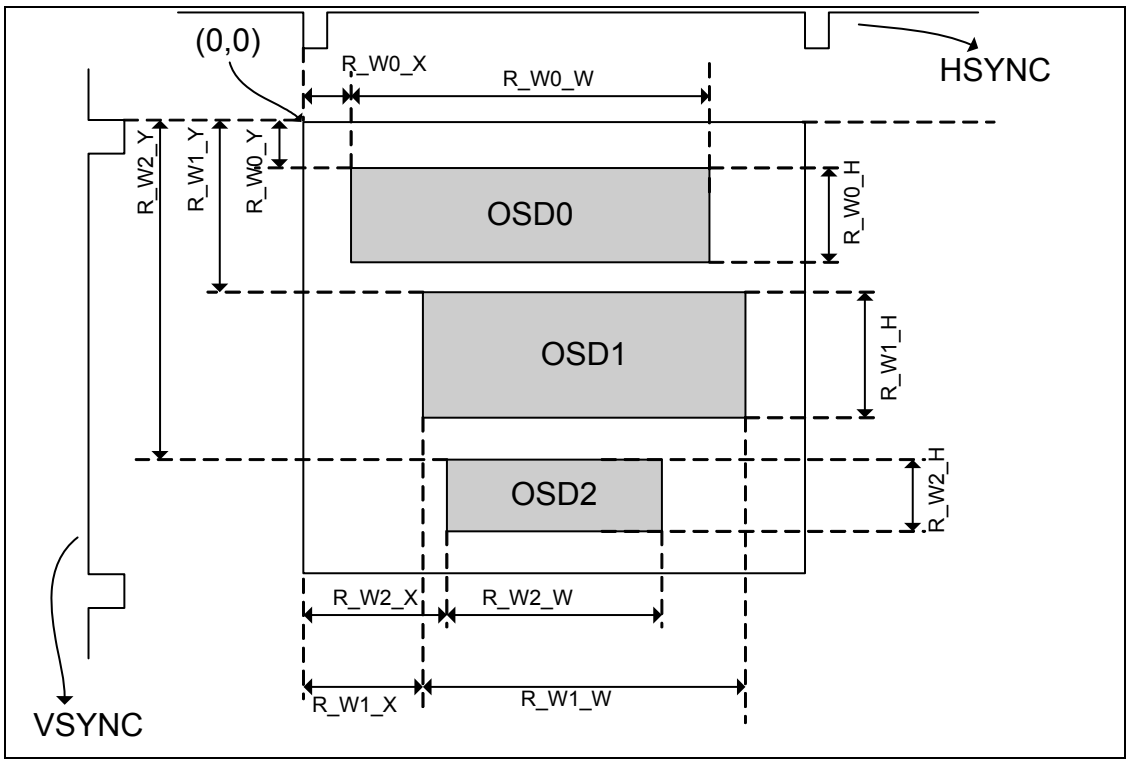


Figure 6-39 OSD Windows Setup

6.32.2 OSD Memory Mapping

OSD的架構如 Figure 6-39 所示：

使用 R_Wx_INDEXS 和 R_Wx_INDEXE 來指出要由 Display RAM 的第幾個 ”WORD” 開始取 Data (同時取用 0x5xx 和 0x4xx 相對應的 Data)，其中 0x5xx[6] 用來控制 ”Background Fade Enable” (須搭配 R_Wx_FADE)、0x5xx[5]用來控制 “Foreground Blink Enable” (須搭配 R_Wx_CYCLE)、0x5xx[3:0]用來選擇 16 個 Palette 中的某一個和 { 0x5xx[4], 0x4xx[6:0] } 用來控制要選取那一個 Font (0x00~0x7F：定義爲 “Fixed Font” (128 個) , 0x80~0xAF：定義爲 “User Font” (48 個)，和 0xB0~0xBF：定義爲 “Color Font” (16 個))。

另外在Palette RAM部份是以 4 個連續位址當一個屬性，位址 “0” 的 “bit5” 用來控制 “Fringe Enable” 、位址 “0” 的 “bit4” 用來控制 “Foreground Transparent Enable” (等於 1 時，完全透過去)、位址 ”0” 的 ”bit3” 用來控制 ”Background Transparent Enable” (等於 1 時，完全透過去)、位址 ”0” 的 ”bit2~0” 及位址 ”1” 的 ”bit5~0” 用來控制 ”Foreground Color”；位址 ”2” 的 ”bit4” 用來控制 ”Foreground Fade Enable” (須搭配R_Wx_FADE)；位址 ”2” 的 ”bit3” 用來控制 ”Background Blink Enable” (須搭配 R_Wx_CYCLE) 和位址 ”2” 的 ”bit2~0” 及位址 ”3” 的 ”bit5~0” 用來控制”Background Color”，可參考 Figure 6-40 及 Figure 6-41。

而在 ”User Font” 和 ”Color Font” 部份是採用共用RAM的方式來設計，分別有 48 及 16 個Font。在 ”User Font” 的部份則是以 32 個RAM位址的Data來組合成一個Font (可參考”Figure 6-42”)；在 ”Color Font” 的部份則是以 96 個RAM位址的Data來組合成一個Font (可參考 Figure 6-43)。

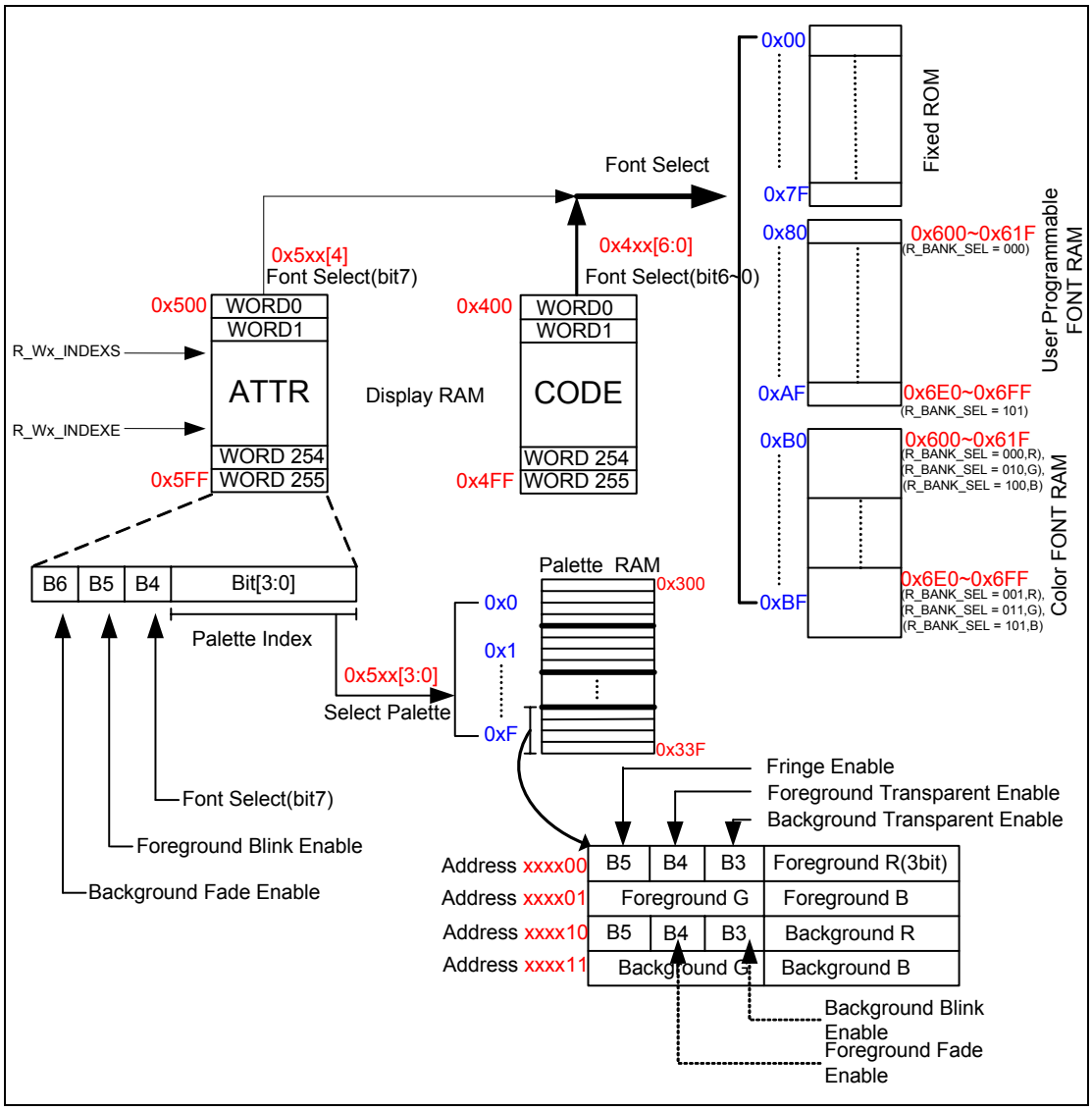


Figure 6-40 OSD Memory Mapping

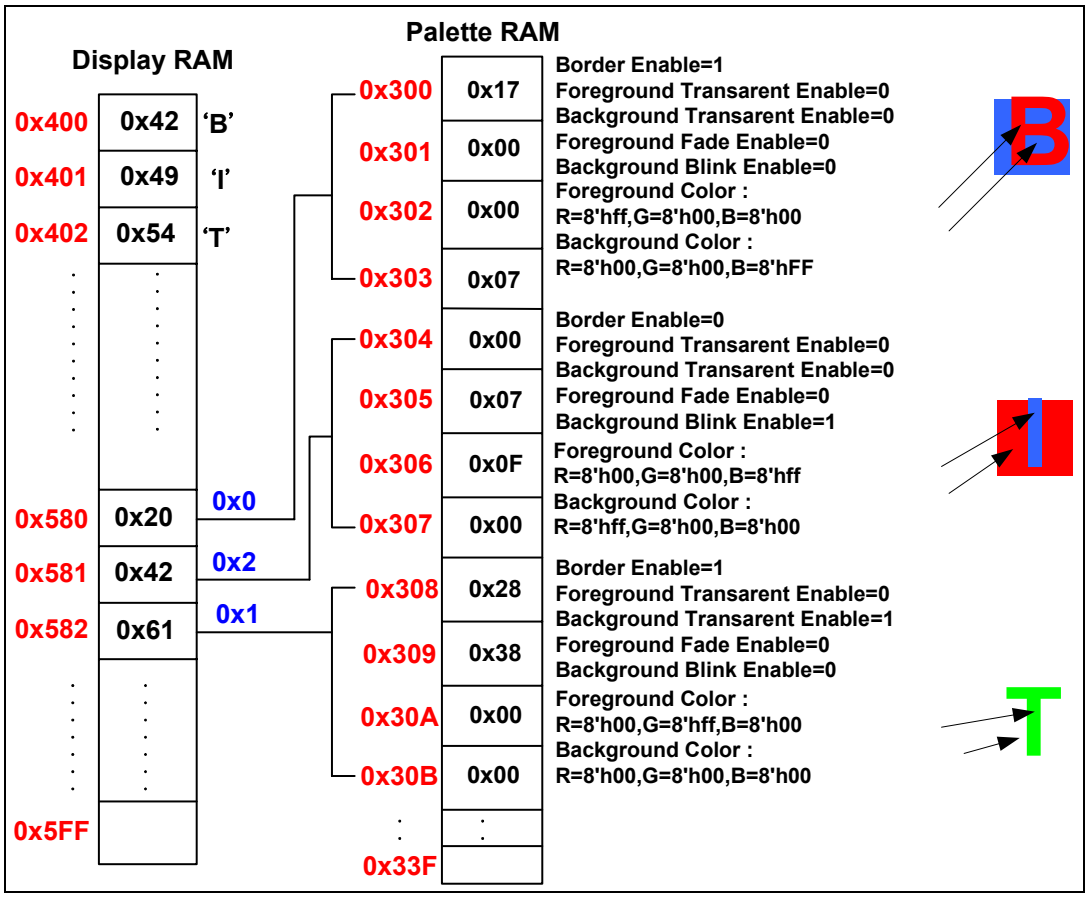


Figure 6-41 Palette RAM Example

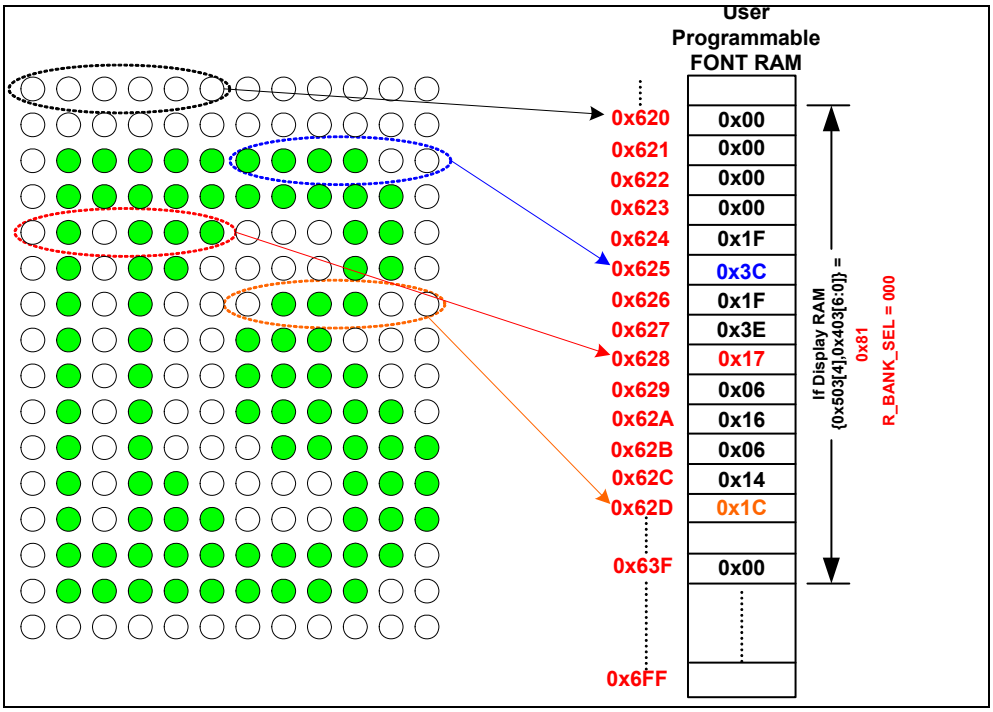


Figure 6-42 OSD User Programmable Font RAM

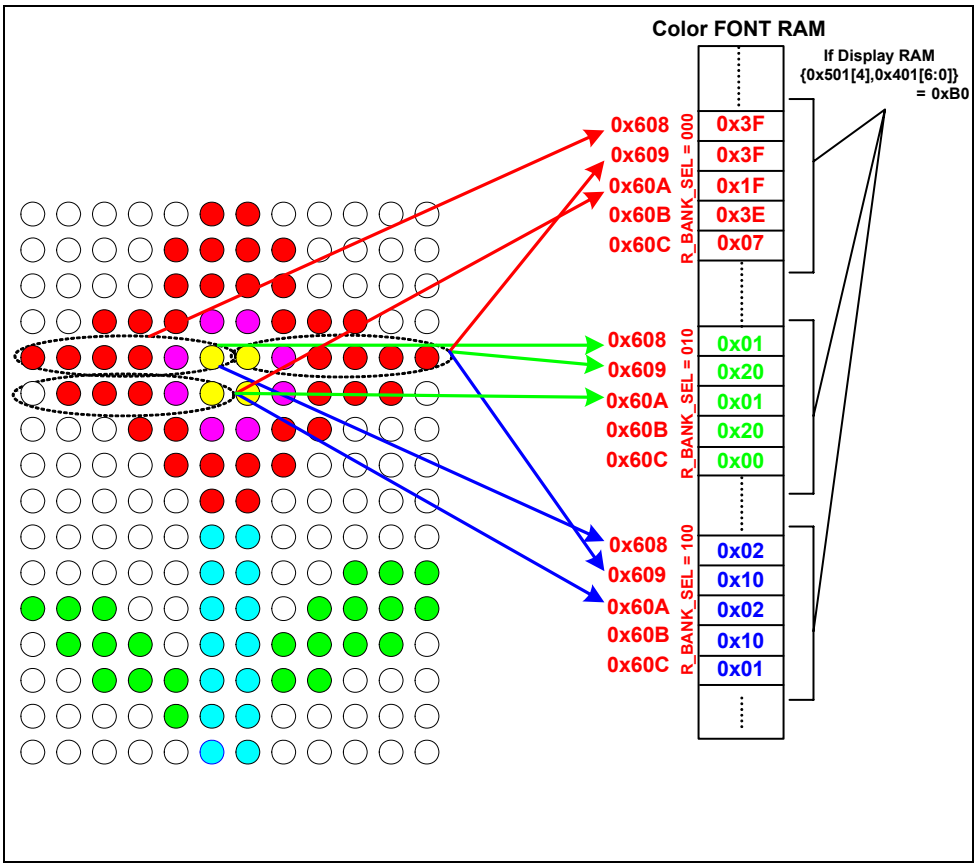


Figure 6-43 OSD Color Font RAM

Table 6-59 OSD Memory Mapping Table			
Memory	Mapping Address		
Display RAM (CODE)	400H~4FFH		
Display RAM (ATTR.)	500H~5FFH		
Palette RAM	300H~33FH (Same as 340H~37FH, 380H~3BFH, 3C0H~3FFH)		
User Programmable Font RAM (Color Font RAM)	600H~6FFH	R_BANK_SEL=000	map to User Font 0~7 or Color R Font 0~7
		R_BANK_SEL=001	map to User Font 8~15 or Color R Font 8~15
		R_BANK_SEL=010	map to User Font 16~23 or Color G Font 0~7
		R_BANK_SEL=011	map to User Font 24~31 or Color G Font 8~15
		R_BANK_SEL=100	map to User Font 32~39 or Color B Font 0~7
		R_BANK_SEL=101	map to User Font 40~47 or Color B Font 8~15

6.32.3 OSD Windows Attributes

BIT1612 可以分別爲 3 個 OSD 視窗設定不同的屬性。

Table 6-60 OSD Windows Attribute Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_W0_INDEX_S	0x107[7:0]	RW	8	OSD0 Display RAM Start Index	0x00
R_W0_INDEX_E	0x108[7:0]	RW	8	OSD0 Display RAM End Index	0xFF
R_W0_FADE	0x10B[3:0]	RW	4	OSD0 Fade In/Out Level	0xF
R_W0_WMIRX	0x109[6]	RW	1	OSD0 Window Mirror for Horizontal	0

R_W0_WMIRY	0x10A[6]	RW	1	OSD0 Window Flip	0
R_W0_FMIRX	0x109[7]	RW	1	OSD0 Characters Mirror for Horizontal	0
R_W0_FMIRY	0x10A[7]	RW	1	OSD0 Characters Mirror for Vertical	0
R_W0_FFRI_SEL	0x10D[7:0]	RW	8	OSD0 Font Fringe Selection Bit7: Left, Up; Bit6: Up; Bit5: Right, Up; Bit4: Left; Bit3: Right; Bit2: Left, Down; Bit1: Down; Bit0: Right, Down;	0xFF
R_W0_FFRI_H	0x10C[3:0]	RW	4	OSD0 Font Fringe Horizontal Width (R_W0_FFRI_H<=R_W0_MULX) 4'b0000: 1 Pixel; ~ 4'b1111: 16 Pixels;	0x0
R_W0_FFRI_V	0x10C[6:4]	RW	3	OSD0 Font Fringe Vertical Width (R_W0_FFRI_V<=R_W0_MULY) 3'b000: 1 Pixel; ~ 3'b111: 8 Pixels;	000
R_W0_FFRI_COR	0x10E[2:0]	RW	3	OSD0 Font Fringe Color Bit2: Color R; Bit1: Color G; Bit0: Color B	111
R_W0_MULX	0x109[4:0]	RW	5	OSD0 Horizontal Character Size 5'b00000: x1; ~ 5'b01111: x16; 5'b10000: x0.5 (Odd); 5'b10001: x0.5 (Even); 5'b1001X: x0.5 (Field Change)	0x00
R_W0_MULY	0x10A[3:0]	RW	4	OSD0 Vertical Character Size 4'b0000: x1; ~ 4'b0111:x8 4'b1000: x0.5 (Odd); 4'b1001: x0.5 (Even), 4'b101x: x0.5 (Field Change)	0x0
R_W0_VANISH_LN	0x10E[7:4]	RW	4	OSD0 Vanish Line Number	0x0
R_W0_VANISH_DIR	0x10E[3]	RW	1	OSD0 Vanish Line Direction	0
R_W0_WFRI_EN	0x10F[7]	RW	1	OSD0 Window Fringe Enable	0
R_W0_WFRI_H	0x10F[3:0]	RW	4	OSD0 Window Fringe Horizontal Width (Pixel)	0x0
R_W0_WFRI_V	0x10F[6:4]	RW	3	OSD0 Window Fringe Vertical Width (Line)	000
R_W0_WFRI_R	0x110[1:0]	RW	2	OSD0 Window Fringe Color Color R	00
R_W0_WFRI_G	0x110[3:2]	RW	2	OSD0 Window Fringe Color Color G	00
R_W0_WFRI_B	0x110[5:4]	RW	2	OSD0 Window Fringe Color Color B	00
R_W0_WFRI_FADE	0x110[7]	RW	1	OSD0 Window Fringe Fade In/Out Enable	0
R_W0_WFRI_BLEN	0x110[6]	RW	1	OSD0 Window Fringe Blink Enable	0
R_W0_WDLY	0x10B[6:4]	RW	3	OSD0 Window Delay (Pixel)	000
R_W0_EN	0x111[7]	RW	1	OSD0 Window Enable	0
R_W0_CYCLE	0x111[6:4]	RW	3	OSD0 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	111
R_W0_SPCY	0x111[2:0]	RW	3	OSD0 Vertical Character Space	000
R_W1_INDEX_S	0x117[7:0]	RW	8	OSD1 Display RAM Start Index	0x0F
R_W1_INDEX_E	0x118[7:0]	RW	8	OSD1 Display RAM End Index	0xFF
R_W1_FADE	0x11B[3:0]	RW	4	OSD1 Fade In/Out Level	0xF
R_W1_WMIRX	0x119[6]	RW	1	OSD1 Window Mirror for Horizontal	0
R_W1_WMIRY	0x11A[6]	RW	1	OSD1 Window Flip	0
R_W1_FMIRX	0x119[7]	RW	1	OSD1 Characters Mirror for Horizontal	0
R_W1_FMIRY	0x11A[7]	RW	1	OSD1 Characters Mirror for Vertical	0
R_W1_FFRI_SEL	0x11D[7:0]	RW	8	OSD1 Font Fringe Selection Bit7: Left, Up; Bit6: Up; Bit5: Right, Up; Bit4: Left; Bit3: Right; Bit2: Left, Down; Bit1: Down; Bit0: Right, Down;	0xFF
R_W1_FFRI_H	0x11C[3:0]	RW	4	OSD1 Font Fringe Horizontal Width (R_W1_FFRI_H<=R_W1_MULX)	0x0

				4'b0000: 1 Pixel; ~ 4'b1111: 16 Pixels;	
R_W1_FFRI_V	0x11C[6:4]	RW	3	OSD1 Font Fringe Vertical Width (R_W1_FFRI_V<=R_W1_MULY) 3'b000: 1 Pixel; ~ 3'b111: 8 Pixels;	000
R_W1_FFRI_COR	0x11E[2:0]	RW	3	OSD1 Font Fringe Color Bit2: Color R; Bit1: Color G; Bit0: Color B	111
R_W1_MULX	0x119[4:0]	RW	5	OSD1 Horizontal Character Size 5'b00000: x1; ~ 5'b01111: x16; 5'b10000: x0.5 (Odd); 5'b10001: x0.5 (Even); 5'b1001X: x0.5 (Field Change)	0x00
R_W1_MULY	0x11A[3:0]	RW	4	OSD1 Vertical Character Size 4'b0000: x1; ~ 4'b0111:x8 4'b1000: x0.5 (Odd); 4'b1001: x0.5 (Even), 4'b101x: x0.5 (Field Change)	0x0
R_W1_VANISH_LN	0x11E[7:4]	RW	4	OSD1 Vanish Line Number	0x0
R_W1_VANISH_DIR	0x11E[3]	RW	1	OSD1 Vanish Line Direction	0
R_W1_WFRI_EN	0x11F[7]	RW	1	OSD1 Window Fringe Enable	0
R_W1_WFRI_H	0x11F[3:0]	RW	4	OSD1 Window Fringe Horizontal Width (Pixel)	0x0
R_W1_WFRI_V	0x11F[6:4]	RW	3	OSD1 Window Fringe Vertical Width (Line)	000
R_W1_WFRI_R	0x120[1:0]	RW	2	OSD1 Window Fringe Color Color R	00
R_W1_WFRI_G	0x120[3:2]	RW	2	OSD1 Window Fringe Color Color G	00
R_W1_WFRI_B	0x120[5:4]	RW	2	OSD1 Window Fringe Color Color B	00
R_W1_WFRI_FADE	0x120[7]	RW	1	OSD1 Window Fringe Fade In/Out Enable	0
R_W1_WFRI_BLEN	0x120[6]	RW	1	OSD1 Window Fringe Blink Enable	0
R_W1_WDLY	0x11B[6:4]	RW	3	OSD1 Window Delay (Pixel)	000
R_W1_EN	0x121[7]	RW	1	OSD1 Window Enable	0
R_W1_CYCLE	0x121[6:4]	RW	3	OSD1 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	111
R_W1_SPCY	0x121[2:0]	RW	3	OSD1 Vertical Character Space	000
R_W2_INDEX_S	0x127[7:0]	RW	8	OSD2 Display RAM Start Index	0x54
R_W2_INDEX_E	0x128[7:0]	RW	8	OSD2 Display RAM End Index	0xFF
R_W2_FADE	0x12B[3:0]	RW	4	OSD2 Fade In/Out Level	0xF
R_W2_WMIRX	0x129[6]	RW	1	OSD2 Window Mirror for Horizontal	0
R_W2_WMIRY	0x12A[6]	RW	1	OSD2 Window Flip	0
R_W2_FMIRX	0x129[7]	RW	1	OSD2 Characters Mirror for Horizontal	0
R_W2_FMIRY	0x12A[7]	RW	1	OSD2 Characters Mirror for Vertical	0
R_W2_FFRI_SEL	0x12D[7:0]	RW	8	OSD2 Font Fringe Selection Bit7: Left, Up; Bit6: Up; Bit5: Right, Up; Bit4: Left; Bit3: Right; Bit2: Left, Down; Bit1: Down; Bit0: Right, Down;	0xFF
R_W2_FFRI_H	0x12C[3:0]	RW	4	OSD2 Font Fringe Horizontal Width (R_W2_FFRI_H<=R_W2_MULX) 4'b0000: 1 Pixel; ~ 4'b1111: 16 Pixels;	0x0
R_W2_FFRI_V	0x12C[6:4]	RW	3	OSD0 Font Fringe Vertical Width (R_W2_FFRI_V<=R_W2_MULY) 3'b000: 1 Pixel; ~ 3'b111: 8 Pixels;	000
R_W2_FFRI_COR	0x12E[2:0]	RW	3	OSD2 Font Fringe Color Bit2: Color R; Bit1: Color G; Bit0: Color B	000
R_W2_MULX	0x129[4:0]	RW	5	OSD2 Horizontal Character Size 5'b00000: x1; ~ 5'b01111: x16; 5'b10000: x0.5 (Odd); 5'b10001: x0.5 (Even);	0x00

				5'b1001X: x0.5 (Field Change)	
R_W2_MULY	0x12A[3:0]	RW	4	OSD2 Vertical Character Size 4'b0000: x1; ~ 4'b0111:x8 4'b1000: x0.5 (Odd); 4'b1001: x0.5 (Even), 4'b101x: x0.5 (Field Change)	0x0
R_W2_VANISH_LN	0x12E[7:4]	RW	4	OSD2 Vanish Line Number	0x0
R_W2_VANISH_DIR	0x12E[3]	RW	1	OSD2 Vanish Line Direction	0
R_W2_WFRI_EN	0x12F[7]	RW	1	OSD2 Window Fringe Enable	0
R_W2_WFRI_H	0x12F[3:0]	RW	4	OSD2 Window Fringe Horizontal Width (Pixel)	0x0
R_W2_WFRI_V	0x12F[6:4]	RW	3	OSD2 Window Fringe Vertical Width (Line)	000
R_W2_WFRI_R	0x130[1:0]	RW	2	OSD2 Window Fringe Color Color R	00
R_W2_WFRI_G	0x130[3:2]	RW	2	OSD2 Window Fringe Color Color G	00
R_W2_WFRI_B	0x130[5:4]	RW	2	OSD2 Window Fringe Color Color B	00
R_W2_WFRI_FADE	0x130[7]	RW	1	OSD2 Window Fringe Fade In/Out Enable	0
R_W2_WFRI_BLEN	0x130[6]	RW	1	OSD2 Window Fringe Blink Enable	0
R_W2_WDLY	0x12B[6:4]	RW	3	OSD2 Window Delay (Pixel)	000
R_W2_EN	0x131[7]	RW	1	OSD2 Window Enable	0
R_W2_CYCLE	0x131[6:4]	RW	3	OSD2 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	111
R_W2_SPCY	0x131[2:0]	RW	3	OSD2 Vertical Character Space	000

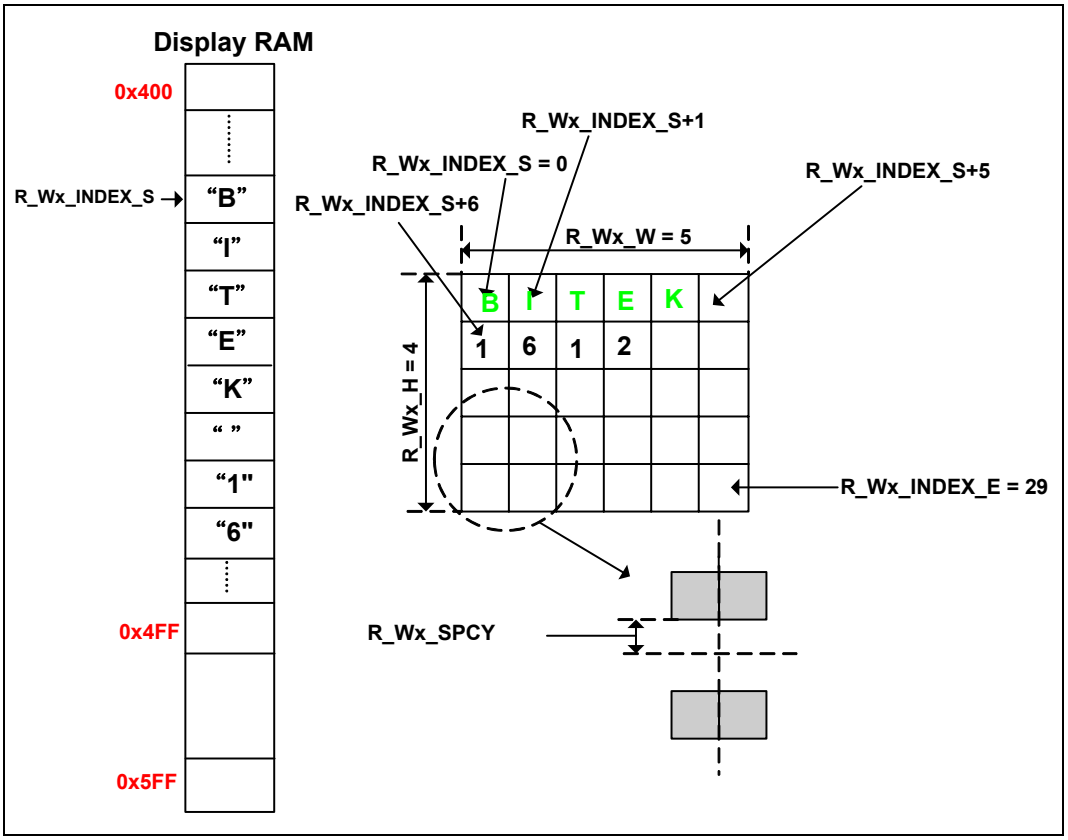


Figure 6-44 OSD Windows Attribute

6.32.4 OSD Windows Overlap Selection

以下 Register 用來選擇 OSD 視窗重疊的順序。

Table 6-61 OSD Windows Overlap Selection

Mnemonic	Address	R/W	Bits	Description		Default
R_OSD_LAYER	0x101[7:5]	RW	3	OSD Windows Overlap Selection		000
				000	OSD0->OSD1->OSD2	
				001	OSD0->OSD2->OSD1	
				010	OSD1->OSD0->OSD2	
				011	OSD1->OSD2->OSD0	
				100	OSD2->OSD0->OSD1	
				101, 11x	OSD2->OSD1->OSD0	

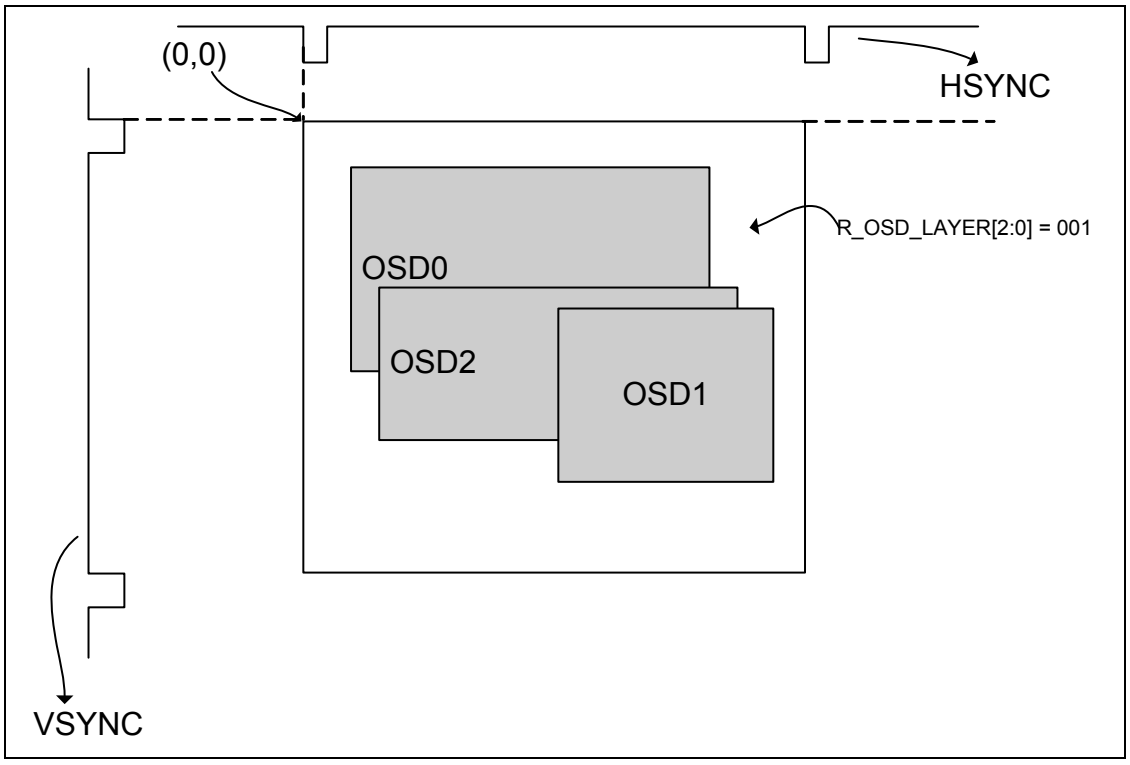


Figure 6-45 OSD Windows Overlap

6.32.5 External OSD Interface

BIT1612 可連接外部 OSD 作爲更複雜的 OSD 應用，共計可以顯示 8 種顏色。然而，因爲 GIN Port 會被外部 OSD 佔用，在這樣情況下，BIT1612 無法支援 Graphic 輸入方式。

Table 6-62 External OSD Register

Mnemonic	Address	R/W	Bits	Description	Default
R_EXTOSD_EN	0x100[0]	RW	1	External OSD Enable 0: Disable 1: Enable	0
R_POL_EXTBNK	0x100[1]	RW	1	External OSD Blank Polarity 0: Normal 1: Invert	0
R_POL_OSDHS	0x100[2]	RW	1	External OSD HSYNC Polarity 0: Normal 1: Invert	0
R_POL_OSDVS	0x100[3]	RW	1	External OSD VSYNC Polarity 0: Normal 1: Invert	0
R_POL_OSDCLK	0x100[4]	RW	1	External OSD CLOCK Polarity 0: Normal 1: Invert	0

6.32.6 OSD User Programmable RAM Selection

以下 Register 用來選擇讀/寫 OSD User Programmable RAM 時所用的 Memory Bank。

Table 6-63 User Programmable RAM Selection

Mnemonic	Address	R/W	Bits	Description		Default
R_BANK_SEL	0x101[4:2]	RW	3	**User Programmable RAM Banks Selection**		000
				000	Bank 0, Mapping to User Font 0~7 (Mapping to R Color Font 0~7)	
				001	Bank 1, Mapping to User Font 8~15 (Mapping to R Color Font 8~15)	
				010	Bank 2, Mapping to User Font 16~23 (Mapping to G Color Font 0~7)	
				011	Bank 3, Mapping to User Font 24~31 (Mapping to G Color Font 8~15)	
				100	Bank 4, Mapping to User Font 32~39 (Mapping to B Color Font 0~7)	
				101	Bank 5, Mapping to User Font 40~47 (Mapping to B Color Font 8~15)	

6.32.7 OSD Clock Control

BIT1612 OSD部份提供 Clock 開或關的功能，其相關Registers設定請參考 Table 6-64。

Table 6-64 OSD Clock Setting Register

Mnemonic	Address	R/W	Bits	Description	Default
R_OSDCLK_EN	0x00B[0]	RW	1	OSD Clock Enable 0: Disable 1: Enable	1
R_OSDCLK_POL	0x00B[1]	RW	1	OSD Clock Polarity 0: Normal 1: Invert	1

6.32.8 OSD Built-In Fixed Font

BIT1612 已內建 128 種 OSD 字型，其定址如下：

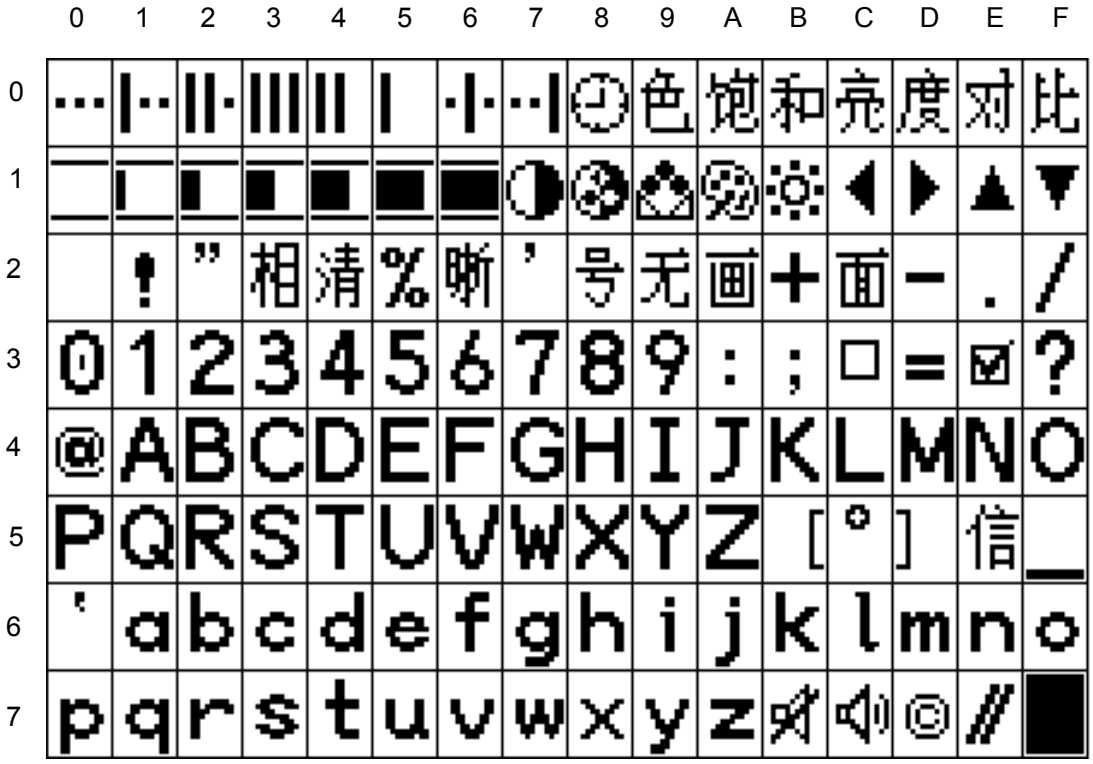


Figure 6-46 Fixed Font

6.33 Timer

BIT1612 提供了兩個獨立 16 位元的計數器，相關說明及設定請參考下列圖表。

Table 6-65 Timer Register

Mnemonic	Address	R/W	Bits	Description	Default
R_TIMER0_VAL	0x143[7:0],0x142[7:0]	RW	16	Timer 0 Count Value	0x0000
R_TIMER0_EN	0x144[0]	RW	1	Timer 0 Enable 0: Disable 1: Enable	0
R_TIMER0_MODE	0x144[1]	RW	1	Timer 0 Count Mode 0: Circulation 1: One-Shot	0
R_TIMER0_BASE_MODE	0x144[3:2]	RW	2	Timer 0 Count Base 00: Output VSYNC 01: Output HSYNC 10: Input VSYNC 11: Input HSYNC	00
R_TIMER1_VAL	0x146[7:0],0x145[7:0]	RW	16	Timer 1 Count Value	0x0000
R_TIMER1_EN	0x147[0]	RW	1	Timer 1 Enable 0: Disable 1: Enable	0
R_TIMER1_MODE	0x147[1]	RW	1	Timer 1 Count Mode 0: Circulation 1: One-Shot	0
R_TIMER1_BASE_MODE	0x147[3:2]	RW	2	Timer 1 Count Base 00: Output VSYNC 01: Output HSYNC 10: Input VSYNC 11: Input HSYNC	00

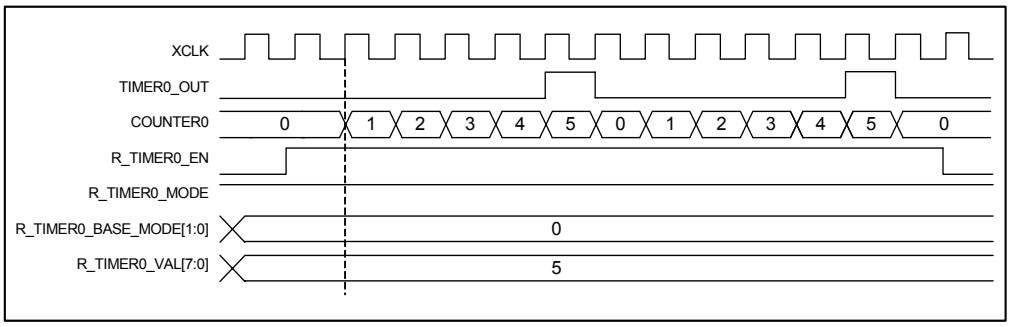


Figure 6-47 Timer Mode 0 (Circulation)

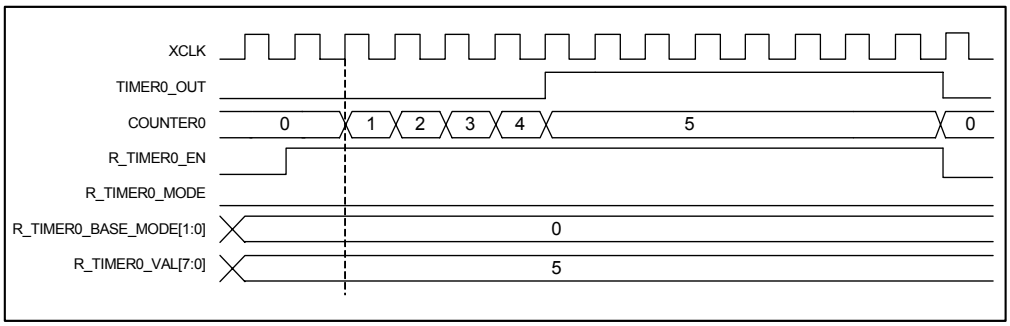


Figure 6-48 Timer Mode 1 (One-Shot)

6.34 IR Decoder Function

BIT1612 提供 NEC IR Decoder function，由 BIT1612 偵測 NEC IR Format，並經由 Interrupt 提供給 MCU 參考，其相關 Registers 設定請參考下表：

Table 6-66 IR Pulse Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IR_CC	0x149[7:0]	RW	8	User Defined Customer Code	0x00
	0x148[7:0]	RW	8	User Defined Customer /Code	0x00
R_POL_IR	0x14A[0]	RW	1	NEC IR Polarity 0: Normal 1: Invert	0
R_IR_DISREPT	0x14A[1]	RW	1	Repeat Code Detection Enable 0: Enable Repeat Code 1: Disable Repeat Code	0
R_IR_BASE	0x14A[4:2]	RW	3	NEC IR Clock Base 000: XCLK 001: XCLK/2 010: XCLK/3 011: XCLK/4 100: XCLK/5 101: XCLK/6 110: XCLK/7 111: XCLK/8	000
R_IR_CHECK	0x14A[7:5]	RW	3	NEC Interrupt Conditions [5]: Check IR Code = ~IR /Code [6]: Check IR Data = ~IR /Data [7]: Check IR Code = User Defined Customer Code and IR /Code = User Defined Customer /Code	000
R_IR_EN	0x14B[0]	RW	1	NEC IR Decoder Enable 0: Disable 1: Enable	0
R_IR_DB	0x14B[3:2]	RW	2	IR De-Bounce Setup	00
R_IR_TYPE	0x14B[4]	R	1	IR Code Type 0: First Code 1: Repeat Code	-
R_IR_CODE	0x14C[7:0]	R	8	NEC IR /Data Byte	-
	0x14D[7:0]	R	8	NEC IR /Code Byte	-
	0x14E[7:0]	R	8	NEC IR Data Byte	-
	0x14F[7:0]	R	8	NEC IR Code Byte	-

6.35 GPI and KEY Function

BIT1612 內建 8 組GPI (General Purpose Input)，並可針對各個GPI Pin分別規劃爲Level Status，Key Down 或 Key Up三種觸發狀態，並可經由Interrupt (0x002[7])、R_KEY_STATUS (0x155) 及R_KEY_ACK (0x156) 讀回其狀態。相關Registers設定請參考 Table 6-67 及 Figure 6-49。

Table 6-67 GPI and KEY Register

Mnemonic	Address	R/W	Bits	Description	Default
R_KEY_STATUS	0x155[7:0]	R	8	Real Time GPI Status	0x00
R_KEY_ACK	0x156[7:0]	R	8	KEY Trigger Status	0x00
R_KEY_LONG_FLAG	0x157[7]	R	1	Long Key Trigger Flag	0
R_KEY_LONG_ACK	0x157[3:0]	R	4	Long Key Trigger Status	0x0
R_KEY_TYPE	0x150[7:0]	RW	8	0: Positive Edge; 1: Negative Edge	0x00
R_KEY_DEDGE	0x151[7:0]	RW	8	0: Single Edge; 1: Double Edge	0x00
R_KEY_SRC	0x152[7]	RW	1	R_KEY_SRC_64=0 0: TOUT_I 1: BIN R_KEY_SRC_64=1 0: RIN 1: HSYNC (Key[1]), VSYNC (Key[0])	1
R_KEY_DB	0x152[6:4]	RW	3	GPI De-Bounce Setup	100
R_KEY_LONG_EN	0x152[3:0]	RW	4	GPI[3:0] Long Key Monitor Enable	0x0
R_KEY_LONG_STR	0x153[7:0]	RW	8	Long Key Trigger Threshold	0xFF
R_KEY_LONG_REP	0x154[7:0]	RW	8	Long Key Trigger Interval	0x50
R_KEY_CLEAR	0x157[4]	RW	1	0: Normal; 1: Clear	1
R_KEY_TB	0x157[6:5]	RW	2	Long Key Basic Clock Cycle	01
R_KEY_SRC_64	0x14B[1]	RW	1	KEY Source Selection 0: Type 1 1: Type 2	0

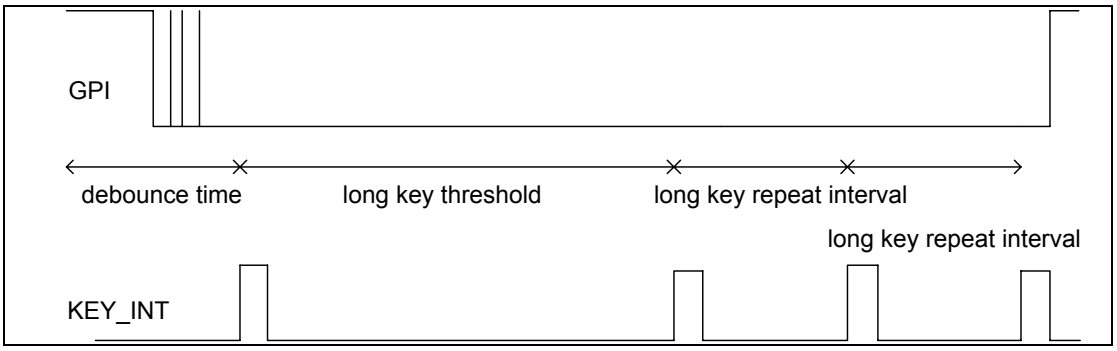


Figure 6-49 Long Key Process

6.36 PLL and OSC Pads

BIT1612 內建一組PLL，並依據Oscillator所提供的頻率產生可程式化的Clock輸出。其相關公式及Registers請參考 Table 6-68 及 Figure 6-50。

Table 6-68 PLL Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PLL_PD	0x158[0]	RW	1	PLL Power Down Enable 0: Normal 1: Disable	0
R_PLL_RESETN	0x158[1]	RW	1	PLL Reset 0: Reset 1: Normal	1

R_PLL_HALFCK	0x158[2]	RW	1	PLL Half Clock Output 0: Normal 1: Half Clock	1
R_PLL_SEL	0x158[3]	RW	1	PLL Clock Control 0: Normal 1: DIV ((R_PLL_DP+1)*2)	0
Auto Switch Mode 0 Input Widows Setup					
R_PLL_DM_M0	0x159[4:0]	RW	5	PLL DM Value	0x08
R_PLL_DN_M0	0x15A[6:0]	RW	7	PLL DN Value	0x09
R_PLL_DP_M0	0x15B[5:0]	RW	6	PLL DP Value	0x00
Auto Switch Mode 1 Input Widows Setup					
R_PLL_DM_M1	0x15C[4:0]	RW	5	PLL DM Value	0x08
R_PLL_DN_M1	0x15D[6:0]	RW	7	PLL DN Value	0x09
R_PLL_DP_M1	0x15E[5:0]	RW	6	PLL DP Value	0x00

$$PLL\_OUT = \frac{(R\_PLL\_DN+1)}{(R\_PLL\_DM+1)} * \frac{1}{2^{R\_PLL\_HALFCK}} * \frac{1}{((R\_PLL\_DP+1)*2)^{R\_PLL\_SEL}} * OSC\_Freq\_Sel$$

Figure 6-50 PLL Frequency Formula

6.37 Auto Detection

BIT1612 提供七種輸入訊號偵測機制，分別爲 PCLK Base SYNC Detection、XCLK Base HSYNC Detection、Mode Change Detection、Mode Type Detection、Even/Odd Type Detection、Data Enable Signal Detection 和 No Signal Detection。

1. PCLK Base SYNC Detection:
   以 PCLK 偵測 External HSYNC、External VSYNC Low Pulse Width 及 Total SYNC Width，其主要作爲 SYNC 極性判別及模式的偵測，此偵測機制 Power On 時就會自動啓動且無法由 MCU 去終止或啓動，其操作步驟如下：

   (讀取偵測 SYNC 資料：)

   Register (0x160[7:0]): HSYNC Low Pulse (in PCLK)。

   Register (0x164[7:4], 0x161[7:0]): HSYNC Total Width (in PCLK)。

   Register (0x162[7:0]): VSYNC Low Pulse (in HSYNC)。

   Register (0x164[2:0], 0x163[7:0]): VSYNC Total Width (in HSYNC)。

2. XCLK Base HSYNC Detection:
   以 XCLK 偵測 External HSYNC，其主要作爲模式的判別。此偵測機制會以 XCLK 爲基準計算 Input HSYNC Low Level Width 和 HSYNC High Level Width，其操作步驟如下：

   (讀取偵測 HSYNC 資料：)

   Register (0x167[7:4], 0x165[7:0]): HSYNC High Level Width (in XCLK)。

   Register (0x167[3:0], 0x166[7:0]): HSYNC Low Level Width (in XCLK)。

3. Mode Change Detection:
   偵測 VSYNC 變化量，如果 VSYNC 變化量大於 8 條 HSYNCs，將會經由 Interrupt 機制回應給 MCU 得知，其操作步驟如下：

   Set Interrupt Enable (Register: 0x004[2])。

   如果 VSYNC 變化量大於 8，將會由 INT Pin 發出 Interrupt，亦可藉由輪詢的方式讀取 Interrupt Flag (Register: 0x002[2]) 而得知。

4. Mode Type Detection:

自動辨別 NTSC/PAL Mode 並可由 Register (0x16A[1]) 直接讀出其狀態。

5. EVEN/ODD Type Detection:

   自動判別 VSYNC 是否有 EVEN/ODD 相關變化，並可由 Register (0x16A[2]) 直接讀出其狀態。

6. Data Enable Signal Detection:

   自動偵測 Data Enable Signal Information 以供系統作爲設定 Input Windows 的參考。

7. No Signal Detection:

   自動判別 HSYNC 是否有 Toggle，如果在 2047 XCLKs 內沒有變化將由 Interrupt (0x002[1:0]) 回應或可由 Register (0x16A[3]) 直接讀出其狀態。

Table 6-69 Auto Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IS_XP	0x160[7:0]	R	8	HSYNC Low Pulse (Base on PCLK)	-
R_IS_XT	0x164[7:4], 0x161[7:0]	R	12	HSYNC Total Width (Base on PCLK)	-
R_IS_YP	0x162[7:0]	R	8	VSYNC Low Pulse (Base on HSYNC)	-
R_IS_YT	0x164[2:0], 0x163[7:0]	R	11	VSYNC Total width (Base on HSYNC)	-
R_DET_XP	0x167[7:4],0x165[7:0]	R	12	HSYNC High Level Width (Base on XCLK)	-
R_DET_XN	0x167[3:0],0x166[7:0]	R	12	HSYNC Low Level Width (Base on XCLK)	-
R_HOUNT	0x169[6:0],0x168[7:0]	R	15	Line Buffer Overflow/Underflow Count	-
R_MODECHG	0x16A[0]	R	1	Mode Change Status ➔0: No Mode Change ➔1: VSYNC Variation Larger than 8 HSYNCs	-
R_MODE_TYPE	0x16A[1]	R	1	Mode Status ➔0: 50Hz ➔1: 60Hz	-
R_EVENSAME	0x16A[2]	R	1	EVEN Type Status ➔0: Had EVEN/ODD Information ➔1: No EVEN/ODD Information	-
R_SIGIN	0x16A[3]	R	1	Sync Status ➔0: Signal Ready ➔1: No Signal	-
R_AUTOON	0x16A[4]	R	1	Auto Blank Status ➔0: Normal Mode ➔1: Free-Run Mode	-
R_SWITCH	0x16A[5]	R	1	Auto Switch Status ➔0: Mode 0 ➔1: Mode 1	-
R_EVEN	0x16A[6]	R	1	EVEN/ODD Information ➔0: EVEN Field ➔1: ODD Field	-
R_IDE_INFO	0x16C[3:0],0x16B[7:0]	R	12	Input Data Enable Information	-
R_IDE_DET	0x4E[1:0]	RW	2	Input Data Enable Mode Selection 00: HSYNC Low Pulse Information 01: HSYNC High Pulse Information 10: VSYNC Low Pulse Information 11: VSYNC High Pulse Information	00
R_IDE_SEL	0x4E[3:2]	RW	2	Input Data Enable Source Selection 00: From HSYNC1 Pin	00

				01: From VSYNC1 Pin	
				10: From HSYNC2 Pin	
				11: From VSYNC2 Pin	

7 User Interface

BIT1612 提供二種 Interface Mode (Slave Mode 和 Script Master Mode)，使其能應用在不同的環境中。

7.1 Options Pins

BIT1612 使用 6 根外部 Pins 來做 Mode 的選擇。主要可以分爲 Master 與 Slave Mode。Slave Mode 下，外部的 MCU 可以經由 Pin OP1、OP0 控制 BIT1612，並視需要選擇 Two-Wire Serial Interface (TWSI) Protocol 或是 Bitek Bus Protocol。Master Mode 則是運用 BIT1612 內建 CPU 搭配外部程式記憶體完成系統設計。在 Master Mode 下 Script MCU 則只需要搭配 24 系列的 Serial EEPROM，並利用 Bitek 自行定義的指令集，即可完成 BIT1612 的相關控制。

Script MCU支援三種工作模式，分別是Single 24C16、Single 24C32 與Dual 24C16。Single 24C16 Mode可以支援單顆 24C16 以下的EEPROM；24C32 Mode可以支援單顆 24C32 系列的EEPROM (24C32/24C64)；Dual 24C16 Mode可以運用 { OP2, OP3 } 做爲第二組TWSI介面，擴充程式記憶體，最多可支援兩顆 24C16，定義及使用方法請參考下表，其示意圖可參考 Figure 7-1、Figure 7-2、Figure 7-3 及 Figure 7-4。

Table 7-1 Options Pins Setup

OP5	OP4	OP3	OP2	OP1	OP0	Mode
0	0	SCL2	SDA2	SCL1	SDA1	EEPROM 24C16 Script Mode
0	1	SCL2	SDA2	SCL1	SDA1	EEPROM 24C32 Script Mode
1	X	SA[1]	SA[0]	SCL1	SDA1	Slave Mode
1	0	0	0	SCL1	SDA1	TWSI Mode Slave Address (0x00~0x0F)
1	0	0	1	SCL1	SDA1	TWSI Mode Slave Address (0x20~0x2F)
1	0	1	0	SCL1	SDA1	TWSI Mode Slave Address (0x40~0x4F)
1	0	1	1	SCL1	SDA1	TWSI Mode Slave Address (0x60~0x6F)
1	1	0	0	SCL1	SDA1	BiTEKBUS Mode Slave Address 0x81
1	1	0	1	SCL1	SDA1	BiTEKBUS Mode Slave Address 0x83
1	1	1	0	SCL1	SDA1	BiTEKBUS Mode Slave Address 0x85
1	1	1	1	SCL1	SDA1	BiTEKBUS Mode Slave Address 0x87

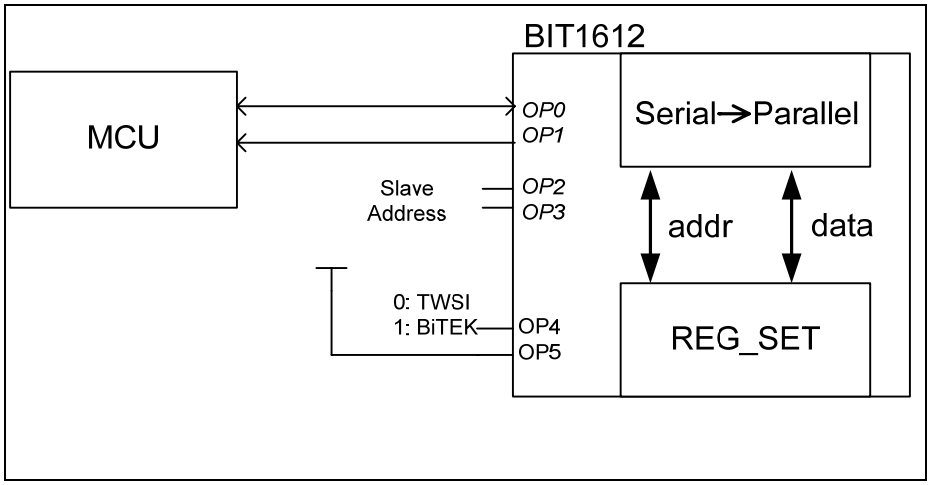


Figure 7-1 Slave Mode

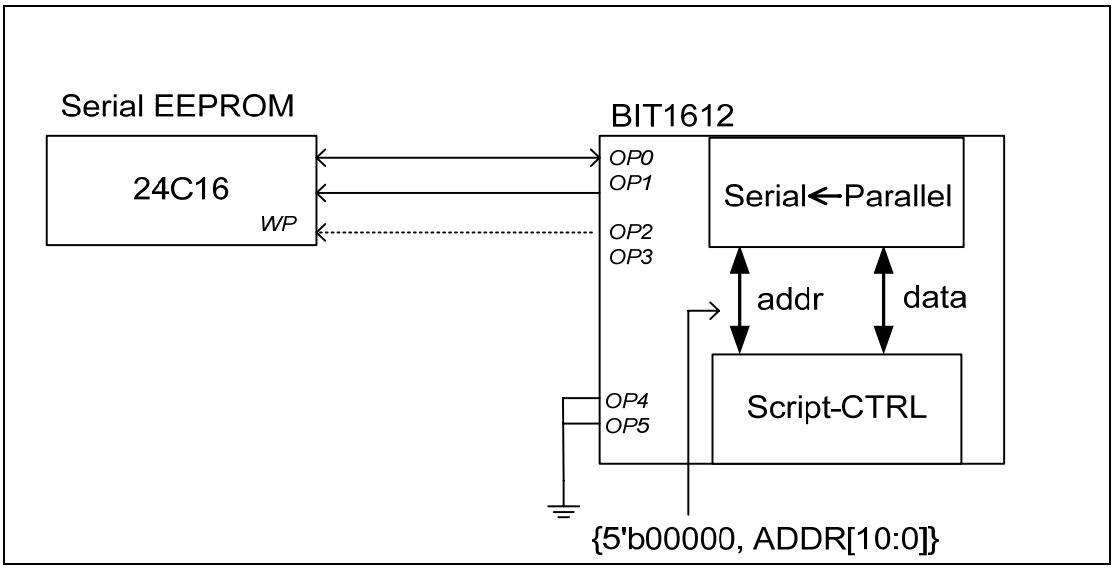


Figure 7-2 Master Mode with Single 24C16

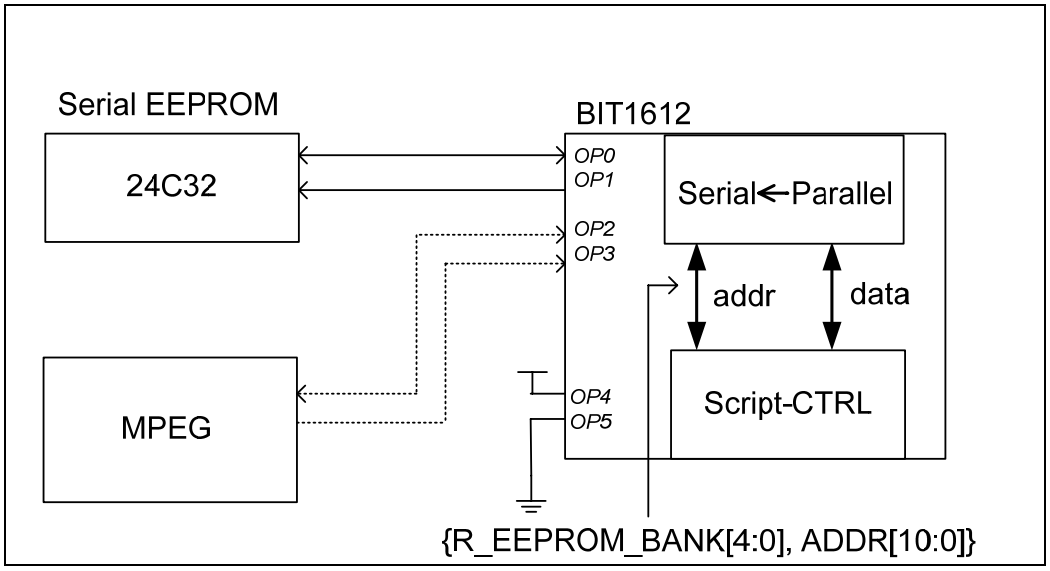


Figure 7-3 Master Mode with Single 24C32

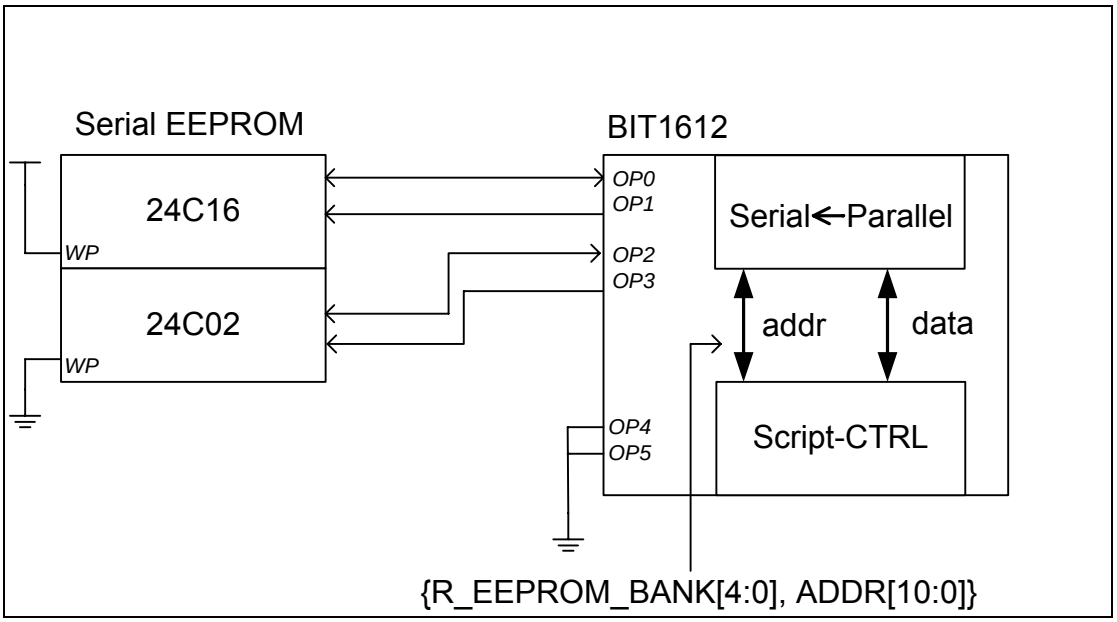


Figure 7-4 Master Mode with Dual EEPROM

7.2 Master Mode – Script MCU

BIT1612 內建 Script MCU，可提供使用者將程式碼儲存在 Serial EEPROM 中，BIT1612 將會依據使用者所撰寫的程式碼內容，解碼後執行其相對的指令，目前僅支援 24 系列 (24C02~24C64) 的 Serial EEPROM。而執行速度則依據於 TWSI 速度而定，透過設定 R_SERIAL_CKEN_SEL (0x138[2:0]) 可調整 TWSI 速度，從 98KHz ~ 384KHz，參考設定如下表。

Table 7-2 TWSI Speed

	R_XCLK_SEL		
	OSC/1	OSC/2	OSC/4
R_SERIAL_CKEN_SEL=0	97KHz	48KHz	24KHz
R_SERIAL_CKEN_SEL=1	189KHz	95KHz	47KHz
R_SERIAL_CKEN_SEL=2	372KHz	186KHz	93KHz
R_SERIAL_CKEN_SEL=3	585KHz	292KHz	146KHz
R_SERIAL_CKEN_SEL=4	614KHz	307KHz	153KHz
R_SERIAL_CKEN_SEL=5	768KHz	384KHz	192KHz
R_SERIAL_CKEN_SEL=6	945KHz	472KHz	236KHz
R_SERIAL_CKEN_SEL=7	x	558KHz	279KHz

7.2.1 Architecture

BIT1612 內建之Script Control內含 4 個Internal Registers (A_REG、B_REG、C_REG、Z_REG) 及 5 組Internal Address Index (PC、EADDR、RADDR、IADDR、R_REG_ADDR)，32 Bytes Internal RAM (0x700~0x71F)，BIT1612 指令集對EEPROM只能定址到 2KB，但可以運用R_EEPROM_BANK_SEL切換 EEPROM BANK方式擴增，最多可以定址到 64KB。相關Registers如 Table 7-3 所示，所有的算數及邏輯運算皆在A_REG及B_REG內進行。

Table 7-3 Register and Address Index

Register and Address Index	Address	R/W	Bits	Memo
A_REG	0x13F[7:0]	R	8	Operand A Register
B_REG	0x140[7:0]	R	8	Operand B Register
C_REG	0x13E[6]	R	1	Carry Flag Register
Z_REG	0x13E[5]	R	1	Zero Flag Register
PC	-	-	11	Program Counter
EADDE	-	-	11	EEPROM Address
RADDR	-	-	11	Internal Register Setting Address
IADDR	-	-	8	TWSI Address Device Address <= R_TWSI_SLAVE REG Address <= Instruction Byte 2
R_REG_ADDR	0x137[2:0],0x136[7:0]	RW	11	ADDR Register (Shared) FILLR JMPR TABLE
R_REG_NUM	0x134[7:0]	RW	8	NUM Register (Shared) FILLR
R_REG_CNT	0x135[7:0]	RW	8	Count Register (Shared) FILLR
R_SERIAL_CKEN_SEL	0x138[2:0]	RW	3	TWSI SCL SPEED 98KHz ~ 384KHz (111: Fastest; 000: Lowest)
R_SECOND_EEPROM	0x138[3]	RW	1	Second EEPROM Enable 0: Single EEPROM 1: Dual EEPROM
R_EEPROM_BANK_SEL	0x137[7:3]	RW	5	EEPROM Bank Selection
R_PG_EN	0x138[4]	RW	1	Power Good Function Enable
R_PG_POL	0x138[5]	RW	1	Power Monitor Input Inverse 0: Low active 1: High active

R_POF	0x13E[4]	R	1	Power Low Flag 0: Normal 1: Power Low Reset
R_MCU_DEBUG	0x138[6]	RW	1	MCU Debug Mode 0: Disable 1: Enable
R_TWSI_SEC	0x138[7]	RW	1	Second EEPROM I/O Pin Enable 0: Disable 1: Enable
R_TWSI_DET_VALUE	0x139[7:0]	RW	8	Second TWSI Bus Detection Value
R_TWSI_DET_IN	0x13A[7:0]	RW	8	Second TWSI Bus Read Value
R_TWSI_DET_MODE	0x13B[1:0]	RW	2	Second TWSI Bus Detection Mode (Trigger Condition) 00: ADDR[7:0] = R_TWSI_DET_VALUE[7:0] 01: Write Trigger 10: Read Trigger 11: Write/Read Trigger
R_TWSI_SEC_SLAVE	0x13B[3:2]	RW	2	Second TWSI Bus Slave Address
R_TWSI_DET_OUT	0x13D[7:0]	R	8	Second TWSI Bus Detection Write Value
R_WDT_CLEAR	0x13B[4]	RW	1	WDT Clear
R_WDT_SEL	0x13B[7:5]	RW	3	WDT Interval Selection 000 : 20ms; 001 : 40ms; 010 : 80ms; 011 : 160ms; 100 : 320ms; 101 : 640ms; 110 : 1.28sec; 111 : 2.56sec;
R_WDT_OV	0x13E[7]	R	1	WDT overflow

R_TWSI_SLAVE	0x136[6:0]	RW	7	TWSI Slave Device Address (Shared)
				For Instruction
				MOV @IADDR, A
				MOV A, @IADDR

R_SPI_CTRL	0x134[7:0]	RW	8	SPI Function Control [7] SPI CS Inverse [6] SPI DATA Inverse [5] SPI CLK Inverse [4] SPI SYNC 0: Immediately 1: Synchronized with TCON [3:2] SPI Mode 00: Mode 0 11: Mode 3 [1:0] SPI Speed 00: XCLK/8 01: XCLK/16 10: XCLK/32 11: XCLK/64
R_SPI_CTRL2	0x133[4:0]	RW	5	SPI Function Control Register 2 [4:0] SPI Bit Number (N) N = 0~24: Bit Number = N N > 24: Bit Number = 24
R_SPI_LOCK	0x13C[1]	RW	1	SPI Mode Lock 0: Unlocked 1: Locked
R_SPI1_EN	0x13C[2]	RW	1	BOUT[5] = SPI CLK BOUT[4] = SPI DATA BOUT[3] = SPI CS

R_SPI2_EN	0x13C[3]	RW	1	SRGBOUT[8] = SPI CLK SRGB_SDO = SPI DATA SRGB_CS = SPI CS
R_WP_EN	0x13C[6]	RW	1	EEPROM Write Protection Enable 0: Disable 1: Enable

7.2.2 Instruction Set

BIT1612 內建Script Control Function 提供下列的指令碼，相對應的Instruction Set與Instruction Format，請參考 Table 7-4 及 Table 7-5。

Table 7-4 Instruction Set

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	Instruction	Command Byte	C	Z
0	0	0	0	0	0	0	0	ADD A_REG ← A_REG +B_REG	1	●	●
0	0	0	0	0	0	0	1	SUB A_REG ←A_REG – B_REG	1	●	●
0	0	0	0	0	0	1	0	INC A_REG ← A_REG + 1	1	●	●
0	0	0	0	0	0	1	1	DEC A_REG ← A_REG – 1	1	●	●
0	0	0	0	0	1	0	0	CLR A_REG ← 0	1		●
0	0	0	0	0	1	0	1	COMP A_REG – B_REG (Not Update A_REG)	1	●	●
0	0	0	0	0	1	1	0	MOV B,A B_REG ← A_REG	1		
0	0	0	0	0	1	1	1	HALT Program Stop Into Standby Mode	1		
0	0	0	0	1	0	0	0	AND A_REG ← A_REG (AND) B_REG	1		●
0	0	0	0	1	0	0	1	OR A_REG ← A_REG (OR) B_REG	1		●
0	0	0	0	1	0	1	0	XOR A_REG ← A_REG (XOR) B_REG	1		●
0	0	0	0	1	0	1	1	NOT A_REG ← ~A_REG	1		●
0	0	0	0	1	1	0	0	SHR A_REG ← A_REG >> 1	1		●
0	0	0	0	1	1	0	1	SHL A_REG ← A_REG << 1	1		●
0	0	0	0	1	1	1	0	SWAP A_REG ⇔ B_REG	1		●
0	0	0	0	1	1	1	1	XCHG A_REG[7:4] ⇔ A_REG[3:0]			●
0	0	0	1	0	R10	R9	R8	MOV A, @R[ADDR] A_REG ← R[ADDR]	2		●
0	0	0	1	1	R10	R9	R8	MOV @R[ADDR], A R[ADDR] ← A_REG	2		
0	0	1	0	0	0	0	0	MOV A, #NUM A_REG ← #NUM	2		●
0	0	1	0	0	0	0	1	MOV B, #NUM B_REG ← #NUM	2		
0	0	1	0	0	0	1	0	DELAY #NUM Delay #NUM XCLK	2		
0	0	1	0	0	1	0	0	NOTC	1	●	

								C_FLAG ← ~C_ FLAG			
0	0	1	0	0	1	0	1	NOTZ Z_ FLAG ← ~Z_ FLAG	1		•
0	0	1	0	0	1	1	0	RET PC ← RET_ADDR	1		
0	0	1	0	1	E10	E9	E8	MOV E[ADDR], #NUM E[ADDR] ← #NUM	3		
0	0	1	1	0	R10	R9	R8	MOV R[ADDR], #NUM R[ADDR] ← #NUM	3		
0	0	1	1	1	R10	R9	R8	FILL R[ADDR], #NUM, CNT Loop CNT [RADDR+CNT] ← #NUM	4		
0	1	E10	E9	E8	R10	R9	R8	MOV R[ADDR], E[ADDR], CNT Loop CNT R[ADDR+CNT] ← E[ADDR+CNT]	4		
1	0	B2	B1	B0	E10	E9	E8	JB EADDR, Bit IF A.[Bit]=1 PC ← EADDR else PC+1	2		
1	1	0	0	0	E10	E9	E8	MOV E[ADDR], A E[ADDR] ← A_REG	2		
1	1	0	0	1	E10	E9	E8	MOV A, E[ADDR] A_REG ← E[ADDR]	2		•
1	1	0	1	0	0	X	X	MOV I[ADDR], A I[ADDR] ← A_REG	2		
1	1	0	1	0	1	X	X	MOV SPI, #NUM SPI ← #NUM (3 Bytes)	4		
1	1	0	1	1	0	X	X	MOV A, I[ADDR] A_REG ← I[ADDR]	2		•
1	1	0	1	1	1	0	0	FILLR LOOP R_REG_CNT R[R_REG_ADDR+CNT] ← R_REG_NUM	1		
1	1	0	1	1	1	0	1	TABLE MOV A, E[R_REG_ADDR] A_REG<=E[R_REG_ADDR]	1		•
1	1	0	1	1	1	1	0	RESERVED (1617 MCALL)	2		
1	1	0	1	1	1	1	1	JMPR PC ← R_REG_ADDR	1		
1	1	1	0	0	E10	E9	E8	JC EADDR IF C_REG=1 PC←EADDR else PC+1	2		
1	1	1	0	1	E10	E9	E8	JZ EADDR IF Z_REG=1 PC←EADDR else PC+1	2		
1	1	1	1	0	E10	E9	E8	JMP EADDR PC ← EADDR	2		
1	1	1	1	1	E10	E9	E8	CALL EADDR RET_ADDR ← Next Command Address PC ← EADDR (3 Layers of Address Stack)	2		

Table 7-5 Instruction Format

1 Byte–

OPCODE

|← *1byte* →|

Instruction: ADD; SUB; INC; DEC; CLR; COMP; MOV B A; HALT; AND; OR; XOR; NOT; SHR; SHL; XCHG; SWAP; NOTC; NOTZ; RET; JMPR; FILLR; TABLE

2 Bytes–

OPCODE	A7	A6	A5	A4	A3	A2	A1	A0

|← *1byte* →|← *1byte* →|

Instruction: MOV A, @I[ADDR]; MOV @I[ADDR], A

OPCODE	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

|← *1byte* →|← *1byte* →|

Instruction: MOV A, @R[ADDR]; MOV @R[ADDR], A; MOV A, @E[ADDR]; MOV @E[ADDR], A; JC EADDR; JZ EADDR; JMP EADDR; CALL EADDR

OPCODE	B2	B1	B0	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

|← *1byte* →|← *1byte* →|

Instruction: JB EADDR, Bit

OPCODE	#NUMBER

|← *1byte* →|← *1byte* →|

Instruction: MOV A, #NUM; MOV B, #NUM; DELAY #NUM

3 Bytes–

OPCODE	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	#NUMBER

|← *1byte* →|← *1byte* →|← *1byte* →|

Instruction: MOV @E[ADDR], #NUM; MOV @R[ADDR], #NUM

4 Bytes–

OPCODE	#NUMBER1	#NUMBER2	#NUMBER3

|← *1byte* →|← *1byte* →|← *1byte* →|← *1byte* →|

Instruction: MOV SPI, #NUM

OPCODE	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	#NUMBER	COUNT VALUE
	← *1byte* →	← *1byte* →	← *1byte* →	← *1byte* →									

Instruction: FILL @R[ADDR], #NUM, CNT

OPCODE	E 10	E 9	E 8	R 10	R 9	R 8	E 7	E 6	E 5	E 4	E 3	E 2	E 1	E 0	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0	COUNT VALUE
	← *1byte* →	← *1byte* →	← *1byte* →	← *1byte* →																				

Instruction: MOV @R[ADDR], @E[ADDR], CNT

7.2.3 Start and Interrupt

BIT1612 內建Script Control Function提供Interrupt Process機制，用以處理BIT1612 所產生的Interrupt (0x002[7:0])，並且支援自動Re-ACK機制，以減少程式碼的複雜度。相關的程式起始位置請參考 Table 7-6 。

Table 7-6 Start and Interrupt

Event	Type	Address
POR (Power On Reset)	Immediate	PC = 0x10
SIGIN (0x002[0])	Index	PC = 0x00, 0x01
NOSIG (0x002[1])	Index	PC = 0x02, 0x03
MODECHG (0x002[2])	Index	PC = 0x04, 0x05
VSYNC (0x002[3])	Index	PC = 0x06, 0x07
ERROR1 (0x002[4])	Index	PC = 0x08, 0x09
ERROR2 (0x002[5])	Index	PC = 0x0A, 0x0B
MV_CC (0x002[6])	Index	PC = 0x0C, 0x0D
IR_KEYIN (0x002[7])	Index	PC = 0x0E, 0x0F

7.2.4 Serial EEPROM and ROM Space Mapping

BIT1612 在硬體上可支援 24C16 及 24C32 兩種Serial EEPROM的通訊協定，指令集支援最高 2K的定址空間。使用小於 2KB程式記憶體時可以完全對映，但使用超過 2KB時，則需利用Bank Selection的方式擴增定址空間，運用R_EEPROM_BANK_SEL可以支援到 64KB的ROM Size (24C512)，如 Figure 7-5 所示。

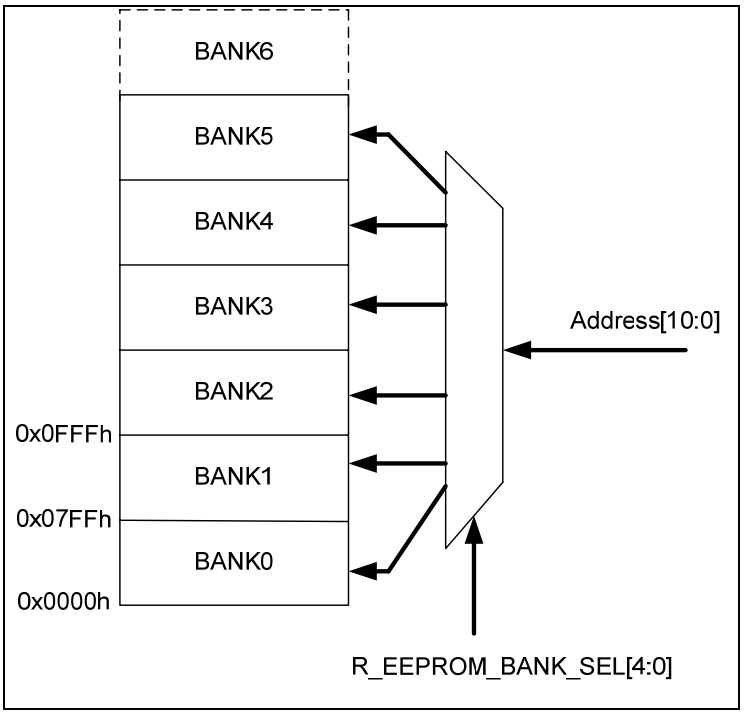


Figure 7-5 BIT1612 Script Controller Addressing Space

有些應用上希望使用超過 2KB的程式記憶體，除了使用 24C32 外，BIT1612 提供兩組TWSI的方式來進行程式記憶體空間的擴充，如 Figure 7-4。無論使用單 24C32 或是雙 24C16 的方式，在做跨Bank的動作時，一定要先設定R_EEPROM_BANK_SEL到正確的BANK。以 Figure 7-4 的情況爲例：

```
……                                          ; ROM 1, BANK0
MOV R_EEPROM_BANK_SEL, 001h
MOV R_REG_ADDR_L,   0A0h
MOV R_REG_ADDR_H,   003h
TABLE                                       ; A<= ROM2[0A0h], BANK1
MOV B, A                                    ; ROM1, BANK0
DEC
……
```

而在定址空間邊界上，則不能讓單一指令跨 BANK，如 MOV S, #NUM 爲 4-Byte 的指令，則 MOV S, #NUM 不能存放於 0x7FD、0x7FE、0x7FF，但可以存放在 0x7FC ~ 0x7FF。

```
0x7FC MOV S, NUM (OP Code)
0x7FD NUM 1
0x7FE NUM 2
0x7FF NUM 3
```

7.2.5 Serial EEPROM Write Protection and Power Monitor

BIT1612 新增Power Monitor 與Dynamic Write Protection功能，避免EEPROM在惡劣環境下產生非預期的誤動作。Dynamic Write Protection功能可以參考 Figure 7-2，將BIT1612 的OP2 接至 24C16 的WP Pin，並將R_WP_EN設爲 1 即可。Power Monitor功能則是會監控電壓是否正常，若不正常將停止對Serial EEPROM讀寫，並對Script MCU Reset，要使用此功能只要將R_PG_EN設爲 1，經過電壓比較器輸出的訊號接至BIT1612 的GIN7 即可。

7.2.6 Watch Dog Timer

BIT1612 有一 Watch Dog Timer (WDT)，R_WDT_SEL 可以選擇 Timer 的 Interval，當超過此 Interval

沒有對 R_WDT_CLEAR 執行寫入 1、寫入 0 的動作，Script MCU 會自動 Reset，透過 R_WDT_OV 可以得知本次 Reset 是起因於正常開機還是 WDT Overflow 所導致。

7.2.7 Second TWSI for Multi-Processor Communication

BIT1612 預留OP2 and OP3 爲Multi-Processor Communication Port，其Protocol與TWSI相容，透過設定R_TWSI_SEC可以開啓此功能，其示意圖如 Figure 7-3。其工作原理是在此BUS上的動作符合預設的條件時，就會產生中斷，此時中斷服務程式就可以執行Multi-Processor Communication的程式。

設定 R_TWSI_DET_MODE 可以決定 TWSI 何種動作會觸動 Interrupt[3]；R_TWSI_SEC_SLAVE[1:0] 決定 BIT1612 在 TWSI 上的 Device Address，R_TWSI_DET_IN[7:0]及 R_TWSI_DET_OUT[7:0]則是透過此 BUS 讀寫的資料，R_TWSI_DET_VALUE 配合 R_TWSI_DET_MODE 可以在特定的 Register Address 下產生中斷。

7.2.8 TWSI Write/Read

BIT1612 可以運用 MOV @IADDR, A 和 MOV A, @IADDR 指令，與 R_TWSI_SLAVE 方便地存取位於｛OP1, OP0｝上的元件內部資料，與 Serial EEPROM 相同，透過最省成本的分時多工方式完成周邊控制，要注意 TWSI 由於是分享給不同的 Device，所以不允許此 TWSI 上同時有第二個 Device Address 是 1010XXX 的元件出現。

7.2.9 SPI Interface

BIT1612 爲了支援 SPI Interface 的 LCD Panel，附加了符合多種規格的 SPI Interface 的功能，透過 R_SPI_CTRL 及 MOV S, #NUM 指令可輕易地完成 LCD Panel 設定功能。SPI 信號可由 R_SPI1_EN 及 R_SPI2_EN 選擇由 BOUT Port 或是 SRGB_D Port 輸出。

7.2.10 Debug Mode

爲了方便在韌體工程師設計 Master Mode 的程序，將 R_MCU_DEBUG 設爲 1，切換 Master 與 Slave 時將不會 Reset，因此可以運用 Master 執行到一 HALT 點後，再切換至 Slave Mode 讀回 BIT1612 內部狀態的技巧進行 Debug。若應用於 Slave Mode 則必須將 R_MCU_DEBUG 設爲 0。

7.3 Slave Mode

BIT1612 提供 BiTEKbus 或 Two-Wire Serial Interface (TWSI) 兩種 Protocol 來存取 Register Sets，並由 OP4 Pin 來決定所選用的 Protocol。當 OP4 爲 1，選用 BiTEKbus Protocol；當 OP4 爲 0，則選用 TWSI Protocol。

7.3.1 BiTEKbus Protocol

BIT1612 可由外部 Pins (OP3 and OP2) 來決定 Slave Address，相關的 Slave Address 請參考下表。

Table 7-7 BiTEKbus Slave Address

OP3	OP2	Slave Address
0	0	Slave Address = 0x81
0	1	Slave Address = 0x83
1	0	Slave Address = 0x85
1	1	Slave Address = 0x87

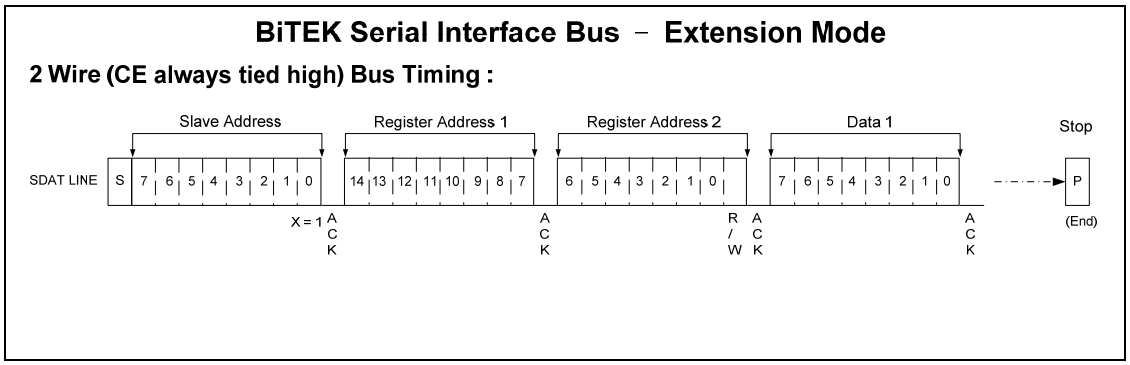


Figure 7-6 Bitek Serial Interface Bus – Extension Mode

7.3.2 TWSI Protocol

BIT1612 Slave Address 也支援 Two-Wire Serial Interface (TWSI) Protocol，以便對 BIT1612 Register Sets 做存取動作。

7.3.2.1 TWSI Protocol Device Address

BIT1612 TWSI Protocol 須在送出 Start Bit 之後送出 8 Bits Device Address (Slave Address)，並可由外部 PIN (OP3 and OP2)決定其 Device Address 的 Bit6 and Bit5 位址。相關設定請參考下表。

Table 7-8 TWSI Protocol Device Address

Internal Register Address	Write Device Address	Read Device Address
0x000~0x0FF (Register Bank1)	0x00(PIN104 = 0、PIN105=0) 0x20(PIN104 = 0、PIN105=1) 0x40(PIN104 = 1、PIN105=0) 0x60(PIN104 = 1、PIN105=1)	0x01(PIN104 = 0、PIN105=0) 0x21(PIN104 = 0、PIN105=1) 0x41(PIN104 = 1、PIN105=0) 0x61(PIN104 = 1、PIN105=1)
0x100~0x17F (Register Bank2)	0x02(PIN104 = 0、PIN105=0) 0x22(PIN104 = 0、PIN105=1) 0x42(PIN104 = 1、PIN105=0) 0x62(PIN104 = 1、PIN105=1)	0x03(PIN104 = 0、PIN105=0) 0x23(PIN104 = 0、PIN105=1) 0x43(PIN104 = 1、PIN105=0) 0x63(PIN104 = 1、PIN105=1)
0x200~0x2FF (Gamma Table)	0x04(PIN104 = 0、PIN105=0) 0x24(PIN104 = 0、PIN105=1) 0x44(PIN104 = 1、PIN105=0) 0x64(PIN104 = 1、PIN105=1)	0x05(PIN104 = 0、PIN105=0) 0x25(PIN104 = 0、PIN105=1) 0x45(PIN104 = 1、PIN105=0) 0x65(PIN104 = 1、PIN105=1)
0x300~0x33F (OSD Attribute RAM)	0x06(PIN104 = 0、PIN105=0) 0x26(PIN104 = 0、PIN105=1) 0x46(PIN104 = 1、PIN105=0) 0x66(PIN104 = 1、PIN105=1)	0x07(PIN104 = 0、PIN105=0) 0x27(PIN104 = 0、PIN105=1) 0x47(PIN104 = 1、PIN105=0) 0x67(PIN104 = 1、PIN105=1)
0x400~0x4FF (OSD Display RAM)	0x08(PIN104 = 0、PIN105=0) 0x28(PIN104 = 0、PIN105=1) 0x48(PIN104 = 1、PIN105=0) 0x68(PIN104 = 1、PIN105=1)	0x09(PIN104 = 0、PIN105=0) 0x29(PIN104 = 0、PIN105=1) 0x49(PIN104 = 1、PIN105=0) 0x69(PIN104 = 1、PIN105=1)
0x500~0x5FF (OSD Display RAM)	0x0A(PIN104 = 0、PIN105=0) 0x2A(PIN104 = 0、PIN105=1) 0x4A(PIN104 = 1、PIN105=0) 0x6A(PIN104 = 1、PIN105=1)	0x0B(PIN104 = 0、PIN105=0) 0x2B(PIN104 = 0、PIN105=1) 0x4B(PIN104 = 1、PIN105=0) 0x6B(PIN104 = 1、PIN105=1)
0x600~0x6FF (OSD User Font RAM)	0x0C(PIN104 = 0、PIN105=0) 0x2C(PIN104 = 0、PIN105=1) 0x4C(PIN104 = 1、PIN105=0) 0x6C(PIN104 = 1、PIN105=1)	0x0D(PIN104 = 0、PIN105=0) 0x2D(PIN104 = 0、PIN105=1) 0x4D(PIN104 = 1、PIN105=0) 0x6D(PIN104 = 1、PIN105=1)
0x700~0x71F (Buffer)	0x0E(PIN104 = 0、PIN105=0) 0x2E(PIN104 = 0、PIN105=1) 0x4E(PIN104 = 1、PIN105=0) 0x6E(PIN104 = 1、PIN105=1)	0x0F(PIN104 = 0、PIN105=0) 0x2F(PIN104 = 0、PIN105=1) 0x4F(PIN104 = 1、PIN105=0) 0x6F(PIN104 = 1、PIN105=1)

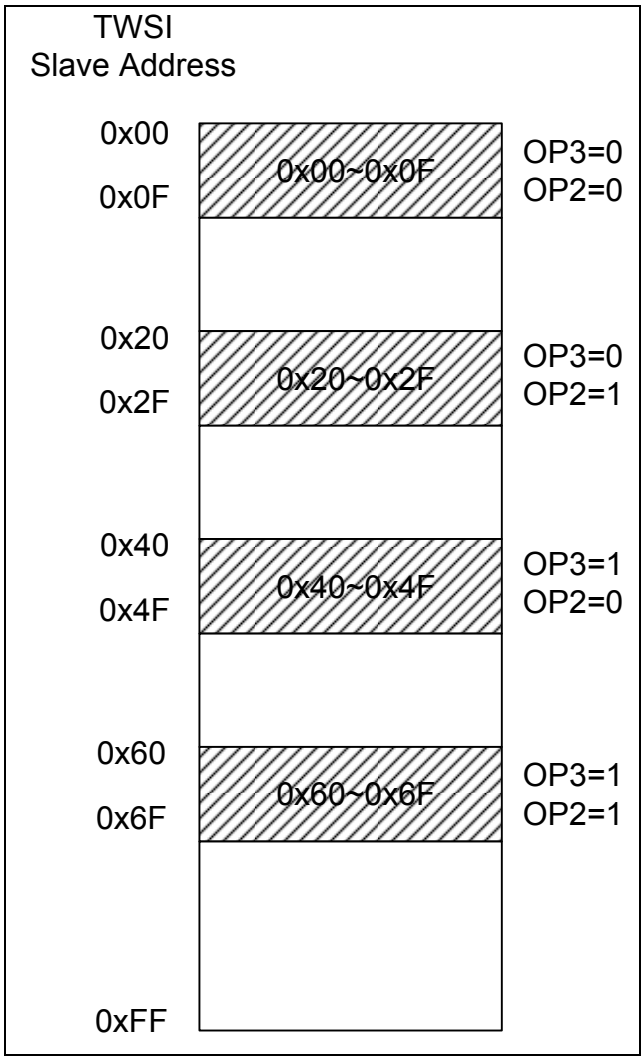


Figure 7-7 TWSI Slave Mapping Address

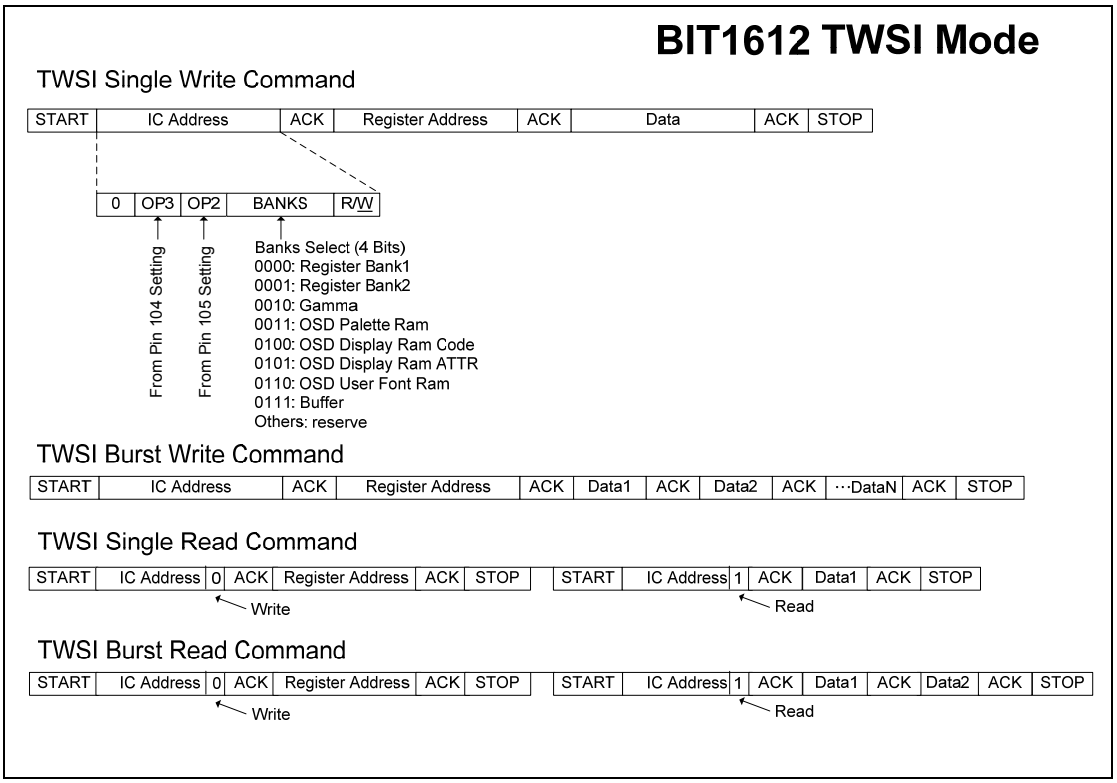
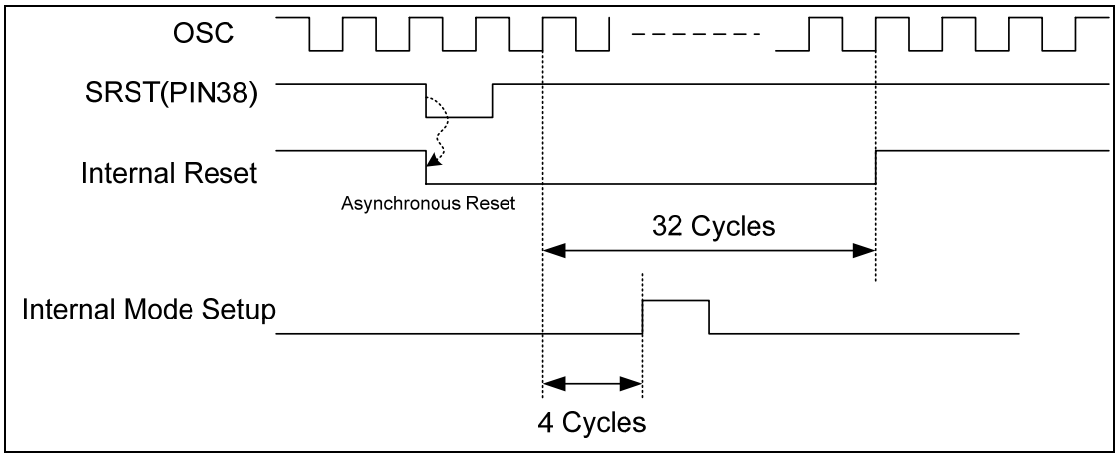


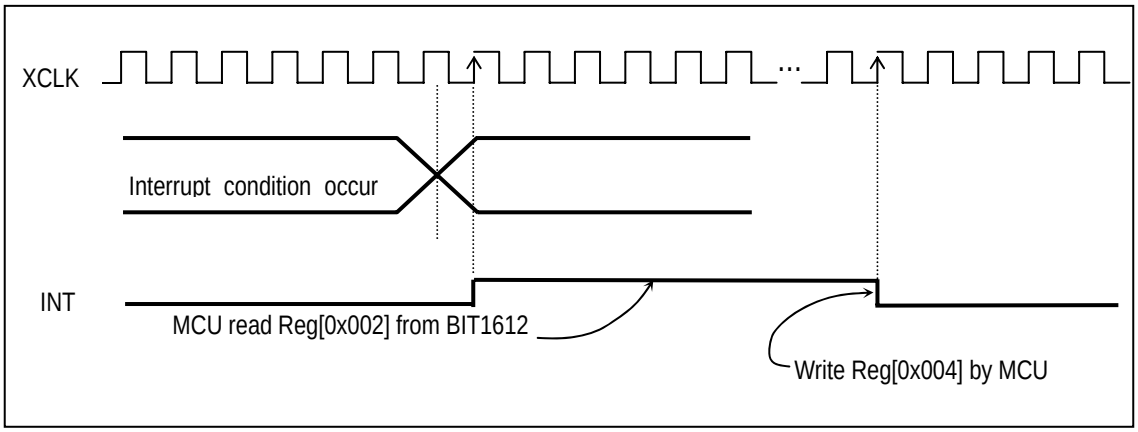
Figure 7-8 TWSI Read/Write Mode

8 Timing Diagram

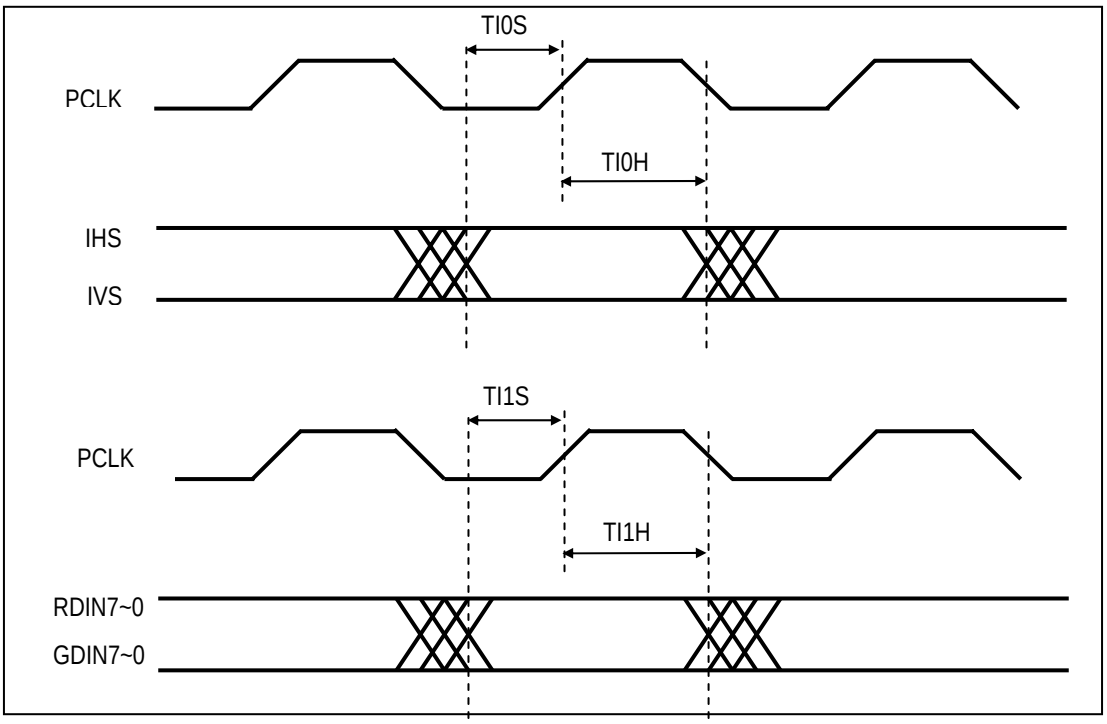
8.1 Hardware Reset



8.2 Clock and Interrupt

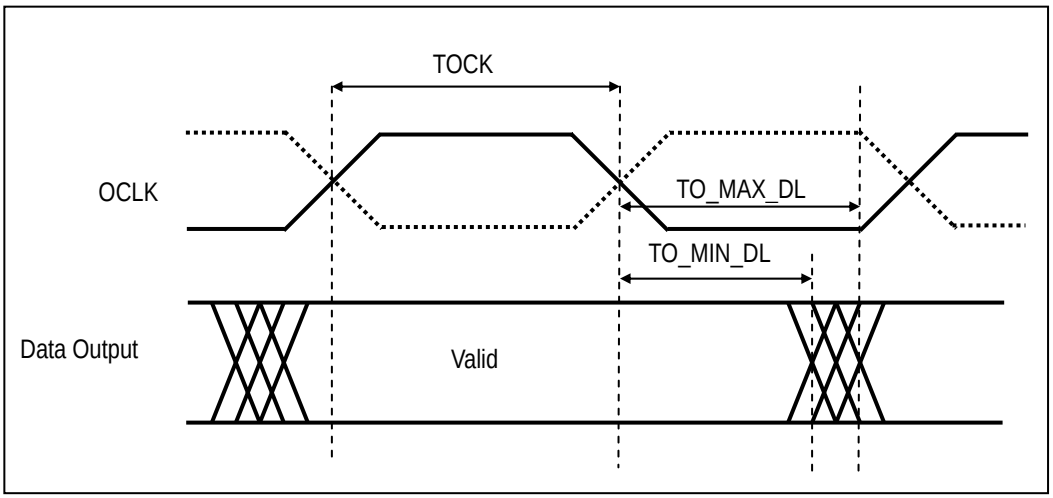


8.3 Input Signal



Symbol	Describe	Max.	Min.	Unit
TI0S, TI1S	Input Setup time		2	Ns
TI0H, TI1H	Input Hold time		2	Ns

8.4 Output Signal



Symbol	Describe	Timing	Unit
TOCK	Output clock half period		ns
TO_MAX_DL	Output signal Max delay	TOCK - 1	ns
TO_MIN_DL	Output signal Min delay	TOCK - 4	ns

9 Electrical Characteristic

9.1 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	-0.5		3.6	V
VDD18	Supply Voltage for Digital Core	- 0.5		2.5	V
V_{IN}	Input Voltage for Digital Core (5V Tolerant)	- 0.5		6	V
T_{STG}	Storage Temperature	- 40		125	℃

9.2 Recommend Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	3.0	3.3	3.6	V
VDD18	Supply Voltage for Digital Core	1.62	1.8	1.98	V
VDD33	Supply Voltage for I/O Pad	3.0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	℃

9.3 DC Electrical Characters

(under Recommend Operating Condition and T_J =0℃ to 115℃)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	No pull-up nor pull-down			10	uA
I_{OZ}	Tri-state Leakage Current				10	uA
V_{IL}	Input Low Voltage	CMOS	-0.3		0.8	V
V_{IH}	Input High Voltage	CMOS	2.0		5.5	V
V_{OL}	Output Low Voltage	I_{OL}= 4,8,16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= 4,8, 16 mA	2.4			V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	0.89	0.94	0.99	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	1.44	1.50	1.56	V
Rpu	Pull-up Resistance		39	65	116	KΩ
Rpd	Pull-down Resistance		40	56	108	KΩ

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance about 0.5pF and the package capacitance.

10 Soldering Information

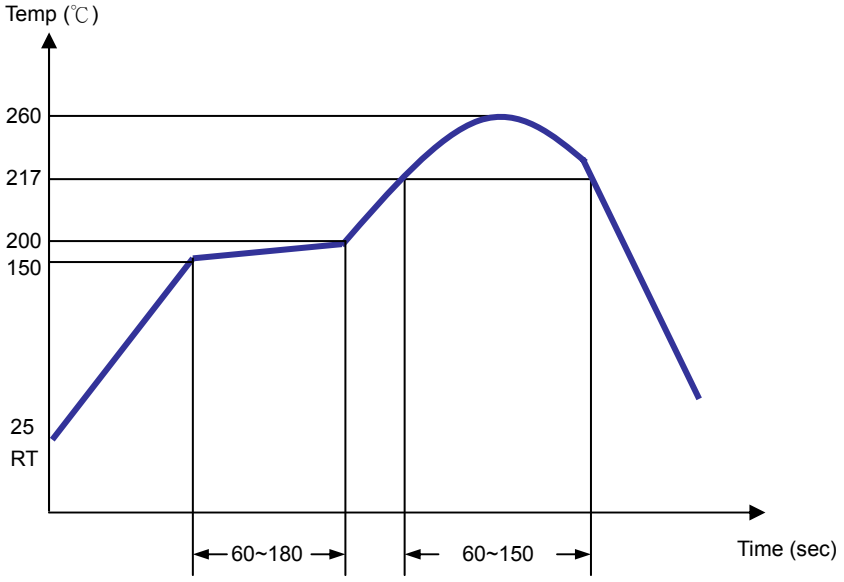
10.1 Reflow Soldering

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



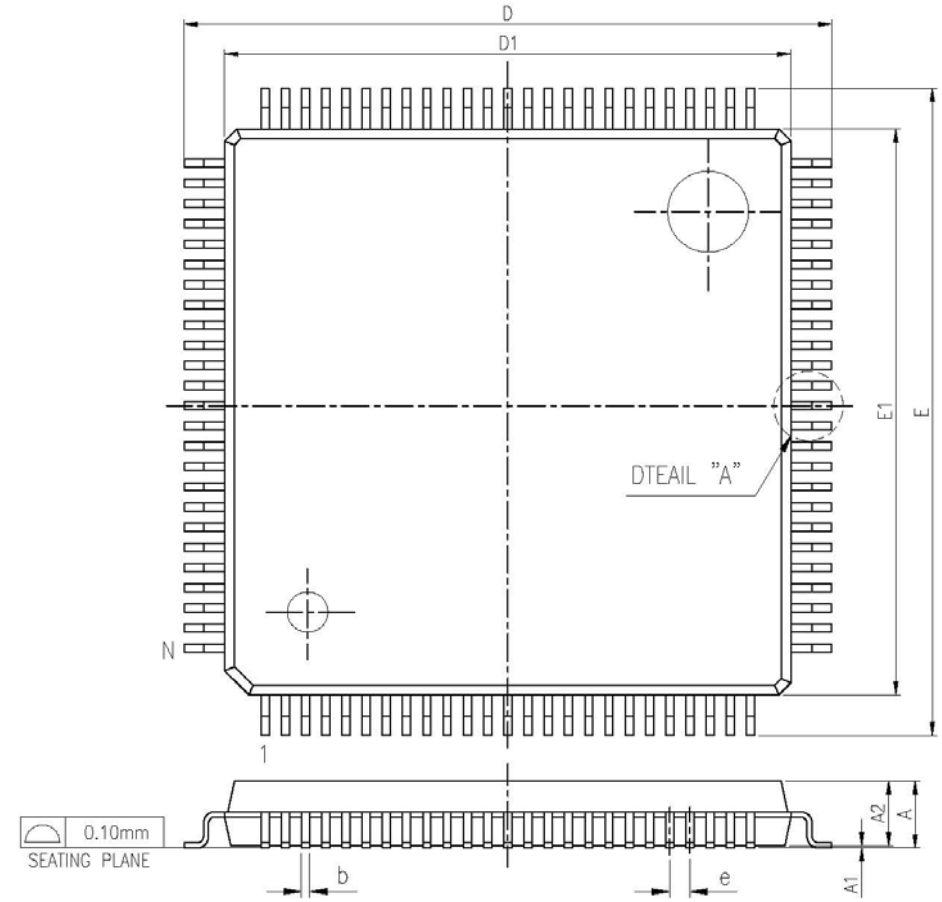
10.2 Wave Soldering

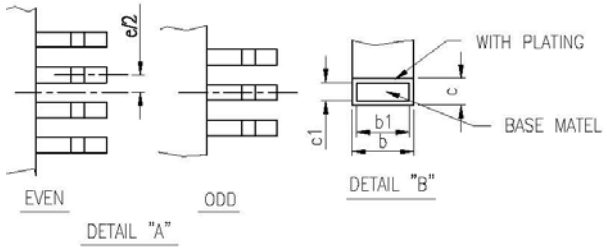
Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

10.3 Manual Soldering

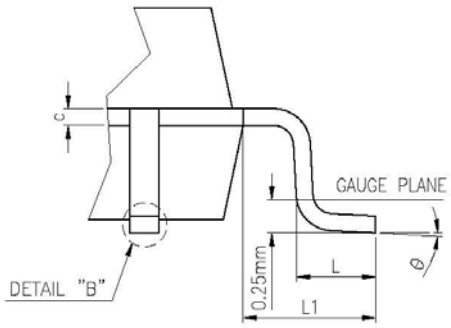
Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11 Package Information





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	15.90	16.00	16.10	0.626	0.630	0.634
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.90	16.00	16.10	0.626	0.630	0.634
E1	13.90	14.00	14.10	0.547	0.551	0.555
⚠ c	0.178			0.007		
c1	0.127 BSC.			0.005 BSC.		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7



DETAIL"A"	ODD	EVEN
⚠ b ±0.03	0.22	0.18
⚠ b1±0.03	0.20	0.16
e (BSC)	0.50	0.40
N	100L	128L
JEDEC	MS-026 BED	

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