BJ8P509F

PRODUCT

SPECIFICATION

(V1.0)

Contents

1.Features

- Only 42 single word instructions
- All instructions are single cycle except for program branches which are two-cycle
- 13-bit wide instructions
- All OTP ROM area GOTO instruction
- All OTP ROM area subroutine CALL instruction
- 8-bit wide data path
- 5-level deep hardware stack
- Operating speed: DC-20 MHz clock input
  DC-100 ns instruction cycle

Device	Pins#	I/O#	OTP ROM(word)	Ram(Byte)
BJ8P509FNB	8	6	1K	49
BJ8P509FDB	8	6	1K	49
BJ8P509FGA	6	4	1K	49
BJ8P509FTB	8	6	1K	49

- Direct, indirect addressing modes for data accessing
- 8-bit real time clock/counter (Timer0) with 8-bit programmable pre-scaler
- Internal Power-on Reset (POR)
- Built-in Low Voltage Detector (LVD) for Brown-out Reset (BOR)
- Power-up Reset Timer (PWRT) and Oscillator Start-up Timer(OST)
- On chip Watchdog Timer (WDT) with internal oscillator for reliable operation and soft-ware watch-dog enable/disable control
- One I/O port IOB with independent direction control
- Soft-ware I/O pull-high/pull-down or open-drain control
- One internal interrupt source: Timer0 overflow; Two external interrupt source: INT pin, Port B input change
- Wake-up from SLEEP by INT pin or Port B input change
- Power saving SLEEP mode
- Built-in 8MHz, 4MHz, 1MHz, and 455KHz internal RC oscillator
- Programmable Code Protection
- Built-in internal RC oscillator
- Selectable oscillator options:
  - ERC: External Resistor/Capacitor Oscillator
  - HF: High Frequency Crystal/Resonator Oscillator
  - XT: Crystal/Resonator Oscillator
  - LF: Low Frequency Crystal Oscillator
  - IRC: Internal Resistor/Capacitor Oscillator
  - ERIC: External Resistor/Internal Capacitor Oscillator
- Wide-operating voltage range: 2.3V to 5.5V

2.General Description

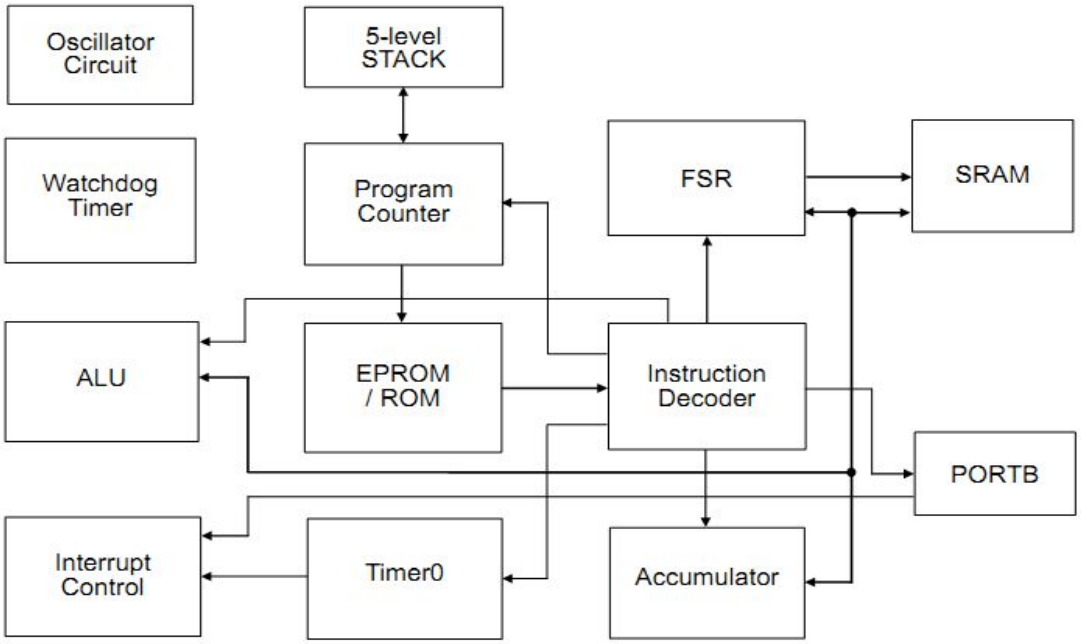
The BJ8P509F series is a family of low-cost, high speed, high noise immunity, OTP ROM-based 8-bit CMOS Micro-controllers. It employs a RISC architecture with only 42 instructions. All instructions are single cycle except for program branches which take two cycles. The easy to use and easy to remember instruction set reduces development time significantly.

The BJ8P509F series consists of Power-on Reset (POR), Brown-out Reset (BOR), Power-up Reset Timer (PWRT), Oscillator Start-up Timer(OST), Watchdog Timer, OTP ROM, SRAM, tristate I/O port, I/O pull-high/open-drain/pull-down control, Power saving SLEEP mode, real time programmable clock/counter, Interrupt, Wake-up from SLEEP mode, and Code Protection for these products. There are three oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator.

The BJ8P509F address 1K×13 of program memory.

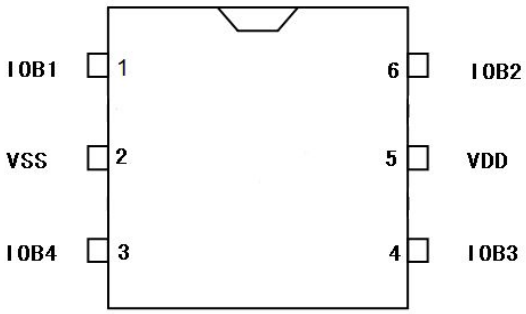
The BJ8P509F can directly or indirectly address its register files and data memory. All special function registers including the program counter are mapped in the data memory.

3. Block Diagram

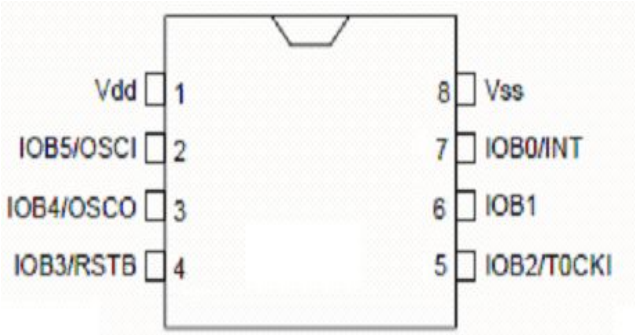


4. Pin connection and Pin descriptions

4.1 Pin Assignments



SOT23-6



8-PIN SOP/DIP/TSSOP

4.2 Pin descriptions

Name	I/O	Description
IOB0/INT	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down / External interrupt input
IOB1	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down
IOB2/T0CKI	I/O	Bi-direction I/O pin with system wake-up function Software controlled pull-high/open-drain/pull-down / External clock input to Timer0
IOB3/RSTB	I	IOB3 is input pin only with system wake-up function / System clear (RESET) input. Active low RESET to the device. Weak pull-high always on if configured as RSTB.
IOB4/OSCO	I/O	Bi-direction I/O pin with system wake-up function (RCOUT optional in IRC/ERIC, ERC mode) Software controlled pull-high/open-drain / Oscillator crystal output (XT, LP mode) Outputs with the instruction cycle rate (RCOUT optional in IRC/ERIC, ERC mode)
IOB5/OSCI	I/O	Bi-direction I/O pin with system wake-up function (IRC mode) Software controlled pull-high/open-drain / Oscillator crystal input (XT, LP mode) External clock source input (ERIC, ERC mode)
Vdd	-	Positive supply
Vss	-	Ground

Legend: I=input, O=output, I/O=input/output

5.memory organization

BJ8P509F memory is organized into program memory and data memory.

5.1 Program Memory Organization

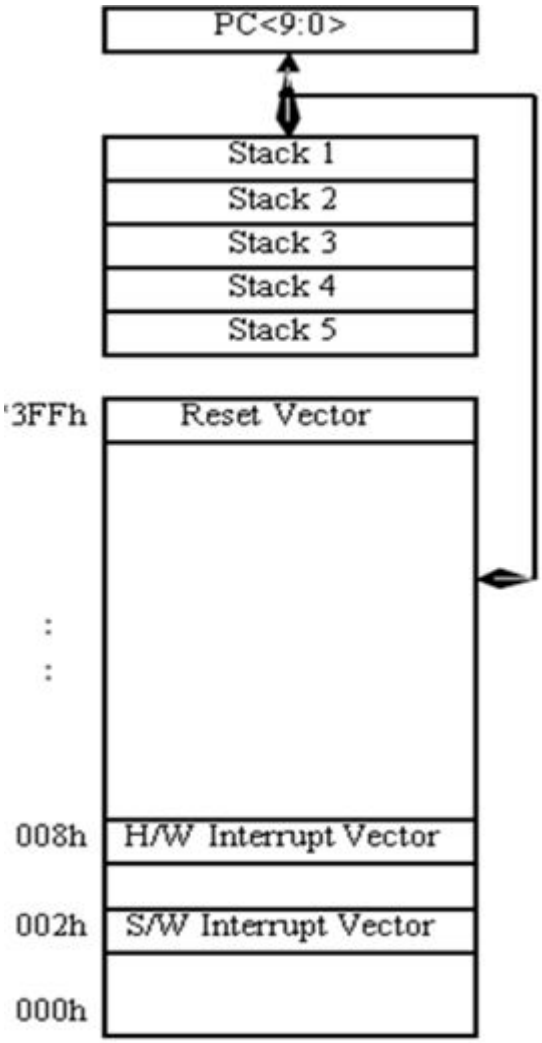
The BJ8P509F have a 10-bit Program Counter capable of addressing a 1K×13 program memory space.

The RESET vector for the BJ8P509F is at 3FFh.

The H/W interrupt vector is at 008h. And the S/W interrupt vector is at 002h.

BJ8P509F supports all OTP ROM area CALL/GOTO instructions without page.

FIGURE 1.1: Program Memory Map and STACK



5.2 Data Memory Organization

Data memory is composed of Special Function Registers and General Purpose Registers.

The General Purpose Registers are accessed either directly or indirectly through the FSR register.

The Special Function Registers are registers used by the CPU and peripheral functions to control the operation of the device.

TABLE 1.1: Registers File Map for BJ8P509 Series

Address	Description
00h	INDF
01h	TMR0
02h	PCL
03h	STATUS
04h	FSR
05h	
06h	PORTB
07h	General Purpose Register
08h	PCON
09h	WUCON
0Ah	PCHBUF
0Bh	PDCON
0Ch	ODCON
0Dh	PHCON
0Eh	INTEN
0Fh	INTFLAG
10h ~ 3Fh	General Purpose Registers

N/A	OPTION
06h	IOSTB

TABLE 1.2: The Registers Controlled by OPTION or IOST Instructions

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
06h (w)	IOSTB	Port B I/O Control Register							

TABLE 1.3: Operational Registers Map

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							
01h (r/w)	TMR0	8-bit real-time clock/counter							
02h (r/w)	PCL	Low order 8 bits of PC							
03h (r/w)	STATUS	RST	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
04h (r/w)	FSR	*	*	Indirect data memory address pointer					
05h	-	Reserved							
06h (r/w)	PORTB	—	—	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0
07h (r/w)	SRAM	General Purpose Register							
08h (r/w)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*
09h (r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0
0Ah (r/w)	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	
0Bh (r/w)	PDCON		/PDB2	/PDB1	/PDB0				
0Ch (r/w)	ODCON	ODB7	ODB6	ODB5	ODB4		ODB2	ODB1	ODB0
0Dh (r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4		/PHB2	/PHB1	/PHB0
0Eh (r/w)	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE
0Fh (r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

Legend: - = unimplemented, read as '0', * = unimplemented, read as '1',

6. Functional description

6.1 Operational Registers

6.1.1 INDF (Indirect Addressing Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
00h (r/w)	INDF	Uses contents of FSR to address data memory (not a physical register)							

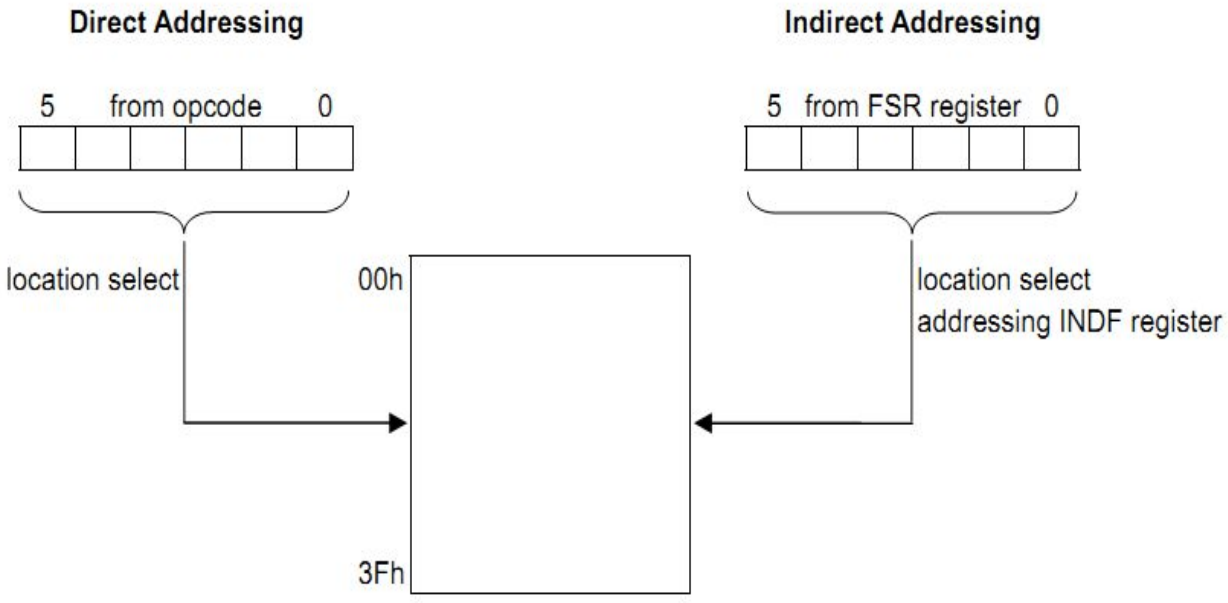
The INDF Register is not a physical register. Any instruction accessing the INDF register can actually access the register pointed by FSR Register. Reading the INDF register itself indirectly (FSR="0") will read 00h. Writing to the INDF register indirectly results in a no-operation (although status bits may be affected).

The bits 5-0 of FSR register are used to select up to 64 registers (address: 00h ~ 3Fh).

EXAMPLE 2.1: INDIRECT ADDRESSING

- Register file 38 contains the value 10h
- Register file 39 contains the value 0Ah
- Load the value 38 into the FSR Register
- A read of the INDF Register will return the value of 10h
- Increment the value of the FSR Register by one (@FSR=39h)
- A read of the INDR register now will return the value of 0Ah.

FIGURE 2.1: Direct/Indirect Addressing



6.1.2 TMR0 (Time Clock/Counter register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
01h (r/w)	TMR0	8-bit real-time clock/counter							

6.1.3 PCL (Low Bytes of Program Counter) & Stack

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
02h (r/w)	PCL	Low order 8 bits of PC							

BJ8P509F devices have a 10-bit wide Program Counter (PC) and five-level deep 10-bit hardware push/pop stack.

The low byte of PC is called the PCL register. This register is readable and writable. The high byte of PC is called the PCH register. This register contains the PC<9:8> bits and is not directly readable or writable. All updates to the PCH register go through the PCHBUF register. As a program instruction is executed, the Program Counter will contain the address of the next program instruction to be executed. The PC value is increased by one, every instruction cycle, unless an instruction changes the PC.

For a GOTO instruction, the PC<9:0> is provided by the GOTO instruction word. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.

For a CALL instruction, the PC<9:0> is provided by the CALL instruction word. The next PC will be loaded (Pushed) onto the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated. For a RETIA, RETFIE, or RETURN instruction, the PC are updated (Popped) from the top of STACK. The PCL register is mapped to PC<7:0>, and the PCHBUF register is not updated.

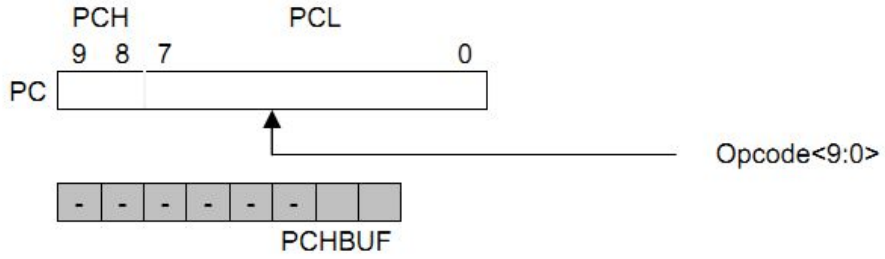
For any instruction where the PCL is the destination, the PC<7:0> is provided by the instruction word or ALU result.

However, the PC<9:8> will come from the PCHBUF<1:0> bits (PCHBUF PCH).

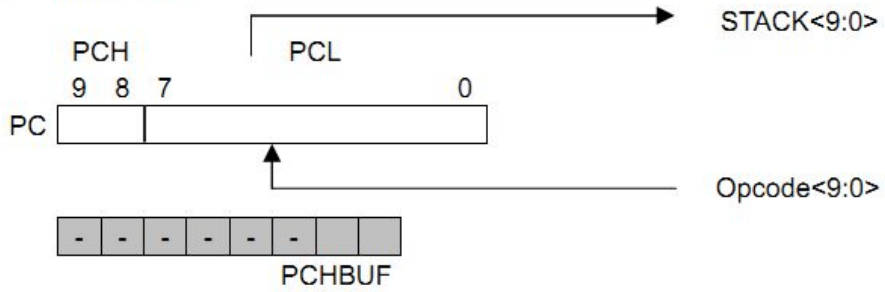
PCHBUF register is never updated with the contents of PCH.

FIGURE 2.2: Loading of PC in Different Situations

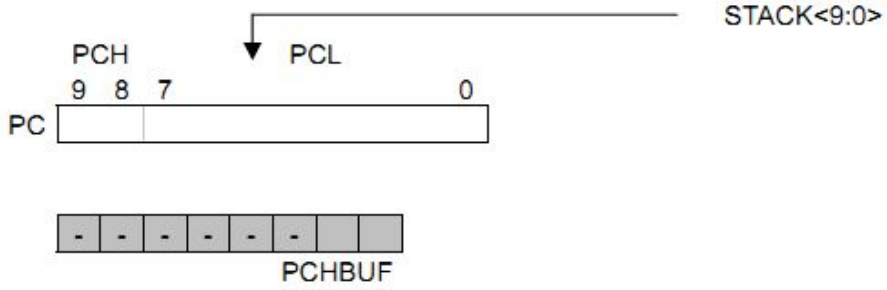
Situation 1: GOTO Instruction



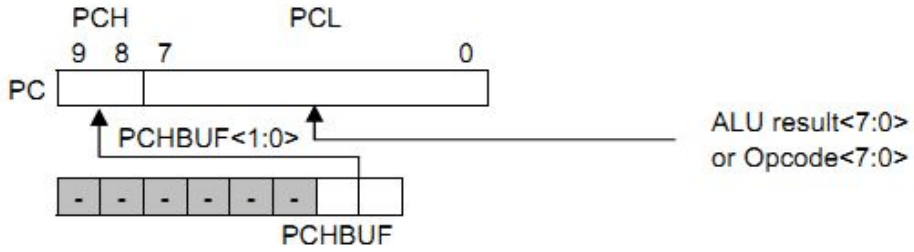
Situation 2: CALL Instruction



Situation 3: RETIA, RETFIE, or RETURN Instruction



Situation 4: Instruction with PCL as destination



Note: 1. PCHBUF is used only for instruction with PCL as destination for BJ8P508

6.1.4 STATUS (Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
03h (r/w)	STATUS	RST	GP1	GP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

This register contains the arithmetic status of the ALU, the RESET status.

If the STATUS Register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS Register as destination may be different than intended. For example, CLRR STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS Register as 000u u1uu (where u = unchanged).

C : Carry/borrow bit.

ADDAR, ADDIA

= 1, a carry occurred.

= 0, a carry did not occur.

SUBAR, SUBIA

= 1, a borrow did not occur.

= 0, a borrow occurred.

Note : A subtraction is executed by adding the two's complement of the second operand. For rotate (RRR, RLR) instructions, this bit is loaded with either the high or low order bit of the source register.

DC : Half carry/half borrow bit.

ADDAR, ADDIA

= 1, a carry from the 4th low order bit of the result occurred.

= 0, a carry from the 4th low order bit of the result did not occur.

SUBAR, SUBIA

= 1, a borrow from the 4th low order bit of the result did not occur.

= 0, a borrow from the 4th low order bit of the result occurred.

Z : Zero bit.

= 1, the result of a logic operation is zero.

= 0, the result of a logic operation is not zero.

PD : Power down flag bit.

= 1, after power-up or by the CLRWDT instruction.

= 0, by the SLEEP instruction.

TO : Time overflow flag bit.

= 1, after power-up or by the CLRWDT or SLEEP instruction.

= 0, a watch-dog time overflow occurred.

GP1:GP0 : General purpose read/write bits.

RST : Bit for wake-up type.
= 1, Wake-up from SLEEP on Port B input change.
= 0, Wake-up from other reset types.

6.1.5 FSR (Indirect Data Memory Address Pointer)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
04h (r/w)	FSR	*	*	Indirect data memory address pointer					

Bit5:Bit0 : Select registers address in the indirect addressing mode. See 2.1.1 for detail description.

Bit7:Bit6 : Not used. Read as “1”s.

6.1.6 PORTB (Port Data Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
06h (r/w)	PORTB	IOB7	IOB6	IOB5	IOB4	IOB3	IOB2	IOB1	IOB0

Reading the port (PORTB register) reads the status of the pins independent of the pin’s input/output modes. Writing
to these ports will write to the port data latch.
PORTB is a 8-bit port data register. And IOB3 is input only.

6.1.7 PCON (Power Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
08h (r/w)	PCON	WDTE	EIS	LVDTE	*	*	*	*	*

Bit4:Bit0 : Not used. Read as “1”s.

LVDTE : LVDT (low voltage detector) enable bit.
= 0, Disable LVDT.
= 1, Enable LVDT.

EIS : Define the function of IOB0/INT pin.
= 0, IOB0 (bi-directional I/O pin) is selected. The path of INT is masked.
= 1, INT (external interrupt pin) is selected. In this case, the I/O control bit of IOB0 must be set to “1”. The path of Port B input change of IOB0 pin is masked by

hardware, the status of INT pin can also be read by way of reading PORTB.

WDTE : WDT (watch-dog timer) enable bit.
= 0, Disable WDT.
= 1, Enable WDT.

6.1.8 WUCON (Port B Input Change Interrupt/Wake-up Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
09h (r/w)	WUCON	WUB7	WUB6	WUB5	WUB4	WUB3	WUB2	WUB1	WUB0

WUB0 : = 0, Disable the input change interrupt/wake-up function of IOB0 pin.
= 1, Enable the input change interrupt/wake-up function of IOB0 pin.

WUB1 : = 0, Disable the input change interrupt/wake-up function of IOB1 pin.
= 1, Enable the input change interrupt/wake-up function of IOB1 pin.

WUB2 : = 0, Disable the input change interrupt/wake-up function of IOB2 pin.
= 1, Enable the input change interrupt/wake-up function of IOB2 pin.

WUB3 : = 0, Disable the input change interrupt/wake-up function of IOB3 pin.
= 1, Enable the input change interrupt/wake-up function of IOB3 pin.

WUB4 : = 0, Disable the input change interrupt/wake-up function of IOB4 pin.
= 1, Enable the input change interrupt/wake-up function of IOB4 pin.

WUB5 : = 0, Disable the input change interrupt/wake-up function of IOB5 pin.
= 1, Enable the input change interrupt/wake-up function of IOB5 pin.

6.1.9 PCHBUF (High Byte Buffer of Program Counter)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ah (r/w)	PCHBUF	-	-	-	-	-	-	2 MSBs Buffer of PC	

Bit1:Bit0 : See 2.1.3 for detail description.

Bit7:Bit2 : Not used. Read as “0”s.

6.1.10 PDCON (Pull-down Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Bh (r/w)	PDCON		/PDB2	/PDB1	/PDB0				

Bit3:0 : General purpose read/write bits.

/PDB0 : = 0, Enable the internal pull-down of IOB0 pin.
= 1, Disable the internal pull-down of IOB0 pin.

/PDB1 : = 0, Enable the internal pull-down of IOB1 pin.
= 1, Disable the internal pull-down of IOB1 pin.

/PDB2 : = 0, Enable the internal pull-down of IOB2 pin.
= 1, Disable the internal pull-down of IOB2 pin.

Bit7 : General purpose read/write bit.

6.1.11 ODCON (Open-drain Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Ch (r/w)	ODCON	ODB7	ODB6	ODB5	ODB4		ODB2	ODB1	ODB0

ODB0 : = 0, Disable the internal open-drain of IOB0 pin.
= 1, Enable the internal open-drain of IOB0 pin.

ODB1 : = 0, Disable the internal open-drain of IOB1 pin.
= 1, Enable the internal open-drain of IOB1 pin.

ODB2 : = 0, Disable the internal open-drain of IOB2 pin.
= 1, Enable the internal open-drain of IOB2 pin.

Bit3 : General purpose read/write bit.

ODB4 : = 0, Disable the internal open-drain of IOB4 pin.
= 1, Enable the internal open-drain of IOB4 pin.

ODB5 : = 0, Disable the internal open-drain of IOB5 pin.
= 1, Enable the internal open-drain of IOB5 pin.

6.1.12 PHCON (Pull-high Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Dh (r/w)	PHCON	/PHB7	/PHB6	/PHB5	/PHB4		/PHB2	/PHB1	/PHB0

/PHB0 : = 0, Enable the internal pull-high of IOB0 pin.
= 1, Disable the internal pull-high of IOB0 pin.

/PHB1 : = 0, Enable the internal pull-high of IOB1 pin.
= 1, Disable the internal pull-high of IOB1 pin.

/PHB2 : = 0, Enable the internal pull-high of IOB2 pin.
= 1, Disable the internal pull-high of IOB2 pin.

Bit3 : General purpose read/write bit.

/PHB4 : = 0, Enable the internal pull-high of IOB4 pin.
= 1, Disable the internal pull-high of IOB4 pin.

/PHB5 : = 0, Enable the internal pull-high of IOB5 pin.
= 1, Disable the internal pull-high of IOB5 pin.

6.1.13 INTEN (Interrupt Mask Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Eh (r/w)	INTEN	GIE	*	*	*	*	INTIE	PBIE	T0IE

T0IE : Timer0 overflow interrupt enable bit.
= 0, Disable the Timer0 overflow interrupt.
= 1, Enable the Timer0 overflow interrupt.

PBIE : Port B input change interrupt enable bit.
= 0, Disable the Port B input change interrupt.
= 1, Enable the Port B input change interrupt .

INTIE : External INT pin interrupt enable bit.
= 0, Disable the External INT pin interrupt.
= 1, Enable the External INT pin interrupt.

Bit6:BIT3 : Not used. Read as “1”s.

GIE : Global interrupt enable bit.
= 0, Disable all interrupts. For wake-up from SLEEP mode through an interrupt event, the device will continue execution at the instruction after the SLEEP instruction.

= 1, Enable all un-masked interrupts. For wake-up from SLEEP mode through an interrupt event, the device will branch to the interrupt address (008h).

Note : When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts. The RETFIE instruction will exit the interrupt routine and set the GIE bit to re-enable interrupt.

6.1.14 INTFLAG (Interrupt Status Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
0Fh (r/w)	INTFLAG	-	-	-	-	-	INTIF	PBIF	T0IF

T0IF : Timer0 overflow interrupt flag. Set when Timer0 overflows, reset by software.

PBIF : Port B input change interrupt flag. Set when Port B input changes, reset by software.

INTIF : External INT pin interrupt flag. Set by rising/falling (selected by INTEDG bit (OPTION<6>)) edge on INT pin, reset by software.

Bit7:BIT3 : Not used. Read as “0”s.

6.1.15 ACC (Accumulator)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (r/w)	ACC	Accumulator							

Accumulator is an internal data transfer, or instruction operand holding. It can not be addressed.

6.1.16 OPTION Register

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
N/A (w)	OPTION	*	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Accessed by OPTION instruction.

By executing the OPTION instruction, the contents of the ACC Register will be transferred to the OPTION Register.

The OPTION Register is a 7-bit wide, write-only register which contains various control bits to configure the

Timer0/WDT pre-scaler, Timer0, and the external INT interrupt.

The OPTION Register are “write-only” and are set all “1”s except INTEDG bit.

PS2:PS0 : Prescaler rate select bits.

PS2:PS0	Timer0 Rate	WDT Rate
0 0 0	1:2	1:1
0 0 1	1:4	1:2
0 1 0	1:8	1:4
0 1 1	1:16	1:8
1 0 0	1:32	1:16
1 0 1	1:64	1:32
1 1 0	1:128	1:64
1 1 1	1:256	1:128

PSA : pre-scaler assign bit.

= 1, WDT (watch-dog timer).

= 0, TMR0 (Timer0).

T0SE : TMR0 source edge select bit.

= 1, Falling edge on T0CKI pin.

= 0, Rising edge on T0CKI pin.

T0CS : TMR0 clock source select bit.

= 1, External T0CKI pin. Pin IOB2/T0CKI is forced to be an input even if IOST IOB2 = “0”.

= 0, internal instruction clock cycle.

INTEDG : Interrupt edge select bit.

= 1, interrupt on rising edge of INT pin.

= 0, interrupt on falling edge of INT pin.

Bit7 : Not used.

6.1.17 IOSTB (Port I/O Control Register)

Address	Name	B7	B6	B5	B4	B3	B2	B1	B0
06h (w)	IOSTB	Port B I/O Control Register							

Accessed by IOST instruction.

The Port I/O Control Registers are loaded with the contents of the ACC Register by executing the IOST R (06h) instruction. A ‘1’ from a IOST Register bit puts the corresponding output driver in hi-impedance state (input mode). A ‘0’ enables the output buffer and puts the contents of the output data latch on the selected pins (output mode). The IOST Registers are “write-only” and are set (output drivers disabled) upon RESET.

6.2 I/O Port

Port B is bi-directional tristate I/O port. Port B is an 8-pin I/O port. Please note that IOB3 is an input only pin. All I/O pins have data direction control register (IOSTB) which

can configure these pins as output or input. The exceptions are IOB3 which is input only and IOB2 which may be controlled by the T0CS bit (OPTION<5>).

IOB<7:4> and IOB<2:0> have its corresponding pull-high control bits (PHCON register) to enable the weak internal pull-high. The weak pull-high is automatically turned off when the pin is configured as an output pin.

IOB<2:0> have its corresponding pull-down control bits (PDCON register) to enable the weak internal pull-down. The weak pull-down is automatically turned off when the pin is configured as an output pin.

IOB<7:4> and IOB<2:0> have its corresponding open-drain control bits (ODCON register) to enable the open-drain output when these pins are configured to be an output pin.

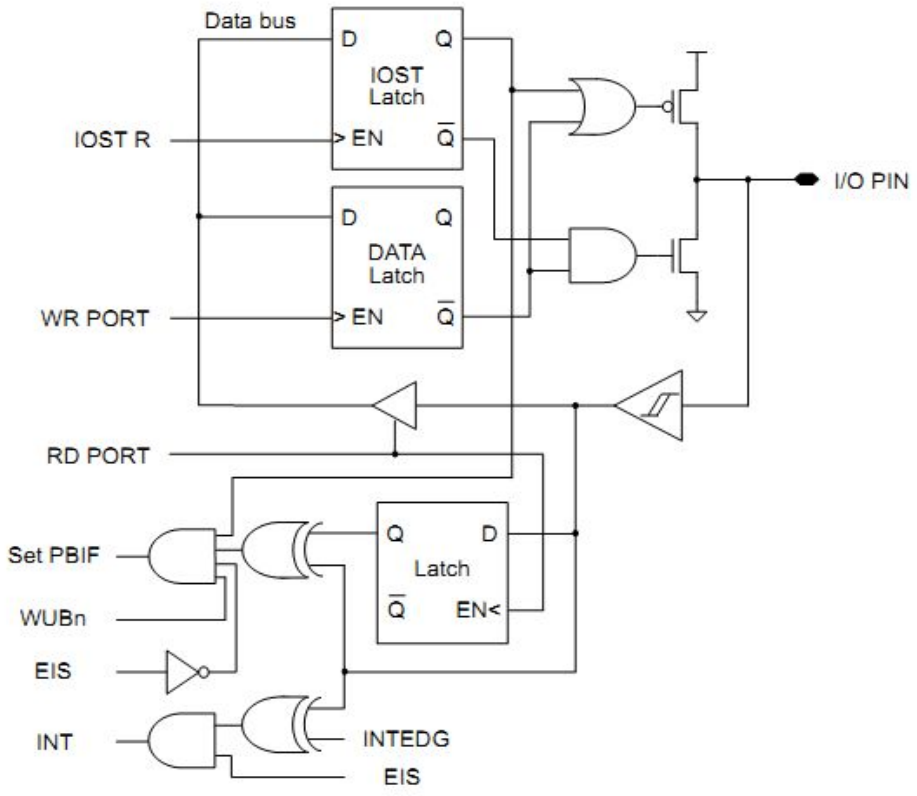
IOB<7:0> also provides the input change interrupt/wake-up function. Each pin has its corresponding input change interrupt/wake-up enable bits (WUCON) to select the input change interrupt/wake-up source.

The IOB0 is also an external interrupt input signal by setting the EIS bit (PCON<6>). In this case, IOB0 input change interrupt/wake-up function will be disabled by hardware even if it is enabled by software.

The CONFIGURATION words can set several I/Os to alternate functions. When acting as alternate functions the pins will read as “0” during port read.

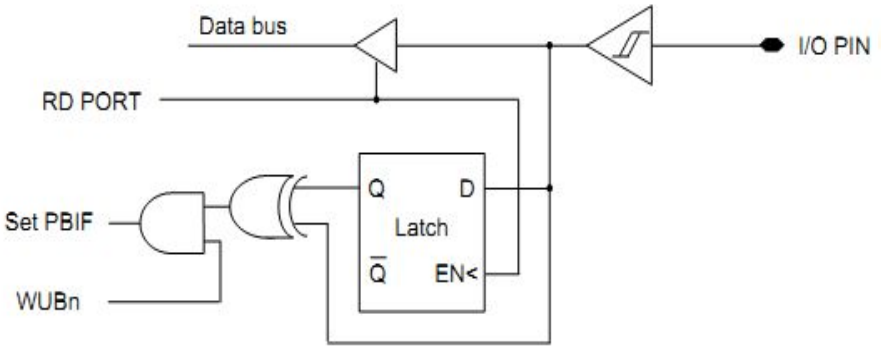
FIGURE 2.3: Block Diagram of I/O PIN s

IOB0/INT :

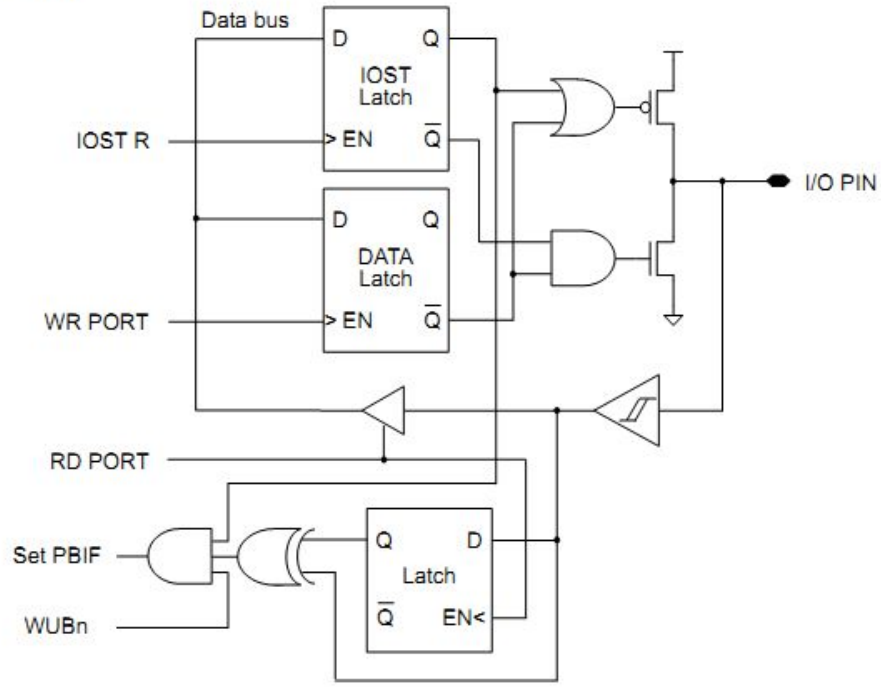


Pull-high/pull-down and open-drain are not shown in the figure

IOB3 :



IOB7 ~ IOB4, IOB2 ~ IOB1 :



Pull-high/pull-down and open-drain are not shown in the figure

6.3 Timer0/WDT & pre-scaler

6.3.1 Timer0

The Timer0 is a 8-bit timer/counter. The clock source of Timer0 can come from the

internal clock or by an external clock source (T0CKI pin).

6.3.1.1 Using Timer0 with an Internal Clock : Timer mode

Timer mode is selected by clearing the T0CS bit (OPTION<5>). In timer mode, the timer0 register (TMR0) will increment every instruction cycle (without pre-scaler). If TMR0 register is written, the increment is inhibited for the following two cycles.

6.3.1.2 Using Timer0 with an External Clock : Counter mode

Counter mode is selected by setting the T0CS bit (OPTON<5>). In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The incrementing edge is determined by the source edge select bit T0SE (OPTION<4>).

The external clock requirement is due to internal phase clock (To sc) synchronization. Also, there is a delay in the actual incrementing of Timer0 after synchronization.

When no pre-scaler is used, the external clock input is the same as the pre-scaler output. The synchronization of T0CKI with the internal phase clocks is accomplished by sampling the pre-scaler output on the T2 and T4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2 TOSC and low for at least 2 To sc.

When a pre-scaler is used, the external clock input is divided by the asynchronous pre-scaler. For the external clock to meet the sampling requirement, the ripple counter must be taken into account. Therefore, it is necessary for T0CKI to have a period of at least 4Tosc divided by the pre-scaler value.

6.3.2 Watchdog Timer (WDT)

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. So the WDT will still run even if the clock on the OSCI and OSCO pins is turned off, such as in SLEEP mode. During normal operation or in SLEEP mode, a WDT time-out will cause the device reset and the TO bit (STATUS<4>) will be cleared.

The WDT can be disabled by clearing the control bit WDTE (PCON<7>) to “0”.

The WDT has a nominal time-out period of 18 ms, 4.5ms, 288ms or 72ms selected by SUT<1:0> bits of configuration word (without pre-scaler). If a longer time-out period is desired, a pre-scaler with a division ratio of up to 1:128 can be assigned to the WDT controlled by the OPTION register. Thus, the longest time-out period is approximately 36.8 seconds.

The CLRWDT instruction clears the WDT and the pre-scaler, if assigned to the WDT, and prevents it from timing out

and generating a device reset.

The SLEEP instruction resets the WDT and the pre-scaler, if assigned to the WDT. This gives the maximum SLEEP time before a WDT Wake-up Reset.

6.3.3 pre-scaler

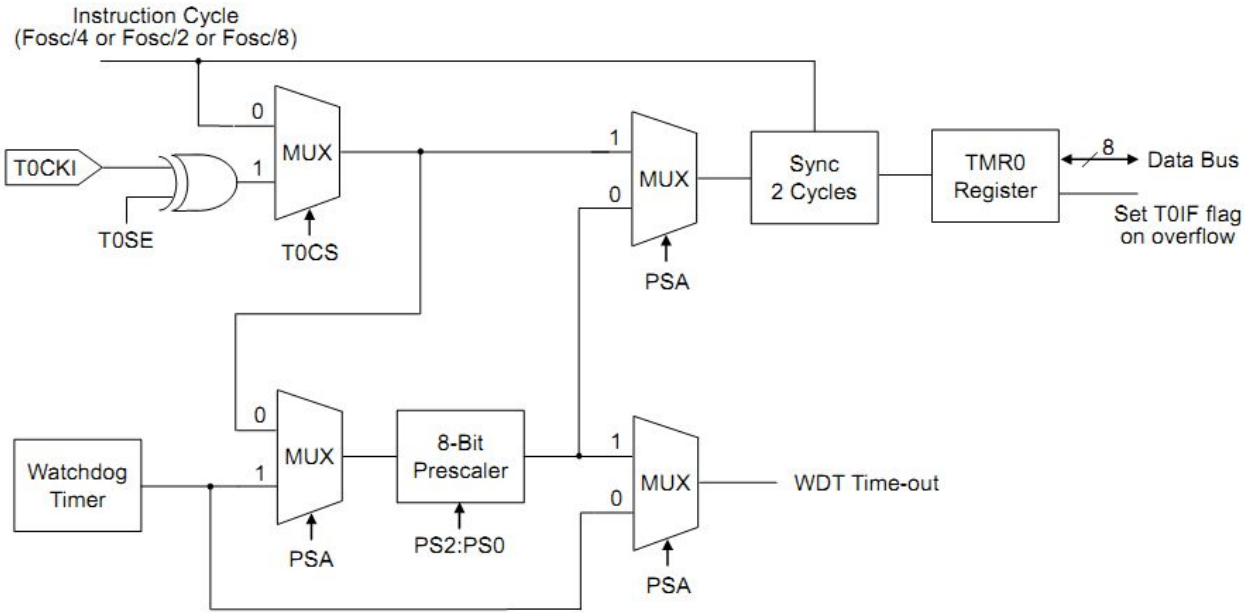
An 8-bit counter (down counter) is available as a pre-scaler for the Timer0, or as a post scaler for the Watchdog Timer (WDT). Note that the pre-scaler may be used by either the Timer0 module or the WDT, but not both. Thus, a pre-scaler assignment for the Timer0 means that there is no pre-scaler for the WDT, and vice-verse. The PSA bit (OPTION<3>) determines pre-scaler assignment. The PS<2:0> bits (OPTION<2:0>) determine pre-scaler ratio.

When the pre-scaler is assigned to the Timer0 module, all instructions writing to the TMR0 register will clear the pre-scaler. When it is assigned to WDT, a CLRWDT instruction will clear the pre-scaler along with the WDT.

The pre-scaler is neither readable nor writable. On a RESET, the pre-scaler contains all '1's.

To avoid an unintended device reset, CLRWDT or CLRR TMR0 instructions must be executed when changing the pre-scaler assignment from Timer0 to the WDT, and vice-verse.

FIGURE 2.4: Block Diagram of The Timer0/WDT pre-scaler



6.4 Interrupts

The BJ8P509F series has up to three sources of interrupt:

1. External interrupt INT pin.
2. TMR0 overflow interrupt.
3. Port B input change interrupt (pins IOB7:IOB0).

INTFLAG is the interrupt flag register that recodes the interrupt requests in the relative flags. A global interrupt enable bit, GIE (INTEN<7>), enables (if set) all un-masked interrupts or disables (if cleared) all interrupts. Individual interrupts can be enabled/disabled through their corresponding enable bits in INTEN register regardless of the status of the GIE bit.

When an interrupt event occur with the GIE bit and its corresponding interrupt enable bit are all set, the GIE bit will be cleared by hardware to disable any further interrupts, and the next instruction will be fetched from address 008h.

The interrupt flag bits must be cleared by software before re-enabling GIE bit to avoid recursive interrupts.

The RETFIE instruction exits the interrupt routine and set the GIE bit to re-enable interrupt.

The flag bit (except PBIF bit) in INTFLAG register is set by interrupt event regardless of the status of its mask bit.

Reading the INTFLAG register will be the logic AND of INTFLAG and INTEN.

When an interrupt is generated by the INT instruction, the next instruction will be fetched from address 002h.

6.4.1 External INT Interrupt

External interrupt on INT pin is rising or falling edge triggered selected by INTEDG (OPTION<6>). When a valid edge appears on the INT pin the flag bit INTIF (INTFLAG<2>) is set. This interrupt can be disabled by clearing INTIE bit (INTEN<2>).

The INT pin interrupt can wake-up the system from SLEEP condition, if bit INTIE was set before going to SLEEP. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

6.4.2 Timer0 Interrupt

An overflow (Ff h 00h) in the TMR0 register will set the flag bit T0IF (INTFLAG<0>). This interrupt can be disabled by clearing T0IE bit (INTEN<0>).

6.4.3 Port B Input Change Interrupt

An input change on IOB<7:0> set flag bit PBIF (INTFLAG<1>). This interrupt can be disabled by clearing PBIE bit (INTEN<1>).

Before the port B input change interrupt is enabled, reading PORTB (any instruction accessed to PORTB, including read/write instructions) is necessary. Any pin which corresponding WUB ON bit (WUCON<7:0>) is cleared to “0” or configured as output or IOB0 pin configured as INT pin will be excluded from this function.

The port B input change interrupt also can wake-up the system from SLEEP condition, if bit PBIE was set before going to SLEEP. And GIE bit also decides whether or not the processor branches to the interrupt vector following wake-up. If GIE bit was set, the program will execute interrupt service routine after wake-up; or if GIE bit was cleared, the program will execute next PC after wake-up.

6.5 Power-down Mode (SLEEP)

Power-down mode is entered by executing a SLEEP instruction.

When SLEEP instruction is executed, the PD bit (STATUS<3>) is cleared, the TO bit is set, the watchdog timer will

be cleared and keeps running, and the oscillator driver is turned off.

All I/O pins maintain the status they had before the SLEEP instruction was executed.

6.5.1 Wake-up from SLEEP Mode

The device can wake-up from SLEEP mode through one of the following events:

1. RSTB reset.
2. WDT time-out reset (if enabled).
3. Interrupt from RB0/INT pin, or PORTB change interrupt.

External RSTB reset and WDT time-out reset will cause a device reset. The PD and TO bits can be used to determine the cause of device reset. The PD bit is set on power-up and is cleared when SLEEP instruction is executed. The TO bit is cleared if a WDT time-out occurred. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set. Wake-up is regardless of the GIE bit. If GIE bit is cleared, the device will continue execution at the instruction after the SLEEP instruction. If the GIE bit is set, the device will branch to the interrupt address (008h). In HF or LF oscillation mode, the system wake-up delay time is 18/4.5/288/72ms (selected by SUT<1:0> bits of configuration word) plus 16 oscillator cycles time.

And in IRC/ERIC or ERC oscillation mode, the system wake-up delay time is 140us.

6.6 Reset

BJ8P509F devices may be RESET in one of the following ways:

1. Power-on Reset (POR)
2. Brown-out Reset (BOR)
3. RSTB Pin Reset
4. WDT time-out Reset

Some registers are not affected in any RESET condition. Their status is unknown on Power-on Reset and unchanged in any other RESET. Most other registers are reset to a “reset state” on Power-on Reset, RSTB or WDT Reset.

A Power-on RESET pulse is generated on-chip when V dd rise is detected. To use this feature, the user merely ties the RSTB pin to V dd.

On-chip Low Voltage Detector (LVD) places the device into reset when V dd is below a fixed voltage. This ensures that the device does not continue program execution outside the valid operation V dd range. Brown-out RESET is typically used in AC line or heavy loads switched applications.

A RSTB or WDT Wake-up from SLEEP also results in a device RESET, and not a continuation of operation before SLEEP.

The TO and PD bits (STATUS<4:3>) are set or cleared depending on the different reset conditions.

6.6.1 Power-up Reset Timer(PWRT)

The Power-up Reset Timer provides a nominal 18/4.5/288/72ms (selected by SUT<1:0> bits of configuration word) (or 140us, varies based on oscillator selection and reset condition) delay after Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset. The device is kept in reset state as long as the PWRT is active.

The PWDT delay will vary from device to device due to V dd, temperature, and process variation.

TABLE 2.1: PWRT Period

Oscillator Mode	Power-on Reset Brown-out Reset	RSTB Reset WDT time-out Reset
ERC & IRC/ERIC	18/4.5/288/72 ms	140 us
HF & LF	18/4.5/288/72 ms	18/4.5/288/72ms

6.6.2 Oscillator Start-up Timer(OST)

The OST timer provides a 16 oscillator cycle delay (from OSCI input) after the PWRT delay (18/4.5/288/72ms) is over in HF or LF oscillation mode. This delay ensures that the X'TAL oscillator or resonator has started and stabilized.

The device is kept in reset state as long as the OST is active.

This counter only starts incrementing after the amplitude of the OSCI signal reaches the oscillator input thresholds.

6.6.3 Reset Sequence

When Power-on Reset (POR), Brown-out Reset (BOR), RSTB Reset or WDT time-out Reset is detected, the reset

sequence is as follows:

1. The reset latch is set and the PWRT & OST are cleared.
2. When the internal POR, BOR, RSTB Reset or WDT time-out Reset pulse is finished, then the PWRT begins counting.
3. After the PWRT time-out, the OST is activated.
4. And after the OST delay is over, the reset latch will be cleared and thus end the on-chip reset signal.

In HF or LF oscillation mode, the totally system reset delay time is 18/4.5/288/72ms plus 16 oscillator cycle time. And in IRC/ERIC or ERC oscillation mode, the totally system reset delay time is 18/4.5/288/72ms after Power-on Reset (POR), Brown-out Reset (BOR), or 140us after RSTB Reset or WDT time-out Reset.

FIGURE 2.5: Simplified Block Diagram of on-chip Reset Circuit

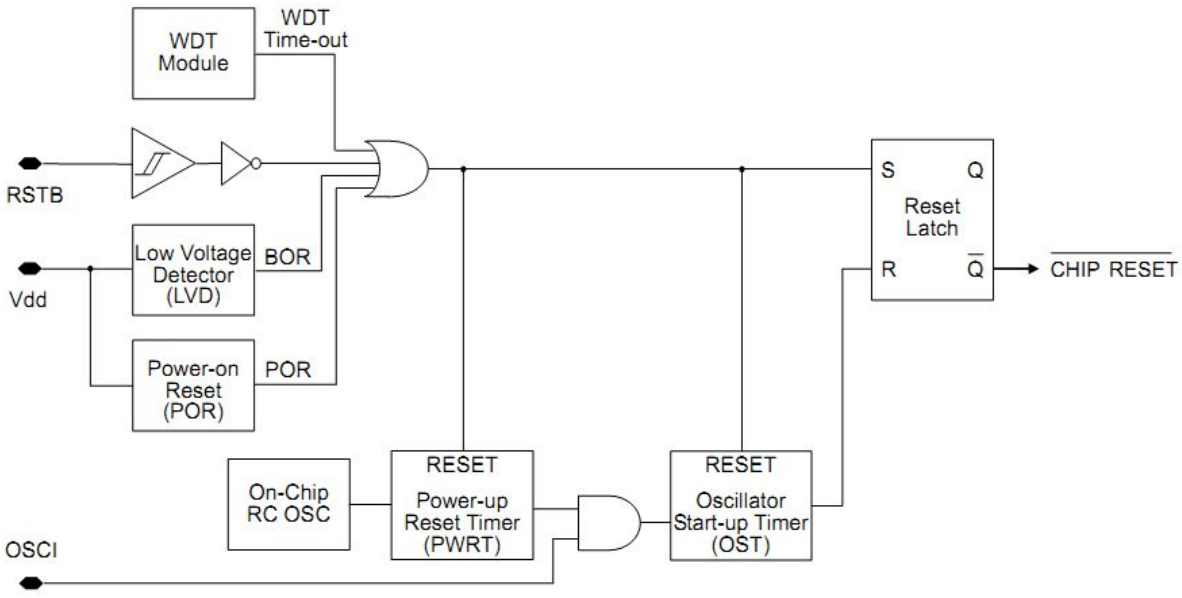


TABLE 2.2: Reset Conditions for All Registers

Register	Address	Power-on Reset Brown-out Reset	RSTB Reset WDT Reset
ACC	N/A	xxxx xxxx	uuuu uuuu
OPTION	N/A	-011 1111	-011 1111
IOSTB	06h	1111 1111	1111 1111
INDF	00h	xxxx xxxx	uuuu uuuu
TMR0	01h	xxxx xxxx	uuuu uuuu
PCL	02h	1111 1111	1111 1111
STATUS	03h	0001 1xxx	000# #uuu
FSR	04h	11xx xxxx	11uu uuuu
-	05h	Reserved	Reserved
PORTB	06h	xxxx xxxx	uuuu uuuu
General Purpose Register	07h	xxxx xxxx	uuuu uuuu
PCON	08h	101- ----	101- ----
WUCON	09h	0000 0000	0000 0000
PCHBUF	0Ah	---- --00	---- --00
PDCON	0Bh	1111 1111	1111 1111
ODCON	0Ch	0000 0000	0000 0000
PHCON	0Dh	1111 1111	1111 1111
INTEN	0Eh	0--- -000	0--- -000
INTFLAG	0Fh	---- -000	---- -000
General Purpose Registers	10 ~ 3Fh	xxxx xxxx	uuuu uuuu

TABLE 2.3: RST/$\overline{TO}$/$\overline{PD}$ Status after Reset or Wake-up

RST	$\overline{TO}$	$\overline{PD}$	RESET was caused by
0	1	1	Power-on Reset
0	1	1	Brown-out reset
0	u	u	RSTB Reset during normal operation
0	1	0	RSTB Reset during SLEEP
0	0	1	WDT Reset during normal operation
0	0	0	WDT Wake-up during SLEEP
1	1	0	Wake-up on pin change during SLEEP

Legend: u = unchanged

TABLE 2.4: Events Affecting $\overline{TO}$/$\overline{PD}$ Status Bits

Event	$\overline{TO}$	$\overline{PD}$
Power-on	1	1
WDT Time-Out	0	u
SLEEP instruction	1	0
CLRWDT instruction	1	1

Legend: u = unchanged

6.7 Hexadecimal Convert to Decimal (HCD)

Decimal format is another number format for BJ8P509F. When the content of the data memory has been assigned as decimal format, it is necessary to convert the results to decimal format after the execution of ALU instructions. When the decimal converting operation is processing, all of the operand data (including the contents of the data memory (RAM), accumulator (ACC), immediate data, and look-up table) should be in the decimal format, or the results of conversion will be incorrect.

Instruction DAA can convert the ACC data from hexadecimal to decimal format after any addition operation and restored to ACC.

The conversion operation is illustrated in example 2.2.

EXAMPLE 2.2: DAA CONVERSION

```
        MOVIA    90h    ; Set immediate data = decimal format number “90” (ACC 90h)
        MOVAR    30h    ;Load immediate data “90” to data memory address 30H
        MOVIA    10h    ;Set immediate data = decimal format number “10” (ACC 10h)
        ADDAR 30h, 0 ;Contents of the data memory address 30H and ACC are binary-added
                       ;the result loads to the ACC (ACC  A0h, C  0)
        DAA            ;Convert the content of ACC to decimal format, and restored to ACC
                       ;The result in the ACC is “00” and the carry bit C is “1”. This represents the
                       ;decimal number “100”
```

Instruction DAS can convert the ACC data from hexadecimal to decimal format after any subtraction operation and restored to ACC.

The conversion operation is illustrated in example 2.3.

EXAMPLE 2.3: DAS CONVERSION

```
      MOVIA  10h    ;Set immediate data = decimal format number “10” (ACC  10h)
      MOVAR  30h     ;Load immediate data “10” to data memory address 30H
      MOVIA  20h    ;Set immediate data = decimal format number “20” (ACC  20h)
        SUBAR 30h,0 ;Contents of the data memory address 30H and ACC are binary-subtracted
                     ;the result loads to the ACC (ACC  F0h, C  0)
      DAS            ;Convert the content of ACC to decimal format, and restored to ACC
                     ;The result in the ACC is “90” and the carry bit C is “0”. This represents the
                     ;decimal number “ -10”
```

6.8 Oscillator Configurations

BJ8P509F can be operated in six different oscillator modes. Users can program three configuration bits (Fo sc<2:0>)

to select the appropriate modes:

- ERC: External Resistor/Capacitor Oscillator
- HF: High Frequency Crystal/Resonator Oscillator
- XT: Crystal/Resonator Oscillator
- LF: Low Frequency Crystal Oscillator
- IRC: Internal Resistor/Capacitor Oscillator
- ERIC: External Resistor/Internal Capacitor Oscillator

In LF, XT, or HF modes, a crystal or ceramic resonator in connected to the OSCI and OSCO pins to establish oscillation. When in LF, XT, or HF modes, the devices can have an external clock source drive the OSCI pin. The ERC device option offers additional cost savings for timing insensitive applications. The RC oscillator frequency is a function of the resistor (Rex t) and capacitor (C ext), the operating temperature, and the process parameter.

The IRC/ERIC device option offers largest cost savings for timing insensitive applications. These devices offer 4 different internal RC oscillator frequency, 8MHz, 4MHz, 1MHz, and 455KHz, which is selected by two configuration bits (RCM<1:0>). Or user can change the oscillator frequency with external resistor. The ERIC oscillator frequency is a function of the resistor (Rex t), the operating temperature, and the process parameter.

FIGURE 2.6: HF, or LF Oscillator Modes (Crystal Operation or Ceramic Resonator)

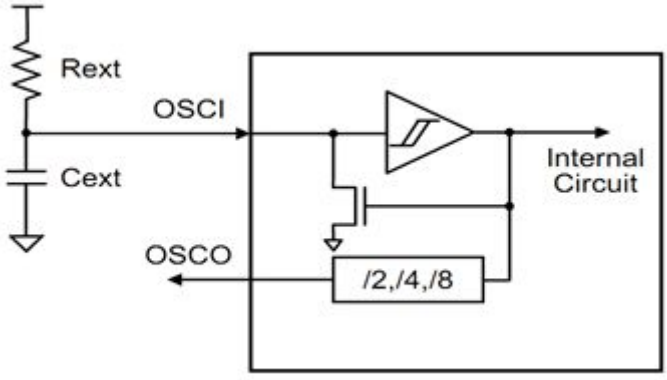


FIGURE 2.7: HF, or LF Oscillator Modes (External Clock Input Operation)

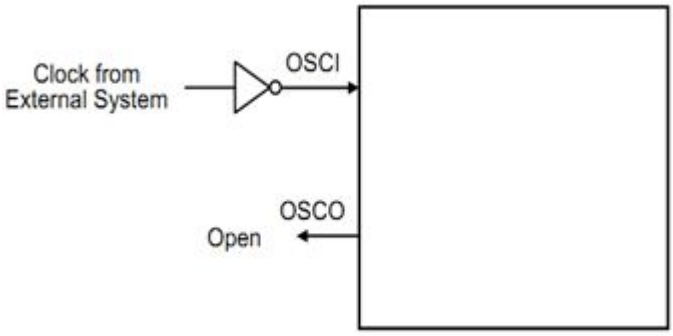


FIGURE 2.8: ERC Oscillator Mode (External RC Oscillator)

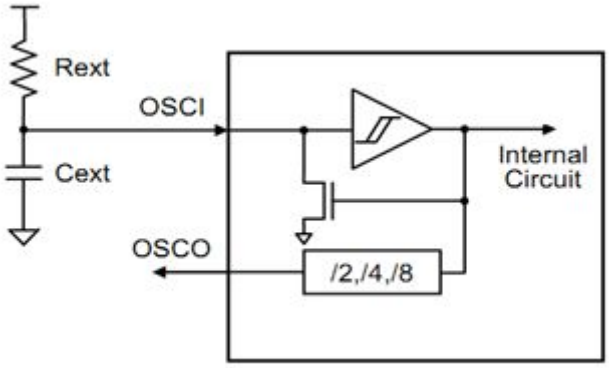


FIGURE 2.9: ERIC Oscillator Mode (External R, Internal C Oscillator)

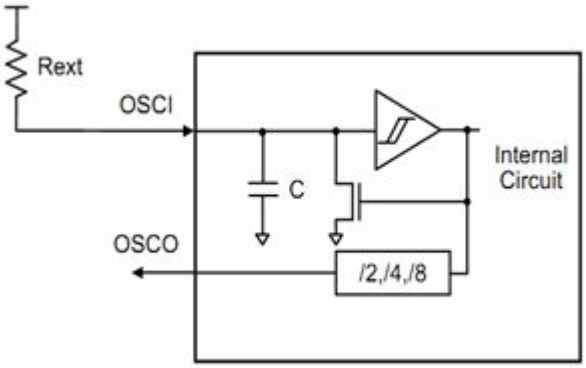
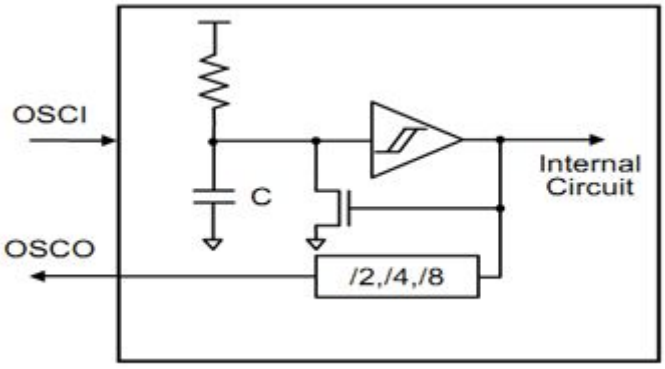


FIGURE 2.10: IRC Oscillator Mode (Internal R, Internal C Oscillator)



6.9 Configurations Word

TABLE 2.4: Configurations Word

Name	Description
Fosc<2:0>	Oscillator Selection Bits = 1, 1, 1 → ERC mode (external R & C) (default) OSCI pin is selected for IOB5/OSCI pin IOB4/OSCO pin is controlled by OSCOUT configuration bit = 1, 1, 0 → HF mode = 1, 0, 1 → XT mode = 1, 0, 0 → LF mode = 0, 1, 1 → IRC mode (internal R & C) IOB5 pin is selected for IOB5/OSCI pin IOB4/OSCO pin controlled by OSCOUT configuration bit = 0, 1, 0 → ERIC mode (external R & internal C) OSCI pin is selected for IOB5/OSCI pin IOB4/OSCO pin controlled by OSCOUT configuration bit
LVDT<2:0>	Low Voltage Detector Selection Bit = 1, 1, 1 → disable (default) = 1, 1, 0 → enable, LVDT voltage = 2.0V, controlled by SLEEP = 1, 0, 1 → enable, LVDT voltage = 2.0V = 1, 0, 0 → enable, LVDT voltage = 3.6V = 0, 1, 1 → enable, LVDT voltage = 1.8V = 0, 1, 0 → enable, LVDT voltage = 2.2V = 0, 0, 1 → enable, LVDT voltage = 2.4V = 0, 0, 0 → enable, LVDT voltage = 2.6V
RCM<1:0>	IRC Mode Selection Bits = 1, 1 → 4MHz (default) = 1, 0 → 8MHz = 0, 1 → 1MHz = 0, 0 → 455KHz
SUT<2:0>	PWRT & WDT Time Period Selection Bits (The value must be a multiple of prescaler rate) = 1, 1, 1 → PWRT = WDT prescaler rate = 18ms (default) = 1, 1, 0 → PWRT = WDT prescaler rate = 4.5ms = 1, 0, 1 → PWRT = WDT prescaler rate = 288ms = 1, 0, 0 → PWRT = WDT prescaler rate = 72ms = 0, 1, 1 → PWRT = 140us, WDT prescaler rate = 18ms = 0, 1, 0 → PWRT = 140us, WDT prescaler rate = 4.5ms = 0, 0, 1 → PWRT = 140us, WDT prescaler rate = 288ms = 0, 0, 0 → PWRT = 140us, WDT prescaler rate = 72ms
OSCOUT	IOB4/OSCO Pin Selection Bit for IRC/ERIC/ERC Mode = 1, OSCO pin is selected (default) = 0, IOB4 pin is selected
RSTBIN	IOB3/RSTB Pin Selection Bit = 1, IOB3 pin is selected (default) = 0, RSTB pin is selected
WDTEN	Watchdog Timer Enable Bit = 1, WDT enabled (default) = 0, WDT disabled
PROTECT	Code Protection Bit = 1 → EPROM code protection off (default) = 0 → EPROM code protection on

Name	Description
OSCD<1:0>	Instruction Period Selection Bits = 1, 1 → four oscillator periods (default) = 1, 0 → two oscillator periods = 0, 0 → eight oscillator periods
PMOD	Power Mode Selection Bit = 1, Non-power saving (default) = 0, Power saving
RDPORT	Read Port Control Bit for Output Pins = 1, From registers (default) = 0, From pins
SCHMITT	I/O Pin Input Buffer Control Bit = 1, With Schmitt-trigger (default) = 0, Without Schmitt-trigger
CAL<6:0>	Calibration Selection Bits for IRC Mode

TABLE 2.5: Selection of IOB5/OSCI and IOB4/OSCO Pins

Mode of oscillation	IOB5/OSCI	IOB4/OSCO
IRC	IOB5	IOB4/OSCO selected by OSCOUT bit
ERC, ERIC	OSCI	IOB4/OSCO selected by OSCOUT bit
HF, XT, LF	OSCI	OSCO

7. Absolute maximum

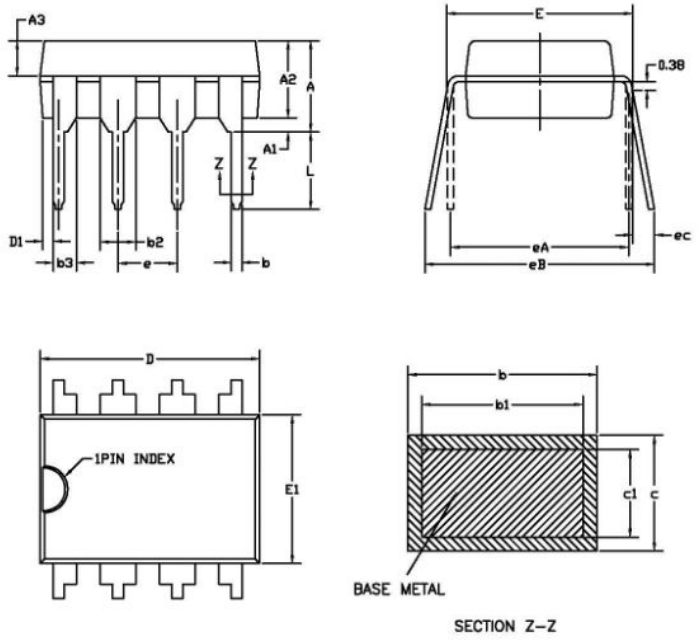
Ambient Operating Temperature	0℃ to +70℃
Store Temperature	-65℃ to +150℃
DC Supply Voltage (VDD)	0V to +6.0V
Input Voltage with respect to Ground (VSS)	-0.3V to (VDD + 0.3)V

8. Operating conditions

DC Supply Voltage	+2.3V to +5.5V
Operating Temperature	0℃ to +70℃

9. Package Dimension

9.1 **8-PIN DIP**

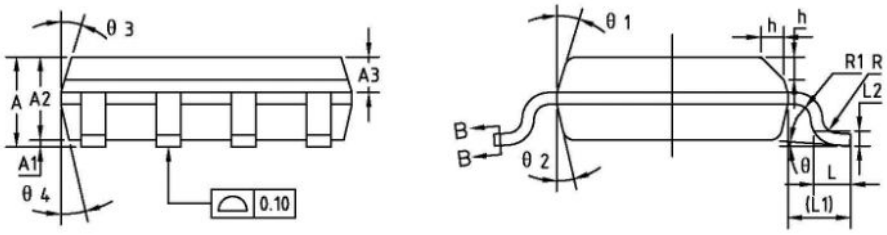


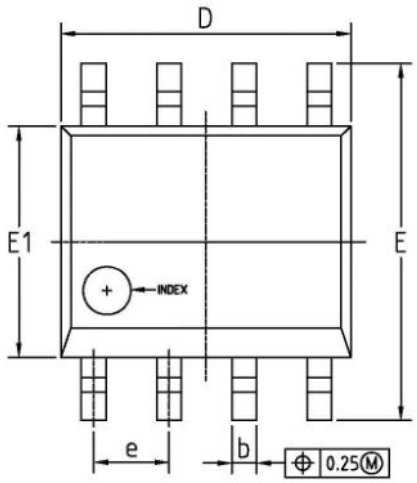
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

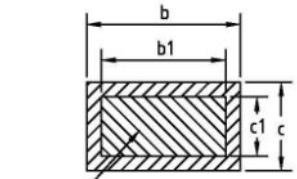
SYMBOL	MIN	NOM	MAX
A	–	–	4.80
A1	0.50	–	–
A2	3.10	3.30	3.50
A3	1.40	1.50	1.60
b	0.38	–	0.55
b1	0.38	0.46	0.51
b2	1.47	1.52	1.57
b3	0.89	0.99	1.09
c	0.21	–	0.35
c1	0.20	0.25	0.30
D	9.10	9.20	9.30
D1	0.13	–	–
E	7.62	7.87	8.25
E1	6.25	6.35	6.45
e		2.54BSC	
eA		7.62BSC	
eB	7.62	8.80	10.90
ec	0	–	1.52
L	2.92	3.30	3.81

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-001 BA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

9.2 8-PIN SOP







BASE METAL

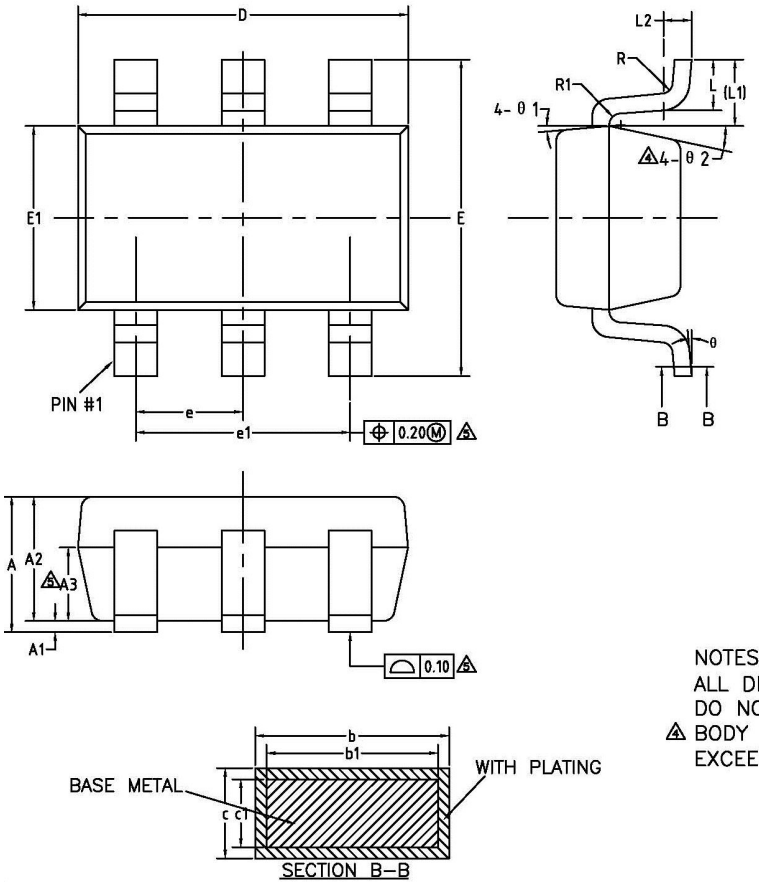
SECTION B–B

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
A3	0.50	0.60	0.70
b	0.38	–	0.51
b1	0.37	0.42	0.47
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ 1	15°	17°	19°
θ 2	11°	13°	15°
θ 3	15°	17°	19°
θ 4	11°	13°	15°

NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS–012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

9.3 6-PIN SOT23

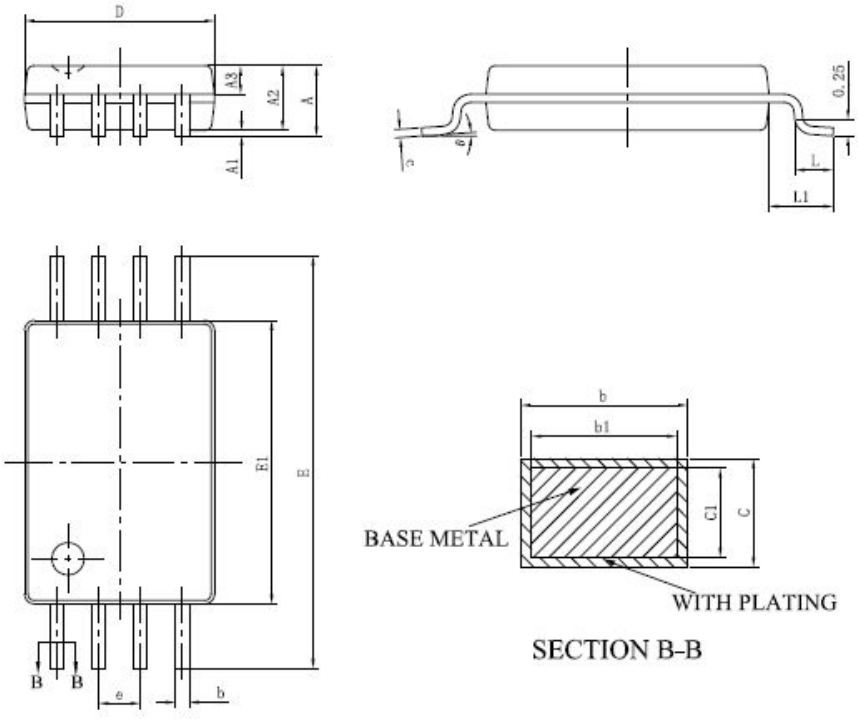


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

	SYMBOL	MIN	NOM	MAX
	A	–	–	1.25
	A1	0	–	0.15
	A2	1.00	1.10	1.20
	A3	0.60	0.65	0.70
	b	0.36	–	0.50
	b1	0.36	0.38	0.45
	c	0.14	–	0.20
	c1	0.14	0.15	0.16
	D	2.826	2.926	3.026
	E	2.60	2.80	3.00
	E1	1.526	1.626	1.726
④	e	0.90	0.95	1.00
④	e1	1.80	1.90	2.00
	L	0.35	0.45	0.60
	L1	0.59REF		
	L2	0.25BSC		
⑤	R	0.10	–	–
⑤	R1	0.10	–	0.20
	θ	0°	–	8°
	θ 1	3°	5°	7°
④	θ 2	6°	–	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–178 AB
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
④ BODY LENGTH INCLUDING MOLD PRUTRUSIONS SHALL NOT EXCEED 3.1mm.

9.4 8-PIN TSSOP8



SYMBOL	MILLIMETER	
	MIN	MAX
A	—	1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.39	0.49
b	0.21	0.30
b1	0.20	0.25
c	0.13	0.19
c1	0.12	0.14
D	2.90	3.10
E1	4.30	4.50
E	6.20	6.60
e	0.65BSC	
L	0.45	0.75
L1	1.00BSC	
θ	0	8°

10.Edition statement

Edition	Date	Content
VER 1.0	Jul ,2015	First Edition