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BJ8P64N

8-Bit Microcontroller with OTP ROM

Product Specification

VER 1.0

March 12, 2010

1 General Description

The BJ8P64N is an 8-bit microprocessor designed and developed with low-power and high-speed CMOS technology. The device has an on-chip 2K*14-bit Electrical One Time Programmable Read Only Memory (OTP-ROM). It provides a protection bit to prevent intrusion of user's code. Three Code option words are also available to meet user's requirements.

With its enhanced OTP-ROM feature, the BJ8P64N provides a convenient way of developing and verifying user's programs. Moreover, this OTP device offers the advantages of easy and effective program updates, using development and programming tools. User can avail of the BJX Writer to easily program his development code.

2 Features

- CPU configuration
  - 2K*14 bits on-chip ROM
  - 80*8 bits on-chip registers (SRAM)
  - 8-level stacks for subroutine nesting
  - Less than 1.9 mA at 5V/4MHz
  - Typically 15uA, at 3V/32kHz
  - Typically 1 uA, during Sleep mode
- I/O port configuration
  - 3 bidirectional I/O ports : P5, P6, P7
  - 17 I/O pins
  - Wake-up port : P5
  - 8 Programmable pull-down I/O pins
  - 8 programmable pull-high I/O pins
  - 8 programmable open-drain I/O pins
  - External interrupt : P60
- Operating voltage range
  - Operating voltage:2.5V~5.5V
- Operating temperature range
  - Operating temperature: -40℃ ~85℃
- Operating frequency range
  - Crystal mode: DC~20MHz/2clks@5V,DC~100ns inst. cycle@5V DC~8MHz/2clks @ 3V, DC~250ns inst. cycle @ 3V
  - ERC mode: DC~16MHz/2clks @ 5V, DC~125ns inst. cycle @ 5V DC~8MHz/2clks @ 3V, DC~250ns inst. cycle @ 3V
  - IRC mode: Oscillation mode : 4MHz, 8MHz, 1MHz, 455kHz
- Peripheral configuration
  - 8-bit real time clock/counter (TCC) with selective signal sources, trigger edges, and overflow interrupt
  - 8-bit real time clock/counter (TCCA, TCCC) and 16-bit real time clock/counter (TCCB) with selective signal sources, trigger edges, and overflow interrupt
  - 4-bit channel Analog-to-Digital Converter with 12-bit resolution in Vref mode
  - Easily implemented IR (Infrared remote control) application circuit
  - One pair of comparators or OP
- Six available interrupts:
  - TCC, TCCA, TCCB, TCCC overflow interrupt
  - Input-port status changed interrupt (wake-up from sleep mode)
  - External interrupt
  - ADC completion interrupt
  - Comparators status change interrupt
  - IR/PWM interrupt
- Special features
  - Programmable free running watchdog timer(4.5ms : 18ms)
  - Power saving Sleep mode
  - Selectable Oscillation mode
  - Power-on voltage detector (2.0V +/- 0.1V)
- Package type:
  - 14-pin DIP 300mil : BJ8P64N-14D
  - 14-pin SOP 150mil : BJ8P64N-14M
  - 16-pin DIP 300mil BJ8P64N-16D
  - 16-pin SOP 150mil : BJ8P64N-16M
  - 18-pin DIP 300mil : BJ8P64N-18D
  - 18-pin SOP 300mil : BJ8P64N-18M
  - 20-pin DIP 300mil : BJ8P64N-20D
  - 20-pin SOP 300mil : BJ8P64N-20M

3 Pin Assignment

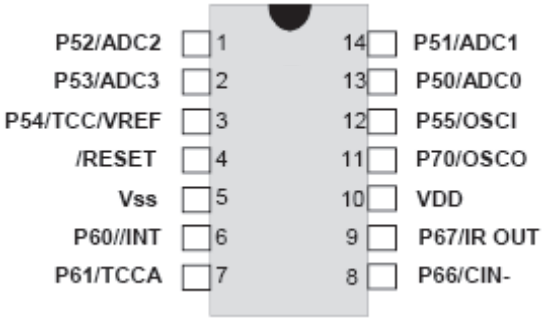

Fig 3-1 BJ8P64N-14D/14M

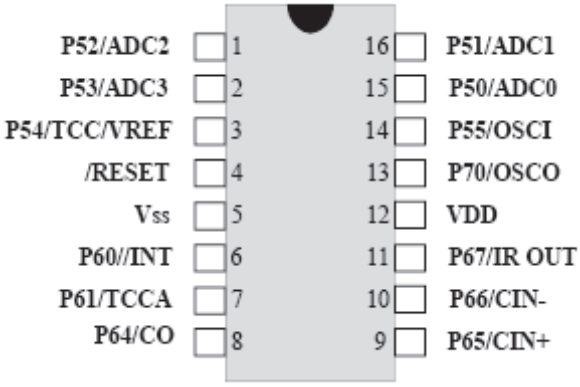

Fig 3-2 BJ8P64-16D/16M

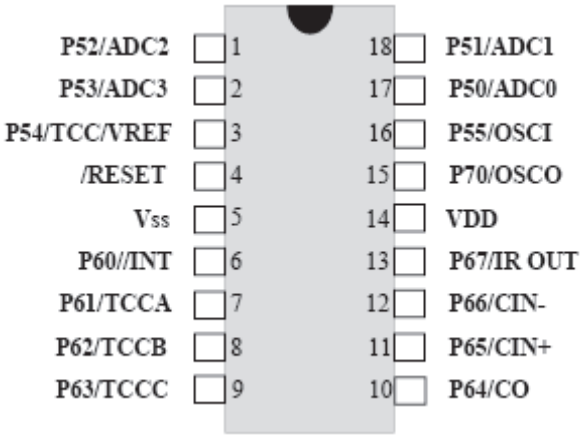

Fig 3-3 BJ8P64-18D/18M

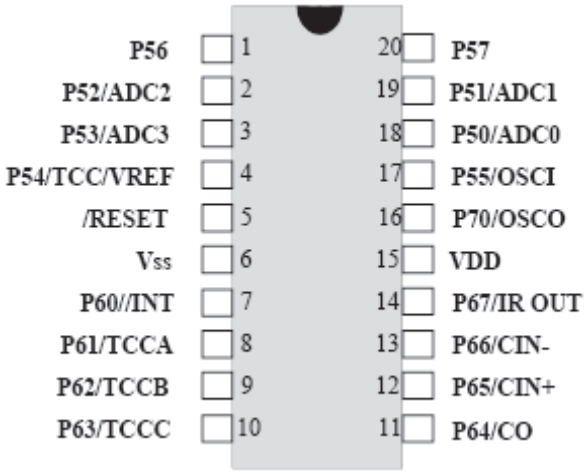

Fig 3-4 BJ8P64N-20D/20M

4 Pin Description

4.1 BJ8P64N-14D/14M

Symbol	Pin No.	Type	Function
P70	11	I/O	General purpose input/output pin Default value after a power-on reset
P60, P61 P66, P67	6~9	I/O	General purpose input/output pin Open-drain Function Default value after a power-on reset
P50~P55	1~3 12~14	I/O	General purpose input/output pin Pull-high/Pull-down Function Default value after a power-on reset Wake up from sleep mode when the status of the pin changes
OSCI	12	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	11	I/O	Crystal type: Crystal input terminal or external clock input pin. RC type: clock output with a duration of one instruction cycle External clock signal input
/RESET	4	I	If set as /RESET and remains at logic low, the device will be reset Voltage on /RESET/Vpp must not exceed Vdd during normal mode
TCC, TCCA	3, 7	I	External Counter input TCC is defined by CONT <5> TCCA is defined by IOC80 <1>
ADC0~ ADC3	1, 2, 13, 14	I	Analog to Digital Converter Defined by ADCON (R9) <1:0>
IR OUT	9	O	IR mode output pin, capable of driving and sinking current=20mA when the output voltage drops to 0.7Vdd and rise to0.3Vdd at Vdd=5V.
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/INT	6	I	External interrupt pin triggered by a falling or rising edge Defined by CONT <7>
VDD	10	–	Power supply
VSS	5	–	Ground

4.2 BJ8P64-16D/16M

Symbol	Pin No.	Type	Function
P70	13	I/O	General purpose input/output pin Default value after a power-on reset
P60~P61, P64~P67	6~11	I/O	General purpose input/output pin Open-drain Function Default value after a power-on reset
P50~P55	1~3 14~16	I/O	General purpose input/output pin Pull-high/Pull-down Function Default value after a power-on reset Wake up from sleep mode when the status of the pin changes
CIN-, CIN+ CO	10, 9 8	I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
OSCI	14	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	13	I/O	Crystal type: Crystal input terminal or external clock input pin. RC type: clock output with a duration of one instruction cycle External clock signal input
/RESET	4	I	If set as /RESET and remains at logic low, the device will be reset Voltage on /RESET/Vpp must not exceed Vdd during normal mode
TCC, TCCA	3, 7	I	External Counter input TCC is defined by CONT <5> TCCA is defined by IOC80 <1>
ADC0~ ADC3	1, 2, 15, 16	I	Analog to Digital Converter Defined by ADCON (R9) <1:0>
IR OUT	11	O	IR mode output pin, capable of driving and sinking current=20mA when the output voltage drops to 0.7Vdd and rise to0.3Vdd at Vdd=5V.
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/INT	6	I	External interrupt pin triggered by a falling or rising edge Defined by CONT <7>
VDD	12	–	Power supply
VSS	5	–	Ground

4.3 BJ8P64N-18D/18M

Symbol	Pin No.	Type	Function
P70	15	I/O	General purpose input/output pin Default value after a power-on reset
P60~P67	6~13	I/O	General purpose input/output pin Open-drain Function Default value after a power-on reset
P50~P55	1~3 16~18	I/O	General purpose input/output pin Pull-high/Pull-down Function Default value after a power-on reset Wake up from sleep mode when the status of the pin changes
CIN-, CIN+ CO	12, 11 10	I/O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
OSCI	16	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	15	I/O	Crystal type: Crystal input terminal or external clock input pin. RC type: clock output with a duration of one instruction cycle External clock signal input
/RESET	4	I	If set as /RESET and remains at logic low, the device will be reset Voltage on /RESET/Vpp must not exceed Vdd during normal mode
TCC, TCCA, TCCB, TCCC	3, 7, 8, 9	I	External Counter input TCC is defined by CONT <5> TCCA is defined by IOC80 <1> TCCB is defined by IOC90 <5> TCCC is defined by IOC90 <1>
ADC0~ ADC3	1, 2, 17, 18	I	Analog to Digital Converter Defined by ADCON (R9) <1:0>
IR OUT	13	O	IR mode output pin, capable of driving and sinking current=20mA when the output voltage drops to 0.7Vdd and rise to0.3Vdd at Vdd=5V.
VREF	3	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/INT	6	I	External interrupt pin triggered by a falling or rising edge Defined by CONT <7>
VDD	14	–	Power supply
VSS	5	–	Ground

4.4 BJ8P64N-20D/20M

Symbol	Pin No.	Type	Function
P70	16	I/O	General purpose input/output pin Default value after a power-on reset
P60~P67	7~14	I/O	General purpose input/output pin Open-drain Function Default value after a power-on reset
P50~P57	1~4 17~20	I/O	General purpose input/output pin Pull-high/Pull-down Function Default value after a power-on reset Wake up from sleep mode when the status of the pin changes
CIN-, CIN+ CO	13, 12 11	I O	"-" : the input pin of Vin- of the comparator "+" : the input pin of Vin+ of the comparator Pin CO is the comparator output Defined by IOC80 <4:3>
OSCI	17	I	Crystal type: Crystal input terminal or external clock input pin RC type: RC oscillator input pin
OSCO	16	I/O	Crystal type: Crystal input terminal or external clock input pin. RC type: clock output with a duration of one instruction cycle External clock signal input
/RESET	5	I	If set as /RESET and remains at logic low, the device will be reset Voltage on /RESET/Vpp must not exceed Vdd during normal mode
TCC, TCCA, TCCB, TCCC	4, 8, 9, 10	I	External Timer/Counter input TCC is defined by CONT <5> TCCA is defined by IOC80 <1> TCCB is defined by IOC90 <5> TCCC is defined by IOC90 <1>
ADC0~ ADC3	2, 3, 18, 19	I	Analog to Digital Converter Defined by ADCON (R9) <1:0>
IR OUT	14	O	IR mode output pin, capable of driving and sinking current=20mA when the output voltage drops to 0.7Vdd and rise to 0.3Vdd at Vdd=5V.
VREF	4	I	External reference voltage for ADC Defined by ADCON (R9) <7>
/INT	7	I	External interrupt pin triggered by a falling or rising edge Defined by CONT <7>
VDD	15	–	Power supply
VSS	6	–	Ground