BK3260N Bluetooth Audio SoC Datasheet

Version 0.1

Beken Corporation
41，1387 Zhangdong Rd, Shanghai 201203, China
PHONE: (86)21 5108 6811
FAX: (86)21 6087 1089

Revision History

Rev.	Date	Remark
0.3	13/JUL/2016	Draft Version

Contents

1. General Description

The BK3260N is a low power, highly integrated Bluetooth system on chip (SoC) audio device. It integrates a high performance Bluetooth RF transceiver, feature rich baseband processor, FLASH memory controller, multiple analog and digital peripherals, and a Bluetooth software stack including the audio, video, and hands free profiles.

The cache based architecture enables full programmability with an SIP 8M FLASH memory device and can be used for both control and multimedia hybrid applications. The internal dual stereo ADC converts stereo analog input to digital signals that can be processed with a digital equalizer. Hardware realizations of the equalizer offload the MCU making the chip ideal for low power headset applications.

The device incorporates on-chip power management with linear and switch-mode buck regulators and also includes a 220 mA internal battery charge controller to further reduce external bill of material (BOM) costs.

1.1. Features

- Operation voltage from 2.8 V to 4.2 V
- -92 dBm sensitivity for 2 Mbps mode
- Bluetooth 4.0 classic and low energy
- A2DP v1.2, AVRCP v1.0 and HFP v1.5
- Scatter net and true wireless stereo
- Full duplex hands-free speakerphone
- 96 dB SNR stereo ADC and DAC
- Stereo line in and dual microphone
- Five bands digital hardware equalizer
- SPI, UART, I2C, SDIO and USB
- FM receiver interface
- Interface for external PA and LNA
- Up to 220 mA battery charge controller

1.2. Applications

- Bluetooth stereo speaker
- Bluetooth stereo headset
- Bluetooth control and multimedia hybrid

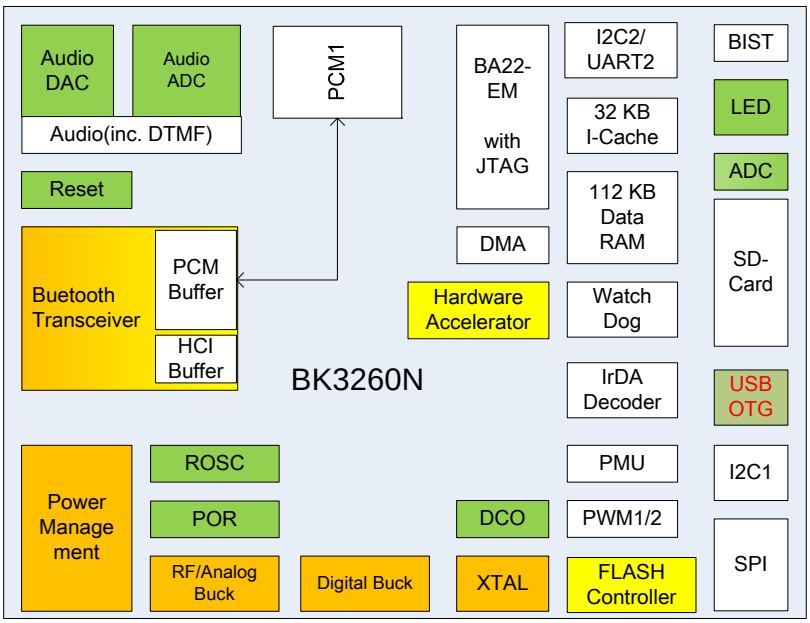


Figure 1. Block diagram of BK3260N Bluetooth Audio SoC

2. Pin Definition

The BK3260N is available in both a 48-pin 6x6 mm^2 QFN package and 40-pin 5x5 mm^2 QFN package.

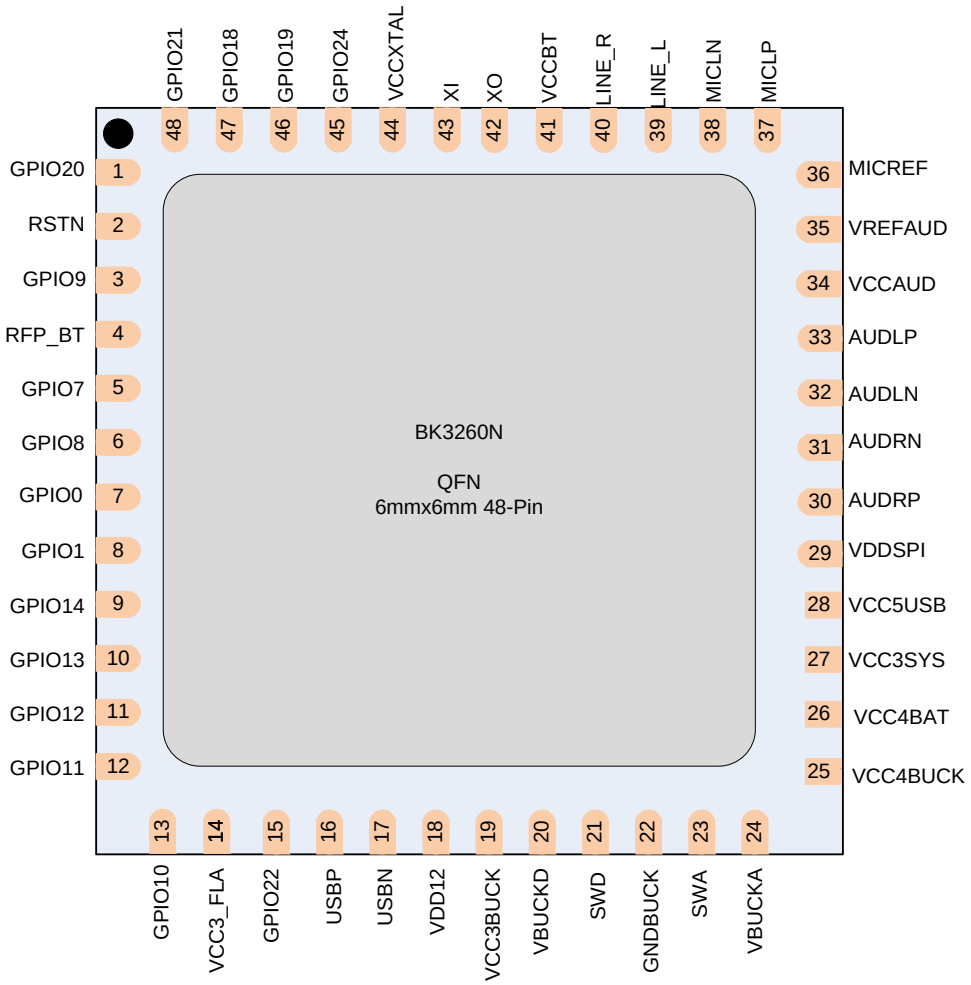


Figure 2. 48-Pin QFN 6mm x 6mm pin diagram

Table 1 Pin Description of 48-Pin Package

PIN	Name	Description
1	TDI/GPIO20	JTAG TDI / GPIO20
2	RSTN	reset
3	GPIO9	GPIO9/SPI MISO
4	RFP_BT	RF port
5	GPIO7	GPIO7 / SPI SCK
6	GPIO8	GPIO8 / SPI MOSI
7	GPIO0	GPIO0 / UART2 TXD
8	GPIO1	GPIO1 / UART2 RXD

9	GPIO14	GPIO14 / SD card data 0
10	GPIO13	GPIO13 / SD card command
11	GPIO12	GPIO12 / SD card clock
12	GPIO11	GPIO11 / PWM 1
13	GPIO10	GPIO10 / PWM 0
14	VCC3_FLA	LDO Output. Power supply to FLASH，local 1uF decoupling Cap
15	GPIO22	GPIO22/ IRDA Input
16	USBP	USBP
17	USBN	USBN
18	VDD12	Power Input for Digital. Connected to Digital BUCK Output(Pin 20)
19	VCC3BUCK	Buck 3V power supply Input. Connected to VCC3SYS(Pin 27)
20	VBUCKD	Switch Regulator Output for Digital
21	SWD	Buck component
22	GNDBUCK	BUCK Ground
23	SWA	Buck component
24	VBUCKA	Switch Regulator Output for Analog
25	VCC4BUCK	VBAT Power Input
26	VCC4BAT	Battery input
27	VCC3SYS	LDO Output, IO voltage; local 4.7uF decoupling cap
28	VCC5USB	USB charge input
29	VDDSPI	LDO Output, SPI power, local 100nF decoupling cap, Normally NC
30	AUDIORP	Audio right channel output positive
31	AUDIORN	Audio right channel output negative
32	AUDIOLN	Audio left channel output negative
33	AUDIOLP	Audio left channel output positive
34	VCCAUD	Audio power supply Input, Connected to Analog BUCK Output
35	VREF1AUD	Audio reference
36	V2MICBIAS	LDO Output for Microphone bias
37	MICIP	Microphone input positive
38	MICIN	Microphone input negative
39	LINE_L	Line input, Left channel
40	LINE_R	Line input, right channel
41	VCCBT	BT power supply input, Connected to Analog BUCK Output
42	XO	XTAL output
43	XI	XTAL input
44	VCC3XTAL	XTAL power
45	GPIO24	GPIO24/SPI_CLK
46	TMS/GPIO19	JTAG TMS / GPIO19
47	TCK/GPIO18	JTAG TCK / GPIO18
48	TDO/GPIO21	JTAG TDO / GPIO21

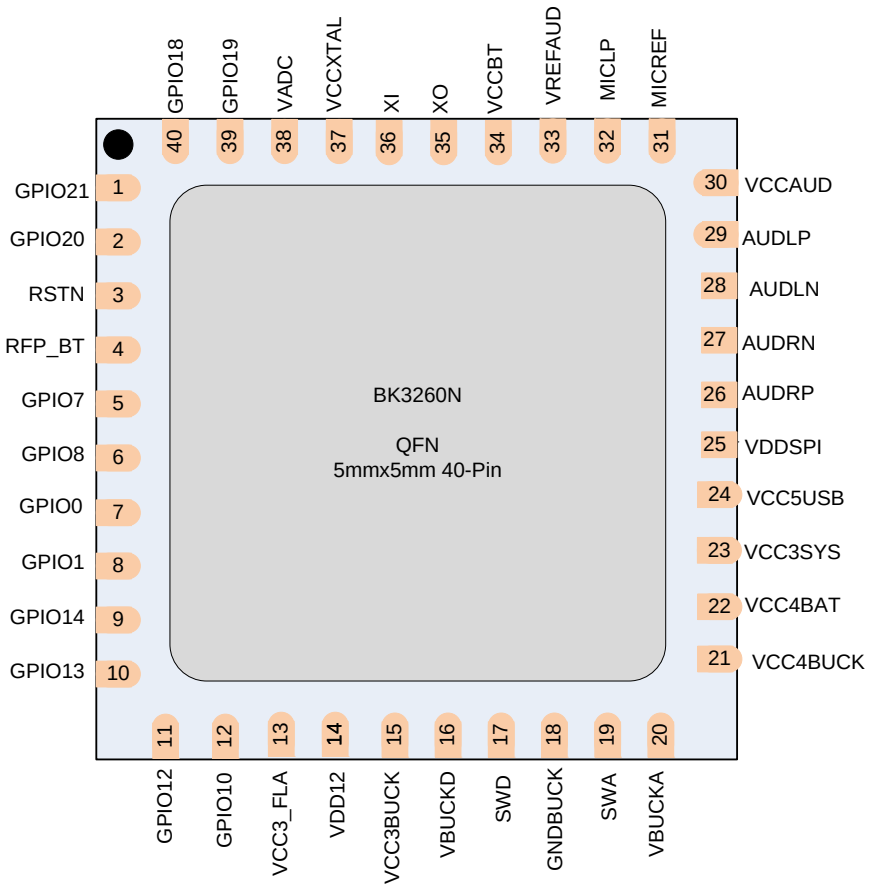


Figure 3. 40-Pin QFN 5mm x 5mm pin diagram

Table 2 Pin Description of 40-Pin Package

PIN	Name	Description
1	TDO/GPIO21	JTAG TDO / GPIO21
2	TDI/GPIO20	JTAG TDI / GPIO20
3	RSTN	reset
4	RFP_BT	RF port
5	GPIO7	GPIO7 / SPI clock
6	GPIO8	GPIO8 / SPI MOSI
7	GPIO0	GPIO0 / UART2 TXD
8	GPIO1	GPIO1 / UART2 RXD
9	GPIO14	GPIO14 / SD card data 0
10	GPIO13	GPIO13 / SD card command
11	GPIO12	GPIO12 / SD card clock
12	GPIO10	GPIO10 / PWM 0
13	VCC3_FLA	LDO Output. Power supply to FLASH，local 1uF decoupling Cap
14	VDD12	Power Input for Digital. Connected to Digital BUCK Output(Pin

		16)
15	VCC3BUCK	Buck 3V power supply Input. Connected to VCC3SYS(Pin 23)
16	VBUCKD	Switch Regulator Output for Digital
17	SWD	Buck component
18	GNDBUCK	BUCK Ground
19	SWA	Buck component
20	VBUCKA	Switch Regulator Output for Analog
21	VCC4BUCK	Power Input
22	VCC4BAT	Battery input
23	VCC3SYS	LDO Output, IO voltage; local 4.7uF decoupling cap
24	VCC5USB	USB charge input
25	VDDSPI	LDO Output, SPI power, local 100nF decoupling cap, normally NC
26	AUDIORP	Audio right channel output positive
27	AUDIORN	Audio right channel output negative
28	AUDIOLN	Audio left channel output negative
29	AUDIOLP	Audio left channel output positive
30	VCCAUD	Audio power supply Input, Connected to Analog BUCK Output
31	V2MICBIAS	LDO Output for Microphone bias
32	MICIP	Microphone input positive
33	VREF1AUD	Audio reference
34	VCC3BT	BT power supply input, Connected to Analog BUCK Output
35	XO	XTAL output
36	XI	XTAL input
37	VADC	ADC input
38	VCC3XTAL	XTAL power
39	TMS(GPIO19)	JTAG TMS / GPIO19
40	TCK(GPIO18)	JTAG TCK / GPIO18

3. Functional Description

3.1. Overview

The BK3260N is a single-chip Bluetooth SoC offering advanced audio processing and low power consumption by utilizing dedicated hardware blocks such as a five band equalizer and a hardware accelerator to increase performance and offload the MCU. The device architecture uses an internal 32 KB cache, 112 KB Data RAM, and SIP FLASH memory for system firmware which includes Beken's Bluetooth version 4.1 EDR stack and application profiles and can be used for both control and multimedia hybrid applications.

The BK3260N includes a rich set of analog and digital peripherals that allow users to add features such as a microphone input, stereo line-in inputs, SDIO memory card, and an FM radio to a Bluetooth application enhancing overall user experience.

3.2. Modes of Operation

The general operation of the BK3260N is as follows. After system reset, the BK3260N enters the low power standby mode waiting for external circuitry via the GPIO interface to wake the device up. Once the device is awake, it will establish a connection with other Bluetooth devices using the Inquire and Paging states. After a connection is made the device can be placed into Active or Sniff mode depending on the master Bluetooth device

Standby – In this mode all circuits are powered down except for the GPIO interface to allow external circuitry to wake-up the device. This is the default low power state of the chip while it is waiting to be used. There is no interaction with any Bluetooth devices in this state.

Inquire – The inquire state is entered when there is no prior information known about any connectable Bluetooth device. This state enables the device to discover which Bluetooth devices are in range and capable for a connection.

Paging – The paging state establishes the actual connection between the device and the connectable Bluetooth devices. Timing and channel hopping frequency sequences are also established in this state.

Active – During this mode, the BK3260N and the other connected Bluetooth device are actively receiving and transmitting data on the channel. This data can be high fidelity audio, voice, or control commands depending on the application.

Sniff – In this mode, the device remains active but listens and communicates at a reduce rate. The device maintains connection with the master with its Active Member Address (AM_ADDR) and goes to sleep and wakes up at assigned Sniff Intervals to exchange packets with the master.

Test – The BK3260N provides a test mode to test the internal RAM memory BIST and other blocks. The test mode is normally not used.

3.3. RF Transceiver

The BK3260N integrates a high-performance Bluetooth transceiver and frequency synthesizer. The transceiver is fully differential and incorporates an integrated on-chip balun which transforms the single-ended RF signal from the antenna through pin, RFP_BT, into an internal differential balanced signal for the low noise amplifier (LNA). On the transmit side, the differential outputs of the power amplifier (PA) are combined and transformed to a single-ended output using the same on-chip balun thus enabling only one RF pin connection to the antenna for both transmit and receive operations. The device is able to output +5 dBm of transmit output power allowing users to develop a class 2 (+4 dBm) device with small printed circuit board (PCB) antenna. The frequency synthesizer is fully integrated and does not require any external components.

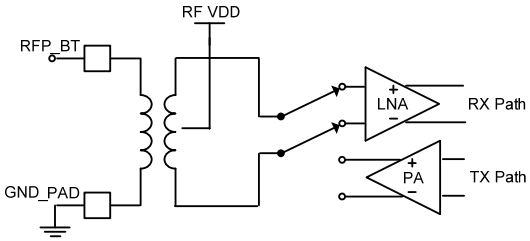


Figure 3. Simplified diagram of Bluetooth RF input pin

3.4. Bluetooth Baseband

The BK3260N Bluetooth baseband implements the Bluetooth version 4.1 Enhanced Data Rate (EDR) modem providing Basic Data Rate (BDR) 1 Mbps as well as the enhanced 2 Mbps, and 3 Mbps data rates.

Data Rate	Modulation	Bits/Symbol
BDR: 1 Mbps	GFSK	1
EDR: 2 Mbps	π/4 DQPSK	2
EDR: 3 Mbps	8 DPSK	3

Table 2. BK3260N Bluetooth Modulation Formats

The Bluetooth baseband utilizes a combination of both hardware blocks and firmware for the frequency hopping sequence generator, access code generation, detection, and correlation, encryption and decryption for security, forward error correction, 16-bit CRC, packet construction, and Bluetooth clocks and timers to optimize for power consumption and user programmability.

3.5. Audio Peripherals

The BK3260N comes with a rich set of audio peripherals to enhance the Bluetooth listening experience. The chip includes a 5-band digital equalizer, 96 dB signal-to-noise ratio (SNR) stereo analog-to-digital converter (ADC) and digital-to-analog converter (DAC), microphone input amplifier and bias, line-in input, and stereo audio left and right (L/R) outputs.

3.5.1. 5 – Band Digital Equalizer

A dedicated 5-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption. The 5-band equalizer is easily configured using the BK3260N software configuration tool kit. For more information, please refer to the BK3260N Software Configuration Tool Users Guide.

3.5.2. Stereo ADC and DAC

The BK3260N contains high fidelity 96 dB SNR stereo ADCs with sample rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates high fidelity 96 dB SNR stereo DACs with sample rates of 8 kHz, 16 kHz, 44.1 kHz or 48 kHz.

3.5.3. Microphone Input Amplifier and Bias

BK3260N contains a fully differential analog microphone input amplifier and a low-noise microphone bias generator. Expensive external components are not needed as the microphone amplifier and active bias circuitry are integrated into the chip allowing the microphone to be interfaced with only cheap passive resistors and capacitors.

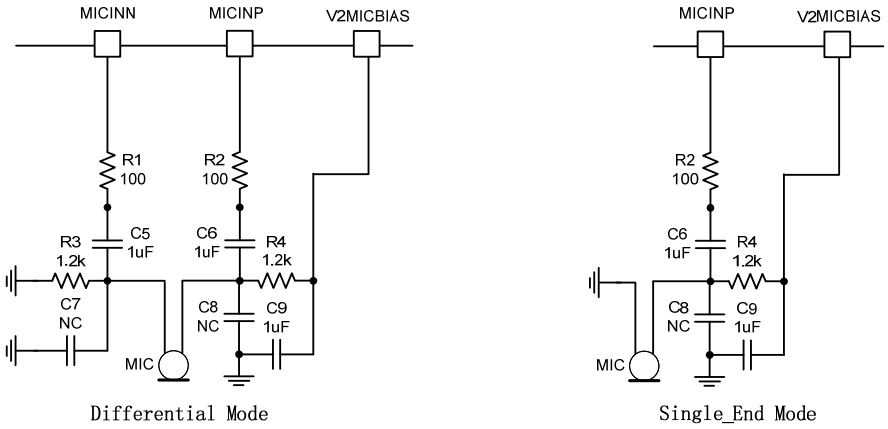


Figure 4. Microphone Interface

The differential microphone inputs (MICINN, MICINP) are routed through the microphone input amplifier providing an input resistance of 5 KΩ with a programmable gain range of 0 dB to 48 dB at a resolution of 0.5 dB. The output

of the microphone amplifier is subsequently routed to one of the stereo ADC enabling digital processing of the microphone signal.
The maximum differential input voltage is 600 mVrms when the gain is set at 0 dB and should be scaled accordingly when the gain setting is higher. The microphone bias voltage is programmable with a voltage range of 1.8V to 2.6V and a default value of 2.1 V.

3.5.4. Line-in Input

BK3260N includes stereo line-in inputs which connect to the stereo left and right channel ADCs through a 0 dB amplifier providing an input impedance of 10 kΩ. The digitized line-in inputs can be amplified with a gain of up to 31 dB and can be further processed with the 5-band equalizer prior to digital-to-analog conversion. For more details on the digital gain amplification and 5-band equalization, please refer to the BK3260N Programming Guide and BK3260N Software Configuration Tool Users Guide.

The maximum single-ended input voltage for the line-in input is 1 V rms.

3.5.5. Stereo Audio L/R Outputs

BK3260N provides high fidelity stereo audio L/R outputs capable of driving 16 Ω speakers with up to 30 pF of load capacitance. The audio outputs when loaded with 16 Ω speakers have a maximum differential output voltage swing of 1.0 V rms.

3.6. MCU

The BK3260N includes a 32-bit internal RISC MCU with 32 kB Instruction-Cache, 112 kB data RAM, and a DMA bus controller to run the Bluetooth software stack and application while supporting efficient execution and data exchange with the internal SIP FLASH memory. The JTAG interface can be used for on-line debug and can also be configured as GPIO.

3.7. FLASH Access Interface

BK3260N internal RISC MCU operates with an internal SIP FLASH program memory (typically 8 Mbits), 32 kB internal instruction cache, and 112 kB data RAM. This internal SIP FLASH memory is used to store program code, external settings and configurations, and can also be used to store user data such as encryption key configuration and Bluetooth paring information.

The BK3260N can support up to 32 Mbit of SIP FLASH memory. The FLASH memory interfaces with the chip through the FLASH Controller with the following 6 interface: CSN_FLA, SI_FLA, SO_FLA, SCK_FLA, HOLD_FLA, WP_FLA.

The BK3260N supports standard Serial Peripheral Interface (SPI) communication with either standard or extended form of the JEDEC (AMD/Fujitsu/SST) or Intel command set.

The BK3260N also supports a fast read mode using a Quad SPI communication as described in section 3.7.1 with the following pin definitions: Serial Clock (SCK_FLA), Chip Select (CSN_FLA), IO0 (SI_FLA), IO1 (SO_FLA), IO2 (WP_FLA) and IO3 (Hold_FLA). All other commands follow the standard form of JEDEC or Intel command set. The Serial Clock operates up to 100 MHz.

3.7.1. Quad I/O Word Fast Read (E7H) with "Continuous Read Mode"

The Quad I/O Word Fast Read command inputs a 3-byte memory address A23-A0 and a command byte M7-M0 with 2-dummy clocks. 2-bit per clock by IO0, IO1, IO2, IO3 each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The first byte addressed can be at any location except the lowest address bit A0 must equal 0. The address is automatically incremented after each byte of data is shifted out. The command sequence is shown in Figure 5 below.

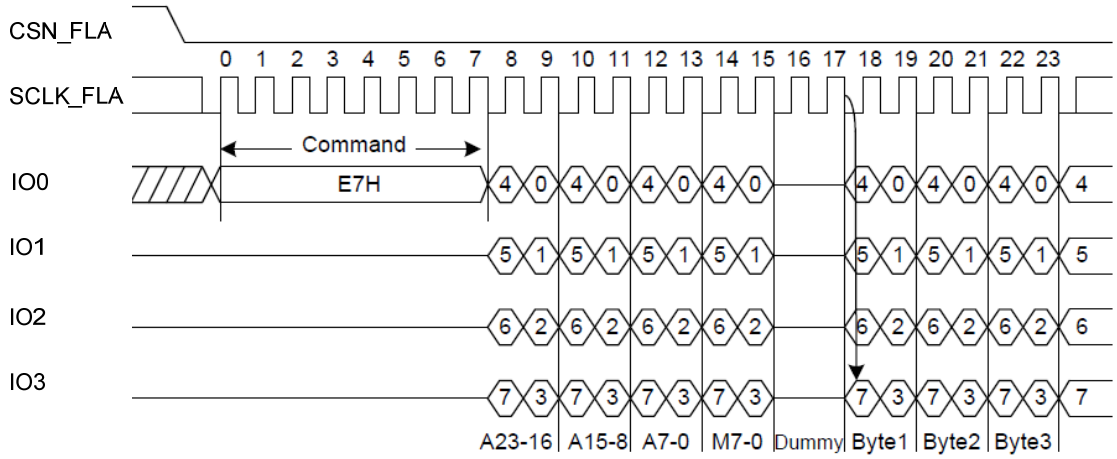


Figure 5. Quad I/O Word Fast Read Sequence (M7-M0 = 0XH or not AXH)

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-M0) after the input 3-byte address A23-A0. If the "Continuous Read Mode" bits (M7-M0) =AXH, then the next Quad I/O Word Fast Read command (after CSN_FLA is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure15. If the "Continuous Read Mode" bits (M7-M0) are any value other than AXH, the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-M0) before issuing normal command.

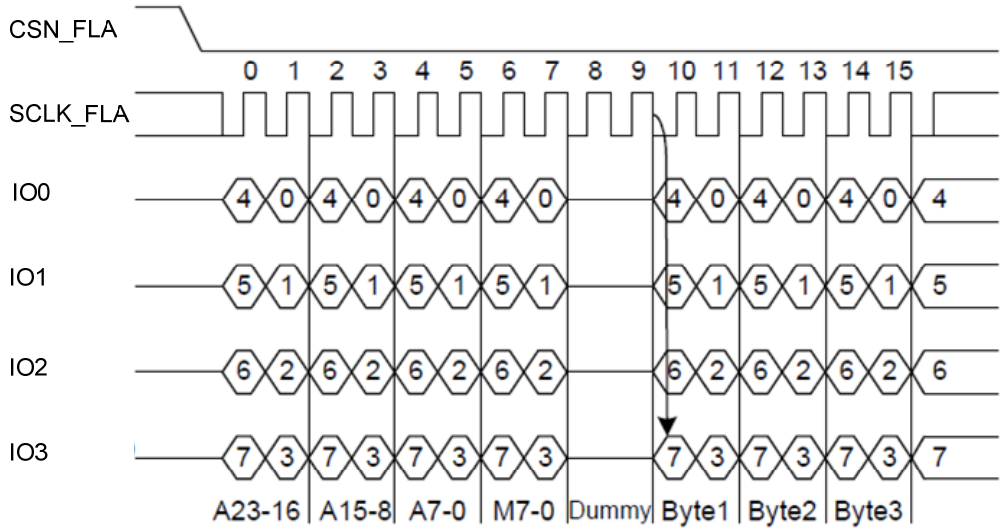


Figure 6. Quad I/O Word Fast Read Sequence (M7-M0 = AXH)

3.8. Beken Bluetooth Software Stack

The BK3260N comes with Bluetooth version 4.1 + EDR compliant software stack which run on the internal 32-bit RISC MCU. The SoC also runs the application program removing the need for an external host controller. An external host can be connected through the UART interface for debugging purposes but is not needed to run the application. Beken Corporation provides a development kit that customers can use to configure their applications. The development kit includes a software configuration tool and reference software code for stereo-mode Bluetooth speakers and hands-free operation. The interested reader is encouraged to contact their local Beken Corporation representative for more information.

3.9. Crystal Oscillator

BK3260N contains an integrated crystal oscillator driver circuit to drive an external ±10 ppm 26 MHz crystal. The 26 MHz crystal frequency provides the reference frequency to the frequency synthesizer and can also be selected as the reference clock to the internal MCU.

If an external reference clock is used, the clock input should be applied to the XI pin. Care must be taken to not overdrive the XI input with a voltage above 3.6 V.

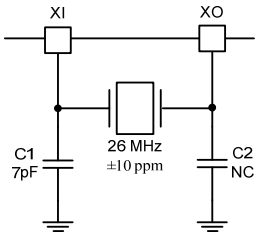


Figure 7. Crystal Oscillator Interface on BK3260N EVB

For proper crystal frequency operation, the crystal should be loaded with its specified load capacitance as given by the crystal manufacture's datasheet. Figure 78 shows 7 pF load capacitors are used with the crystal that is used on the BK3260N evaluation board (EVB). For more detailed information about the crystal oscillator interface on the EVB, please refer to the BK3260N Module Application Note.

3.10. Power Management

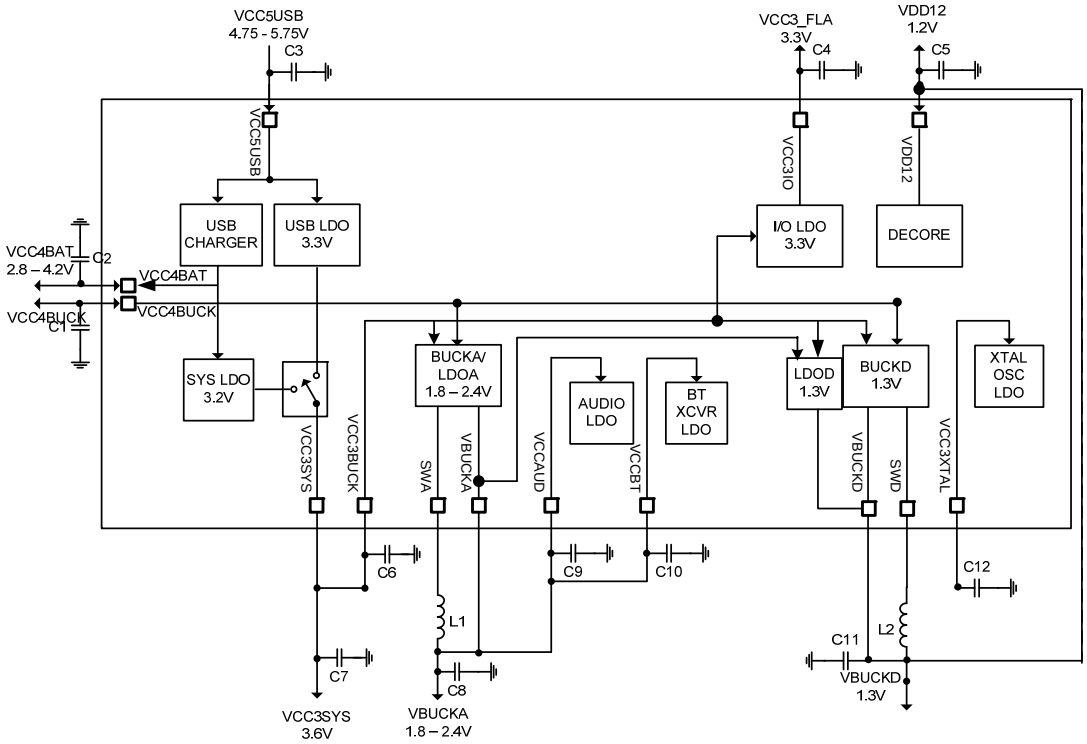


Figure 8. Block diagram of the BK3260N power management system

The power management system on the BK3260N includes a battery charger, two buck regulators which can be configured as low–drop out (LDO) regulators and 7 internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The BK3260N can be powered directly from a 2.8V to 4.2V external battery via the VCC4BAT pin and VCC4BUCK or it can be powered from a 4.75V to 5.75V

USB power supply via the VCC5USB pin. For battery powered applications, the BK3260N will generate 3.2V to the VCC3SYS pin using the SYS LDO regulator for the other of the chip to run off of. When USB power is available, the BK3260N will get its power from the USB power supply and will use the USB LDO regulator to generate 3.3V for the rest of the system to run from. If a low voltage battery is connected while the USB power supply is applied, the BK3260N will automatically charge the battery using charge current control while providing power to the chip through the USB LDO 3.3V regulator.

When BUCK is enabled, the internal analog and digital buck regulators (BUCKA, BUCKD) directly work under VBAT; The VCC3SYS regulated output voltage serves as the voltage source to all others of the chip. The LDO regulators (LDOA, LDOD, XTAL, Flash and digital) all use the VCC3SYS output voltage as their input voltage. Outputs from the buck and LDO regulators require proper bypass capacitors to reduce supply noise and these outputs are to be used only by the BK3260N. Please refer to the BK3260N EVB Users Guide or application note for more details about choosing the proper bypass capacitors.

Also one BUCK mode is available. In this condition, BUCKA is on, and BUCKD is off; and LDOD is work under output of BUCKA.

The two on-chip buck converters reduce the current consumption by about 50% and thus provide a significant improvement in overall chip power consumption.

The BK3260N can enter standby mode when there is no active connection. The standby mode can be awakened by any GPIO signal and by applying the USB power supply.

3.11. GPIO and LED Driver

The BK3260N has a total 27 GPIOs, which can be configured as either input or output. Most of them have a second function as shown below:

GPIO PIN	MBIST Mode	Peripheral Mode	GPIO Mode
GPIO0	MBIST DONE	UART_TXD / I2C_SCL	General I/O
GPIO1	MBIST_FAIL	UART_RXD / I2C_SDA	General I/O
GPIO2	INPUT	TX_EN	General I/O
GPIO3	INPUT	RX_EN	General I/O
GPIO4	INPUT	NC	General I/O
GPIO5	INPUT	ADC2	General I/O
GPIO6	INPUT	SPI_CSN	General I/O
GPIO7	MODE_SEL[1]	SPI_SCK	General I/O
GPIO8	MODE_SEL[0]	SPI_MOSI	General I/O
GPIO9	INPUT	SPI_MISO	General I/O
GPIO10	INPUT	PWM0	General I/O
GPIO11	MBIST_PASS	PWM1	General I/O
GPIO12	INPUT	SD_CLK	General I/O
GPIO13	INPUT	SD_CMD	General I/O

GPIO14	INPUT	SD_DATA0	General I/O
GPIO15	INPUT	SD_DATA1	General I/O
GPIO16	INPUT	SD_DATA2	General I/O
GPIO17	INPUT	SD_DATA3	General I/O
GPIO18	MBIST_FAIL_IND[3]	JTAG_TCK	General I/O
GPIO19	MBIST_FAIL_IND[2]	JTAG_TMS/ADC3	General I/O
GPIO20	MBIST_FAIL_IND[1]	JTAG_TDI	General I/O
GPIO21	MBIST_FAIL_IND[0]	JTAG_TDO	General I/O
GPIO22	INPUT	IRDA_INPUT	General I/O
GPIO23 (Schmidt)	INPUT	CLK32K_INPUT	General I/O
GPIO24	INPUT	FM_CLK13M	General I/O
GPIO25	INPUT	FM_SCL	General I/O
GPIO26	INPUT	FM_SDA	General I/O

Table 4 GPIO Function Mapping

All GPIO pins can wake up the internal MCU from standby mode. In standby mode, any level change on the set GPIO will trigger the wake up procedure.

During power up, the default state of GPIO0~GPIO9, GPIO12~GPIO17, and GPIO22~GPIO26 is high impedance and pulled low internally; the default state of GPIO10~GPIO11 is high impedance and pulled high; and the default state of GPIO18~GPIO21 is JTAG function, GPIO18~GPIO20 is input with pull down, and GPIO21 is output without pull.

GPIO11 and GPIO10 can be configured as LED drivers to support up to 10 mA current. The LED drivers are easily programmable with the BK3260N tool kit.

3.12. PWM Timer and Watch Dog Timer

There are two sets of PWM timers. One set (fast) uses 1 MHz clock as the main clock, and another set (slow) uses 100 kHz clock as main clock. Each set has three 16-bit counters with 4-bit pre-divider. The first two timers in the slow set can be used for LED duty cycle control.

The watch dog timer runs from the 100 kHz clock and has a maximum programmable period of up to 10.48 (2^16/100kHz * 16) seconds.

3.13. I2C and UART Interface

There is an I2C interface or UART interface for debug or external MCU control of the BK3260N. They both share the same pins GPIO0 and GPIO1.

3.14. SPI Interface

The 4-wire SPI interface supports high speed data communication which can be used as an interface for an external memory or LCD controller.

3.15. FM Receiver Control Interface / I2C Interface

BK3260N interfaces directly with all of Beken's BK108X series of FM receivers to easily add an FM radio to a Bluetooth application. The FM receiver control interface consists of a two-wire I2C interface and a 13 MHz clock. The BK3260N can be programmed to provide the 13 MHz clock on the GPIO24 pin and the SCL and SDA I2C signals can be programmed onto the GPIO25 and GPIO26 pins, respectively.

3.16. General Purpose SAR ADC

The general purpose SAR ADC has 10-bit resolution with a programmable sampling rate range from 5 kHz up to 50 kHz and is used to measure DC and low frequency voltages. The input voltage range for the ADC is from 0V to 3V. The general purpose ADC has six channels as shown in Table 5.

Channel Number	Detected Voltage	Description
1	VBAT	Monitor battery voltage(0.65*VBAT)
2	VADC-pin	Pin VADC voltage
3	GPIO5	GPIO5 Voltage
4	VCC5USB-pin 6	Monitor USB voltage(0.5*VUSB)
5	GPIO19	GPIO19 voltage
6	Temp-Sensor	Temp-Sensor Output voltage

Table 5 ADC Channel Table

3.17. DTMF Generator

BK3260N contains a dual-tone multi-frequency (DTMF) generator allowing a Bluetooth application to generate DTMF tones for telephone signaling. The DTMF tones can be configured using the BK30060N tool kit. For more details, please refer to the BK3260N Programming Guide and BK3260N Software Configuration Tool Users Guide.

3.18. SDIO Card Interface

BK3260N includes a secure digital input output (SDIO) card interface. The six GPIO lines GPIO12 through GPIO17 can be used as SD_CLK, SD_CMD, SD_DATA[0], SD_DATA[1], SD_DATA[2], and SD_DATA[3]. This interface allows users to easily add an SDIO card to a Bluetooth application. For more information, please refer to the BK3260N Programming Guide and BK3260N Software Configuration Tool Users Guide.

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Parameter	Description	MIN	TYP	MAX	Unit
VCC4BAT	Battery regulator supply voltage	-0.3		4.2	V
VCC5USB	USB power supply voltage	4.75		5.75	V
VCCBT	BT transceiver supply voltage	1.6		2.4	V
VCCAUD	Audio supply voltage	1.6		2.4	V
VCC3XTAL	Crystal supply voltage	2.8		3.8	V
P_{RX}	RX input power	-	10	-	dBm
T_{STR}	Storage temperature range	-40	-	150	℃

4.2. Recommended Operating Conditions

Parameter	Description	MIN	TYP	MAX	Unit
VCC4BAT	Battery regulator supply voltage	2.8	3.6	4.2	V
VCC5USB	USB power supply voltage	4.75	5	5.75	V
VCCBT	BT transceiver supply voltage	1.6		2.4	V
VCCAUD	Audio supply voltage	1.6		2.4	V
VCC3XTAL	Crystal supply voltage	2.8		3.8	V
T_{OPR}	Operation temperature range	-20	-	80	℃

4.3. System LDO

Parameter	Description	MIN	TYP	MAX	Unit
VCC4BAT	Battery input voltage	2.8		4.2	V
VCC3SYS	LDO output voltage	2.8	3.2	3.8	V
Load Current	Load current			200	mA

4.4. USB LDO

When USB is plug in, VCC3SYS will be generated from USB LDO.

Parameter	Description	MIN	TYP	MAX	Unit
VCC5USB	USB Input voltage	4.75	5	5.75	V
VCC3SYS	LDO output voltage		3.3		V
Load Current	Load current			200	mA

4.5. BATTERY CHARGE

Parameter	Description	MIN	TYP	MAX	Unit
VCC5USB	Charger input voltage	4.75	5	5.75	V
I_trickle	Charge Current at trickle mode as percent of fast charge mode		10		%
I_fast	Charge current at fast charge mode	40		220	mA
V_end(Need Calibrated)	VBAT voltage when Charge End		4.2		V

4.6. Analog LDO/BUCK

System can choose the analog BUCK or LDO as the power supply of RF and Audio part.

Parameter	Description	MIN	TYP	MAX	Unit
Analog LDO					
VCC3BUCK	Analog LDO input voltage	2.8		3.6	V
VBUCKA	Analog LDO output voltage	1.6	1.8	2.4	V
Load Current	Load current			150	mA
Analog BUCK					
VCC4BUCKA	Analog BUCK input voltage	2.8		4.2	V
VBUCKA	Analog BUCK output voltage	1.6	1.8	2.4	V
Load Current	Load current			150	mA
Switching frequency	BUCK modulation frequency	0.5	1	6	MHz

4.7. Digital LDO/BUCK

System can also choose the digital BUCK or LDO as the power supply for the Digital part.

Parameter	Description	MIN	TYP	MAX	Unit
Digital LDO					
VCC3BUCK	Digital LDO input voltage	1.6		3.6	V
VBUCKD	Digital LDO output voltage	1	1.2	1.35	V
Load Current	Load current			70	mA
Digital BUCK					
VSYS3V8D	Digital BUCK input voltage	2.8	3.3	4.2	V
VBUCKD	Digital BUCK output voltage	1	1.2	1.35	V
Load Current	Load current			100	mA
Switching frequency	BUCK modulation frequency	0.5	1	6	MHz

4.8. Crystal and Reference Clock

Parameter	Description	MIN	TYP	MAX	Unit
Frequency	Crystal and Reference frequency	-	26	-	MHz

Tolerance	Crystal and Reference frequency tolerance	-10	-	+10	ppm
XI Pin	Input voltage range for reference clock input	-0.3		3.6	V

4.9. Typical Power Consumption

State	Description	MIN	TYP	MAX	Unit
Standby	Software sets device into standby mode, wake up from GPIO		6	9	uA
Idle-Sniff	Idle state at Sniff mode		700		uA
Active (A2DP)	2DH5		17		mA
Active (HFP)	HV1		19		mA

4.10. RF Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
Operate Frequency	2402~2480	2402		2480	MHz
RXSENS-1 Mbps	BER=0.001		-90		dBm
RXSENS-2 Mbps	BER=0.0001		-92		dBm
RXSENS-3 Mbps	BER=0.0001		-84		dBm
Maximum received signal	BER=0.001	0			dBm
Maximum RF transmit power			5		dBm
RF Power Control Range		30			dB

4.11. Audio Characteristics

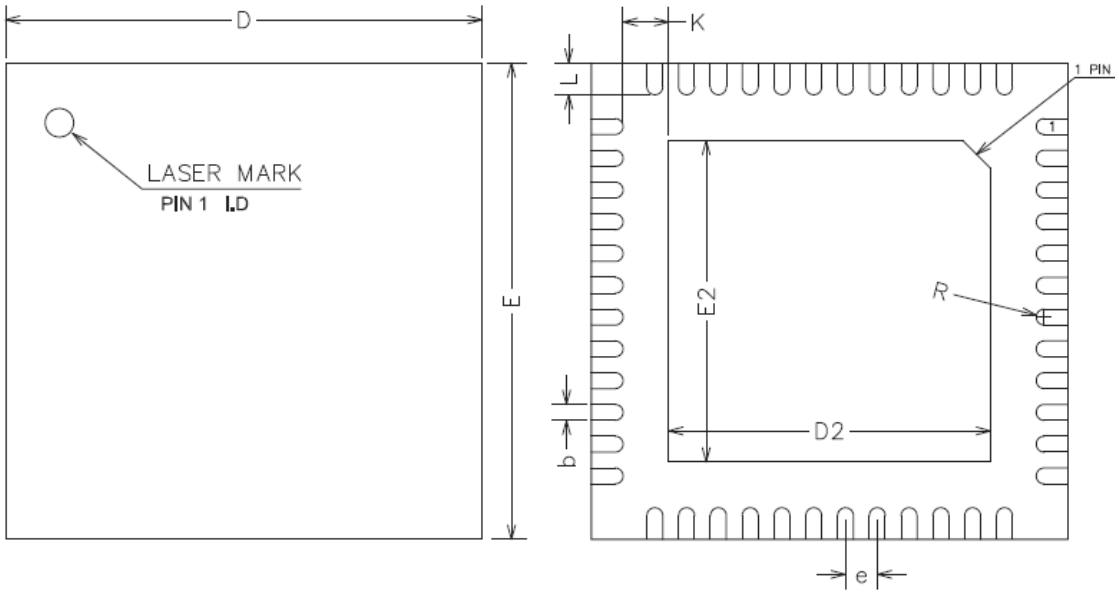
Parameter	Condition	MIN	TYP	MAX	Unit
DAC Diff. Output Vpp	With 600ohm loading			1.2	Vrms
	With 32ohm loading			1.05	Vrms
	With 16ohm loading			0.85	Vrms
DAC Diff. Output THD	With 1.1Vrms@600ohm loading		78		dB
	With 0.8Vrms@16ohm loading		73		dB
DAC output SNR	1 kHz sine wave		96		dB
DAC Sample Rate		8		48	kHz
ADC SNR	1 kHz sine wave		96		dB
ADC Sample Rate		8		48	kHz

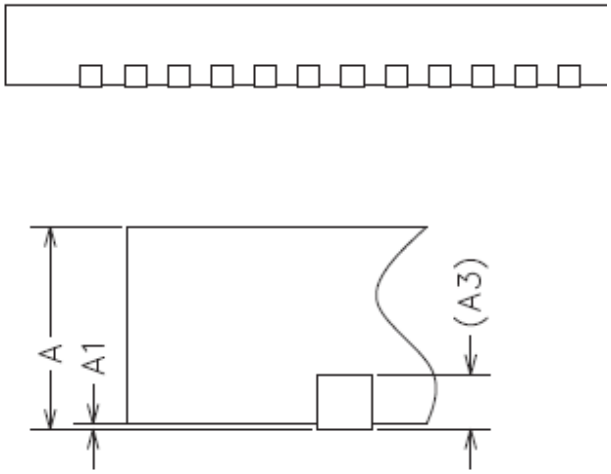
5. About Qualification

By carefully laying out the printed circuit board (PCB), the BK3260N RF performance meets FCC, CE and BQB requirement. The Bluetooth protocol and profile provided by Beken are already qualified and listed in the SIG website. If there is any end product listing requirement with the BK3260N, please inquire your local Beken Corporation representative for the related QDID authorization.

6. Package Information

6.1. QFN 6x6 48-pin package

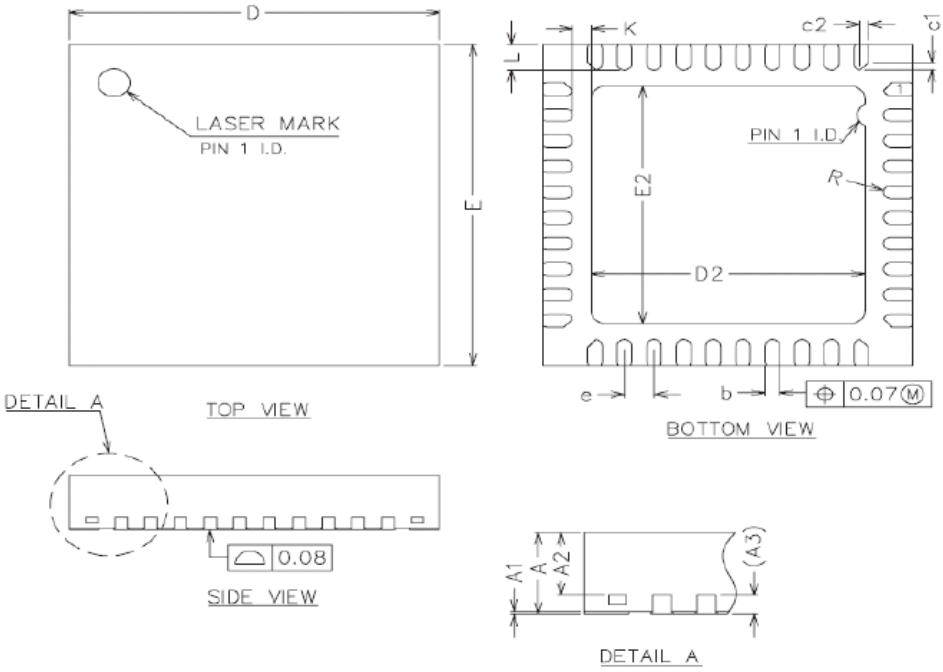




COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.95	4.05	4.15
E2	3.95	4.05	4.15
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.09	–	–

6.2. QFN 5x5 40-pin package



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2	0.50	0.65	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	–	–
L	0.35	0.40	0.45
R	0.075	–	–
C1	–	0.12	–
C2	–	0.12	–

7. Ordering Information

Part number	Package	Packing	MOQ (ea)
BK3260N	QFN 6mmx6mm 48-Pin	Tape Reel	10 k
BK3260N	QFN 5mmx5mm 40-Pin	Tape Reel	10 k

Remark:

MOQ: Minimum Order Quantity