BK3511

Specifications

Beken Internal Data — Signed NDA Required for Distribution

Single Chip for Bluetooth and FM Receiver

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Contents

1. General Description

The BK3511 chip is mainly used for mobile applications to provide Bluetooth 2.1 + EDR and FM radio. It can use battery power supply directly to save the power consumption and can make the Bluetooth and FM operate simultaneously and independently. BK3511 enables Bluetooth and FM radio with small board space and minimum number of external components then the manufactures can fast and successfully make their product integrated with BK3511 go on the market.

The BK3511 is available in 32-pin 4x4 mm QFN packages.

1.1. Features

1.1.1. BT Radio Features

- On-chip TX/RX switch
- Polar modulation transmitter architecture with very low power consumption and high TX performance
- Near-Zero IF receiver architecture with -91dBm sensitivity
- Support for class 1, class 2 and class 3 transmitting power requirement
- Fully integrated synthesizer without external loop filter component

1.1.2. BT Baseband Features

- Fully compliant with Bluetooth 2.1 + EDR specification
- Support Bluetooth Piconet and Scatternet
- Support up to 3Mbps high speed UART interface
- Support Sniff mode, hold mode and park mode
- Support A-law, μ-law and CVSD digitize audio CODEC in PCM interface
- Provide I2C interface

1.1.3. FM Features

- Support 64~108 MHz band
- Automatic gain control
- Automatic frequency control
- Seek tuning
- Receive signal strength indicator
- Channel quality assessment
- Stereo decoder
- Automatic stereo/mono switching
- Automatic noise suppression
- 50us/75us de-emphasis
- 2.5 ~ 5.5 V supply voltage
- Wide range reference clock supported
- 32.768KHz crystal oscillator

1.1.4. Device Features

- Enhanced support for WLAN/BT Co-existence
- Standby and sleep modes to minimize power consumption
- Support share handset system reference clock

1.2. Applications

- Mobile handset
- MP3, MP4 player and PMP
- Other portable devices

2. Pin Definition

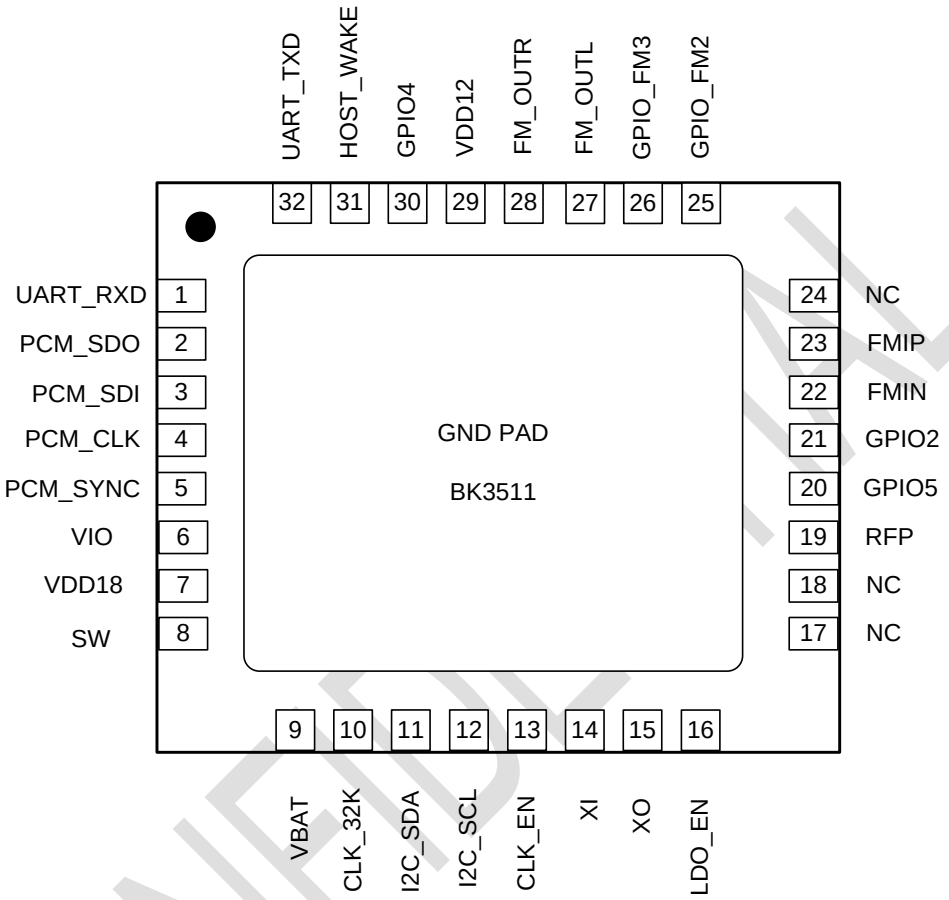

Figure 1 BK3511 PIN Definition Diagram

Table 1 Pin Definition

Package Pin #	Name	Description
1	UART_RXD	UART RX data input
2	PCM_SDO	PCM data output
3	PCM_SDI	PCM data input
4	PCM_CLK	PCM data clock
5	PCM_SYNC	PCM data sync
6	VIO	IO power supply
7	VDD18	1.8V voltage output, connected with 1uF decoupling cap.
8	SW	Internal buck regulator output
9	VBAT	VBAT LDO input, connected with 1uF decoupling cap.
10	CLK_32K	32.768 kHz clock input

11	I2C_SCL	I2C Clock signal
12	I2C_SDA	I2C Data signal
13	CLK_EN	Request source clock active
14	XI	Crystal input or oscillator input.
15	XO	Crystal output.
16	LDO_EN	System power on/off control
17	NC	Not connect
18	NC	Not connect
19	RFP	RF input and output
20	GPIO5	General purpose input/output
21	GPIO2	General purpose input/output or Bluetooth Priority signal
22	FMIN	FM RF input negative port
23	FMIP	FM RF input positive port
24	NC	Not connect
25	GPIO_FM2	FM General purpose input/output
26	GPIO_FM3	FM General purpose input/output
27	FM_OUTL	FM left audio output
28	FM_OUTR	FM right audio output
29	VDDD12	Power supply for digital
30	GPIO4	General purpose input/output or WLAN Active signal
31	HOST_WAKE	To wakeup host. Output to host.
32	UART_TXD	UART TX data output

3. Functional Description

3.1. Block Diagram

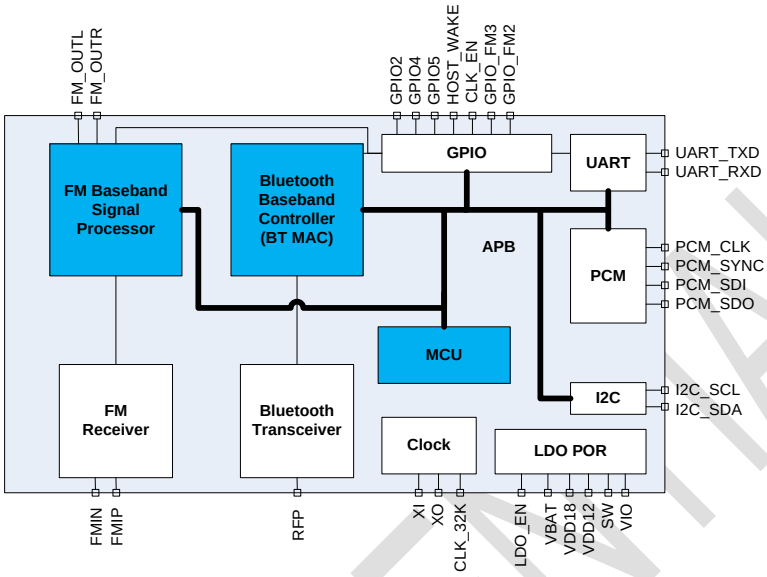

Figure 2 BK3511 Block Diagram

As shown in the **Figure 2**, the BK3511 integrates the Bluetooth transceiver, FM receiver, Bluetooth baseband controller, FM baseband signal processor and MCU etc. The Bluetooth transceiver integrates the low-IF single conversion RX and Polar loop modulation TX. The FM receiver employs a digital low-IF architecture that reduces external components. The Bluetooth baseband controller carries out the baseband protocols and other low-level link routines such as modulation/demodulation, packets processing, bit stream processing, frequency hopping and so on.

3.2. I2C bus mode

When selecting I2C mode, user must set MODE = 0.

I2C bus mode only uses I2C_SCL and I2C_SDA pins. A transaction begins with the start condition, which occurs when I2C_SDA falls while I2C_SCL is high. Next, user drivers an 8-bit device ID serially on I2C_SDA, which is captured by BK3511 at the rising edge of I2C_SCL. The device ID of BK3511 is 0x80.

After driving the device ID, user drives an 8-bit control word on I2C_SDA. The control word consists of a 7-bit start register address, followed by a read/write bit (read = 1, write = 0).

For I2C host reading, the host must give an ACK to BK3511 after each byte access, and should give a NACK to BK3511 after last byte read out.

For stable communication, the rising edge time of I2C_SCL should be less than 200ns.

3.3. I2C Control Interface Characteristics

Table 2 I2C Control Interface Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
I2C_SCL Frequency	f_{SCL}		—	—	400	kHz
I2C_SCL Low Time	t_{LOW}		1.3	—	—	μs
I2C_SCL High Time	t_{HIGH}		0.6			μs
I2C_SCL Input to I2C_SDA Setup (START)	$t_{SU:STA}$		0.6	—	—	μs
I2C_SCL Input to I2C_SDA Hold (START)	$t_{HD:STA}$		0.6	—	—	μs
I2C_SDA Input to I2C_SCL Setup	$t_{SU:DAT}$		100	—	—	ns
I2C_SDA Input to I2C_SCL Hold	$t_{HD:DAT}$		—	—	900	ns
I2C_SCL Input to I2C_SDA Setup (STOP)	$t_{SU:STO}$		0.6	—	—	μs
STOP to START Time	t_{BUF}		1.3	—	—	μs
I2C_SDA Output Fall Time	$t_{f:OUT}$		—	—	250	ns
I2C_SDA Input, I2C_SCL Rise/Fall Time	$t_{f:IN}$ $t_{r:IN}$		—	—	200	ns
I2C_SCL,I2C_SDA Capacitive Loading	C_b		—	—	60	pF
Input Filter Pulse Suppression	t_{SP}		—	—	40	ns

Details please refer to BK3511 programming guide and BK1080E programming guide and Datasheet.

4. Bluetooth Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

Parameter	Description	MIN	TYP	MAX	Unit
VBAT	Battery Regulator Supply Voltage	-0.3		4.8	V
P_{RX}	RX Input Power	-	10	-	dBm
T_{STR}	Storage Temperature Range	-40	-	150	℃
Vcc	Input Voltage	-0.3	-	3.6	V

4.2. Recommended Operating Conditions

Table 4 Recommended Operating Conditions

Parameter	Description	MIN	TYP	MAX	Unit
VBAT	Battery Regulator Supply Voltage	3.3	4	4.2	V
T_{OPR}	Operation Temperature Range	-20	-	60	℃
V_{IL}	CMOS Low Level Input Voltage	0	-	0.3*VIO	V
V_{IH}	CMOS High Level Input Voltage	0.7*VIO	-	VIO	V
V_{TH}	CMOS Threshold Voltage		0.5*VIO		V

Notes:
1. VIO=1.8~3.3V

4.3. Typical Power Consumption

Table 5 Typical Power Consumption

State	Description	MIN	TYP	MAX	Unit
Shut Down			8		uA
Sleep			600		uA
Only HCI Active			5		mA
DH1/DM1			42		mA
DH3/DM3			46		mA
DH5/DM5			47		mA

4.4. RX AC Characteristics

4.4.1. Basic Data Rate mode RX AC Characteristics

Table 6 Basic Data Rate mode RX AC Characteristics

(VBAT = 3.6 V, T_{OPR} = 27℃, unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Input Frequency	2402~2480	2402	-	2480	MHz

RXSENS	BER=0.001	-	-89	-	dBm
Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	10	-	dB
C/I1ST	F = F0 + 1MHz	-	0	-	dB
	F = F0 - 1MHz	-	0	-	dB
C/I2ND	F = F0 + 2MHz	-	-15	-	dB
	F = F0 - 2MHz	-	-24	-	dB
C/I3RD	F = F0 + 3MHz	-	-30	-	dB
	F = F0 - 3MHz	-	-40	-	dB
C/I Image Channel	F = Fimage	-	-15	-	dB
Out-of-Band Blocking Performance	30MHz–2000MHz	-10	-	-	dBm
	2000MHz–2400MHz	-27	-	-	dBm
	2500MHz–3000MHz	-27	-	-	dBm
	3000MHz–12.5GHz	-10	-	-	dBm
Intermodulation		-	-37	-	dBm

4.4.2. Enhanced Data Rate mode RX AC Characteristics

Table 7 Enhanced Data Rate mode RX AC Characteristics

(VBAT = 3.6 V, T_{OPR} = 27℃, unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
π/4 DQPSK					
RXSENS	BER=0.0001	-	-91	-	dBm
BER Floor	BER=0.00001	-	-85	-	dBm
Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	11	-	dB
C/I1ST	F = F0 + 1MHz	-	-11	-	dB
	F = F0 - 1MHz	-	-11	-	dB
C/I2ND	F = F0 + 2MHz	-	-15	-	dB
	F = F0 - 2MHz	-	-27	-	dB
C/I3RD	F = F0 + 3MHz	-	-32	-	dB
	F = F0 - 3MHz	-	-40	-	dB
C/I Image Channel	F = F_{image}	-	0	-	dB
8DPSK					
RXSENS	BER=0.0001	-	-83	-	dBm
BER Floor	BER=0.00001	-	-78	-	dBm
Maximum Received Signal	BER=0.001	0	-	-	dBm
C/ICO		-	20	-	dB
C/I1ST	F = F0 + 1MHz	-	-5	-	dB
	F = F0 - 1MHz	-	-5	-	dB
C/I2ND	F = F0 + 2MHz	-	-10	-	dB
	F = F0 - 2MHz	-	-22	-	dB
C/I3RD	F = F0 + 3MHz	-	-30	-	dB
	F = F0 - 3MHz	-	-30	-	dB

C/I Image Channel	$F = F_{image}$	-	4	-	dB

4.5. TX AC Characteristics

4.5.1. Basic Data Rate mode TX AC Characteristics

Table 8 Basic Data Rate mode TX AC Characteristics

(VBAT = 3.6 V, T_{OPR} = 27℃, unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Maximum RF Transmit Power		-	8	9	dBm
RF Power Control Range		-	15	-	dB
20dB Band Width		-	0.9	-	MHz
ACP1ST	F = F0 + 1MHz	-	-	-	dBm
	F = F0 - 1MHz	-	-	-	dBm
ACP2ND	F = F0 + 2MHz	-	-30	-	dBm
	F = F0 - 2MHz	-	-30	-	dBm
ACP≥3RD	F = F0 + ≥ 3MHz	-	-40	-	dBm
	F = F0 - ≥ 3MHz	-	-40	-	dBm
Out-of-Band Spurious Emission	30MHz to 1GHz, Operating Mode	-	-36	-	dBm
	1GHz to 12.75GHz, Operating Mode	-	-30	-	dBm
	1.8GHz to 1.9GHz, 5.15GHz to 5.3GHz	-	-47	-	dBm
Δf1avg Maximum Modulation		-	160	-	KHz
Δf2max Minimum Modulation		-	120	-	KHz
Δf2avg/Δf1avg		-	0.9	-	-
Initial Carrier Frequency Tolerance		-	5	-	KHz
Drift Rate		-	7	-	KHz/50us
Drift (1 slot packet)		-	8	-	KHz
Drift (3 slot packet)		-	8	-	KHz
Drift (5 slot packet)		-	10	-	KHz

4.5.2. Enhanced Data Rate mode TX AC Characteristics

Table 9 Enhanced Data Rate mode TX AC Characteristics

(VBAT = 3.6 V, T_{OPR} = 27℃, unless otherwise specified)

Parameter	Condition	MIN	TYP	MAX	Unit
Maximum RF Transmit Power		-	4	6	dBm
Relative Transmit Power		-	-4	-	dB
π/4 DQPSK Max Carrier Frequency Stability w_0		-	2	-	kHz
π/4 DQPSK Max Carrier Frequency Stability w_i		-	3	-	kHz

π/4 DQPSK Max Carrier Frequency Stability $\|w_i + w_0\|$		-	1.5	-	kHz
8DPSK Max Carrier Frequency Stability w_0		-	2	-	kHz
8DPSK Max Carrier Frequency Stability w_i		-	3	-	kHz
8DPSK Max Carrier Frequency Stability $\|w_i + w_0\|$		-	1.5	-	kHz
π/4 DQPSK Modulation Accuracy	RMS DEVM	-	7	-	%
	99% DEVM	-	-	20	%
	Peak DEVM	-	15	-	%
8DPSK Modulation Accuracy	RMS DEVM	-	9	-	%
	99% DEVM	-	-	20	%
	Peak DEVM	-	17	-	%
ACP1ST	F = F0 + 1MHz	-	-14	-	dBm
	F = F0 - 1MHz	-	-13	-	dBm
ACP2ND	F = F0 + 2MHz	-	-20	-	dBm
	F = F0 - 2MHz	-	-20	-	dBm
ACP≥3RD	F = F0 + ≥3MHz	-	-40	-	dBm
	F = F0 - ≥ 3MHz	-	-40	-	dBm
EDR Differential Phase Coding		-	100	-	%

5. FM Electrical Characteristics

5.1. Recommended Operating Conditions

Table 10 Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Digital Supply Voltage	V_D		2.5	—	5.5	V
Analog Supply Voltage	V_A		2.5	—	5.5	V
Interface Supply Voltage	V_{IO}		1.6	—	3.6	V
Ambient Temperature	T_A		-20	25	85	℃
Notes: All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at VIO = VBAT = 3.3 V and 25 ℃ unless otherwise stated. Parameters are tested in production unless otherwise stated.						

5.2. Absolute Maximum Ratings

Table 11 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Digital Supply Voltage	V_D	-0.5	—	+5.8	V
Analog Supply Voltage	V_A	-0.5	—	+5.8	V
Interface Supply Voltage	V_{IO}	-0.5	—	+4.0	V
Operating Temperature	T_{OP}	-20	—	85	℃
Storage Temperature	T_{STG}	-55	—	150	℃

5.3. Power Consumption Specification

Table 12 Power Consumption Specification

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Supply Current	I_S	ENABLE = 1 DISABLE = 0	—	20	22	mA
Power down Current	I_{PD}	ENABLE = 0 DISABLE = 1	—	10	20	μA
Interface Power down Current	Ip_{IO}	I2C_SCL, RCLK inactive ENABLE = 0	—	1.9	5	μA

5.4. FM Receiver Characteristics

Table 13 FM Receiver Characteristics

Parameter	Test Condition	Min	Typ	Max	Unit
Input Frequency [14]		64	—	108	MHz
Sensitivity[2, 3, 4,5]	(S+N)/N = 26 dB	—	1.5	2.5	µV EMF
LNA Input Resistance[7]		2.5	3	3.5	kΩ
Input IP3[8]		90	95	—	dBµV EMF
AM Suppression[2, 3, 4, 5, 7]	m = 0.3	40	45	—	dB
Adjacent Channel Selectivity	±200 kHz	40	50	—	dB
Alternate Channel Selectivity	±400 kHz	50	60	—	dB
Audio Output Voltage[2, 3, 4, 7]		—	100	—	mVRMS
Audio Stereo Separation[2, 4, 5, 7]		30	40	—	dB
Audio S/N[2, 3, 4, 5, 7, 13]			60	—	dB
Audio THD[2, 3, 5, 7, 10]		—	0.2	0.5	%
Audio Common Mode Voltage[12]	ENABLE = 1	1.1	1.2	1.3	V
Audio Output Load Resistance	Single-ended	—	32	—	Ω
Seek/Tune Time		—	—	60	ms/channel
RSSI Offset	Input levels of 8 and 50 dBµV at RF input	–3	—	3	dB

Notes:

1. Volume = maximum for all tests
2. F_{MOD} = 1 kHz, 75 µs de-emphasis
3. MONO = 1, and L = R unless noted otherwise
4. Δf = 22.5 kHz
5. B_{AF} = 300 Hz to 15 kHz, A-weighted
6. Sensitivity without matching network
7. Measured at V_{EMF} = 1 mV, f_{RF} = 64 to 108 MHz
8. |f2 – f1| > 1 MHz, f0 = 2 x f1 – f2. AGC is disabled by setting AGCD = 1
9. The channel spacing is selected with the SPACE [1:0] bits
10. Δf = 75 kHz
11. The de-emphasis time constant is selected with the DE bit
12. At LOUT and ROUT pins
13. Guaranteed by reference clock performance

6. Application Schematic

The compatible design for BK3211 and BK3511,
which inside the square brackets are BK3511 Pin names or component values

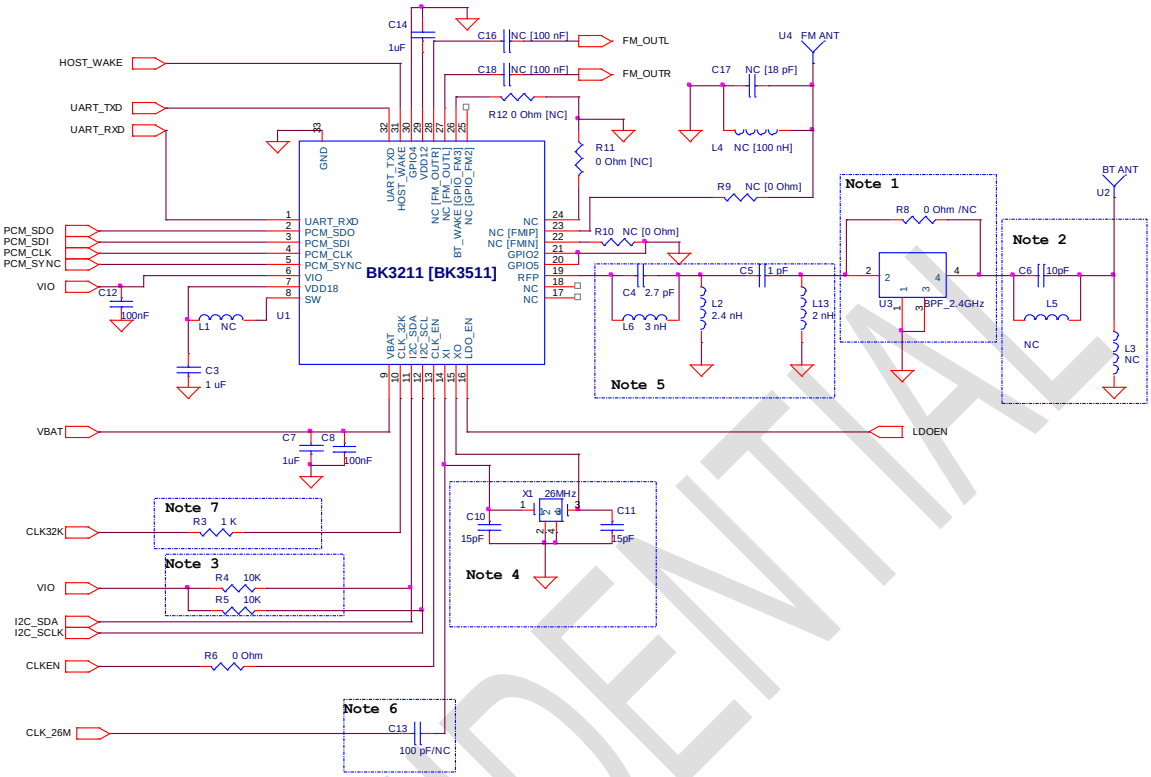

Figure 3 BK3511 Application Diagram

The detail schematic design please refers to the hardware design reference.

7. Package Information

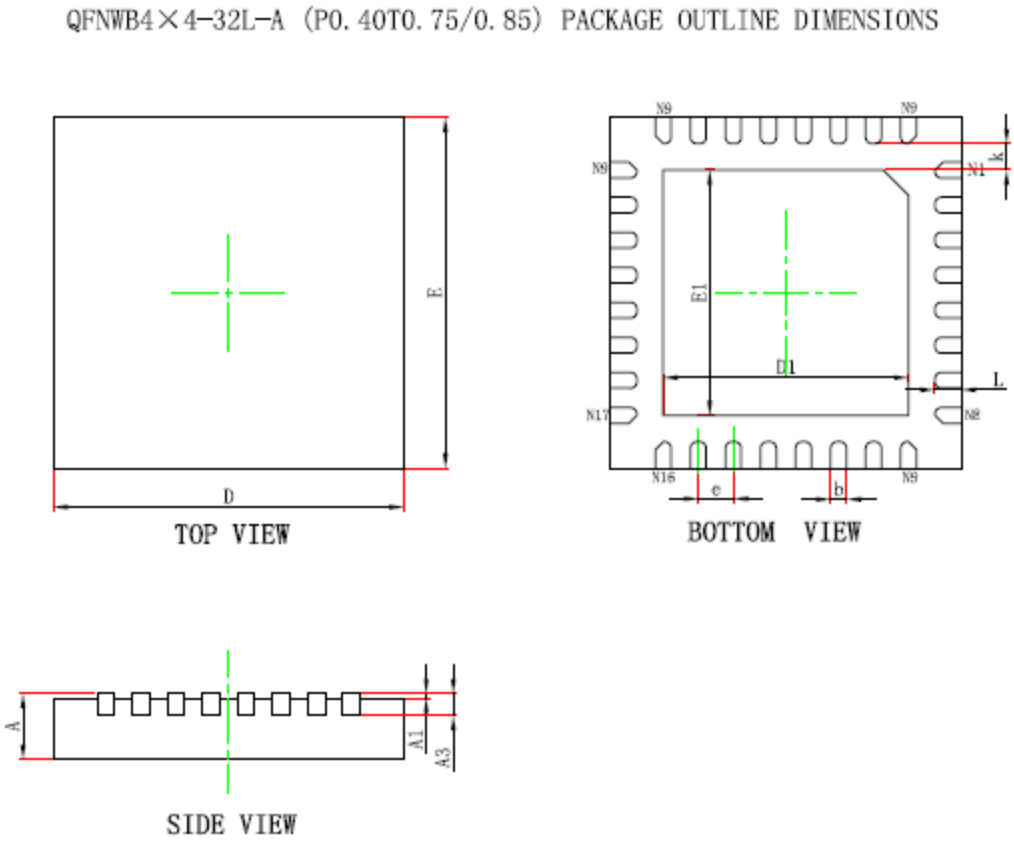

Figure 4 QFN 4x4 32 Pin Package diagram

Table 14 QFN 4x4 32 Pin Package dimensions

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.700	2.900	0.106	0.114
E1	2.700	2.900	0.106	0.114
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.224	0.376	0.009	0.015

8. Solder Reflow Profile

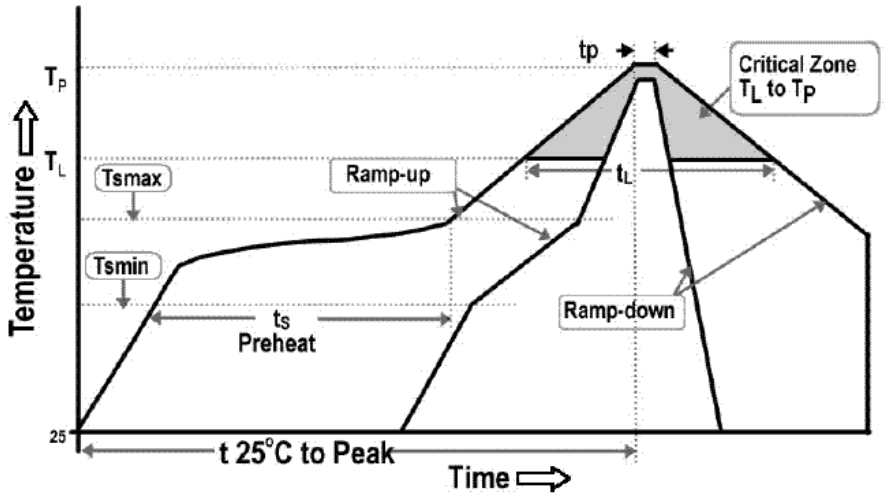

Figure 5 Classification Reflow Profile

Table 15 Solder Reflow Profile

Profile Feature		Specification
Average Ramp-Up Rate (tsmax to tp)		3℃/second max.
Pre_heat	Temperature Min (Tsmin)	150℃
	Temperature Max (Tsmax)	200℃
	Time (ts)	60-180 seconds
Time Maintained above	Temperature (TL)	217℃
	Time (tL)	60-150 seconds
Peak/Classification Temperature (Tp)		260℃

Time within 5℃ of Actual PeakTemperature (tp)	20-40 seconds
Ramp-Down Rate 6	6℃/second max.
Time 25℃ to Peak Temperature 8	8 minutes max.

8.1. RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB&PBDE content in accordance with directive 2002/95/EC(RoHS).

8.2. ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Revision History

Rev.	Date	Author(s)	Remark
1.0	5/9/2012	YMHUANG	Initial release
1.1	6/15/2012	YMHUANG	Change the serial resistance from 0 to 1K at 32.768K clock path
1.2	06/19/2012	YMHUANG	Updated application schematic to improve the GSM suppression