# BK7235 Datasheet

DS-BK7235-E05 V1.3

2023/11/17

# Contents

       DS-BK7235-E05 V1.3

# 1. Features

## Wi-Fi

- IEEE 802.11b/g/n/ax 1x1 compliant

- 20/40 MHz channel bandwidth for 2.4 GHz

- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)

- Supports Orthogonal Frequency Division Multiple Access (OFDMA)

- Supports Target Wake Time (TWT)

- TX and RX Low-Density Parity Check (LDPC) support for extended range

- WPA/WPA2/WPA3-Personal support for enhanced security

- Working modes: STA, AP, Direct

- Concurrent AP + STA

- TX power up to +20 dBm

- RX sensitivity -99 dBm

## Bluetooth Low Energy

- Bluetooth 5.2 Low Energy (LE)

- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)

- Supported Bluetooth Low Energy features: LE audio, 2 Mbps, advertising extensions, and long range

## Core

- 32-bit RISC-V MCU at up to 320 MHz:

    - 32 KB ITCM + 32 KB DTCM

    - 5-stage in-order execution pipeline

    - Hardware multiplier and divider

    - Branch prediction

    - Machine (M) and User (U) Privilege levels

    - Performance monitors

    - Misaligned memory accesses

    - Physical Memory Protection (PMP), 8 regions

    - RISC-V RV32I base integer instruction set

    - RISC-V "M" standard extension for integer multiplication and division

    – RISC-V "A" standard extension for atomic instructions

    – RISC-V "F" standard extensions for single-precision floating-point

    – RISC-V "C" standard extension for compressed instructions

    – DSP extension

    – RISC-V "N" standard extension for user-level interrupt and exception handing

    – Performance extension

    – CoDense extension

    – 3.57 CoreMark/MHz, 1.98 DMIPS/MHz

- UART Flash download

- Serial Wire Debug (SWD) interface

## Memory

- 4 MB SiP Flash

- SiP PSRAM: 4 MB or none

- 512 KB Share SRAM

- 64 KB ROM

- eFuse

## Security

- Isolated secure element (FIPS 140-2 Level 2 certified) with hardware cryptography

- Secure boot

- Unique ID and secure storage

- Secure update and anti-rollback

- Lifecycle management such as secure debug

- Flash encryption

- Cryptographic hardware acceleration:

    – Crypto accelerator: DES, AES-128/192/256, ChaCha20-128/256, SM4-128

    – Public key accelerator: ECDSA-P256/P384, RSA-2048/3072, SM2

    – Hash: SHA-224/256, SHA-384/512, HMAC, Poly1305, SM3-512

    – True Random Number Generator (TRNG)

- Key Derivation Function (KDF)

## Clock Management

- External oscillator: 26 MHz crystal oscillator (XTALH), 32.768 kHz crystal oscillator (XTALL)

- Internal oscillator: 32 kHz ring oscillator (ROSC), 26–360 MHz digitally controlled oscillator (DCO)

- 320/480 MHz PLL (DPLL)

- Audio PLL (APLL)

## Power Management

- 2.8 to 5.0 V VBAT supply

- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)

- Embedded buck (DC-DC) converter and LDO regulators

- Low power consumption:

    – Active mode RX: 85 mA

    – Active mode TX @ 17 dBm: 230 mA

    – Sleep mode: 238 μA

    – Deep sleep mode: 16 μA

    – Shutdown mode: 3.4 μA

## Peripherals

- 26 GPIOs

- 1x SPI

- 2x UART: 1 with Flash download support

- 1x I2C

- 1x CAN controller with CAN FD

- 1x general-purpose DMA controller (GDMA) with 12 channels

- 1x JPEG hardware encoder

- 1x JPEG hardware decoder

- 1x 8-bit CIS DVP interface

- 10x 32-bit PWM channel

- 13-bit AUX ADC, up to 5 channels

- 6x 32-bit general-purpose timer

- 2x watchdog timer (WDT)

- 1x real-time counter (RTC)

- 1x IrDA

- 1x temperature sensor

- 1x touch sensor, up to 14 touch sensing I/Os

## Packaging

- QFN40 package, 5 x 5 mm

- Operating temperature range: -40 up to +125 °C

## Applications

- Home appliance

    - Refrigerator

    - Air conditioner

    - Thermostat

    - Washing machine

    - Robot cleaner

- Smart plug

- Smart lighting

    - Light bulb

    - Light switch

    - Ceiling light

    - Stand light

- Others

    - Remote controller

    - Toy

    - Industrial terminal

    - Factory automation sensor/switch

    - Smart meter

    - Payment terminal

    - Industrial computer

    - Medical devices

    - Kitchen appliances

    - Home automation switch/sensor

# 2. Overview
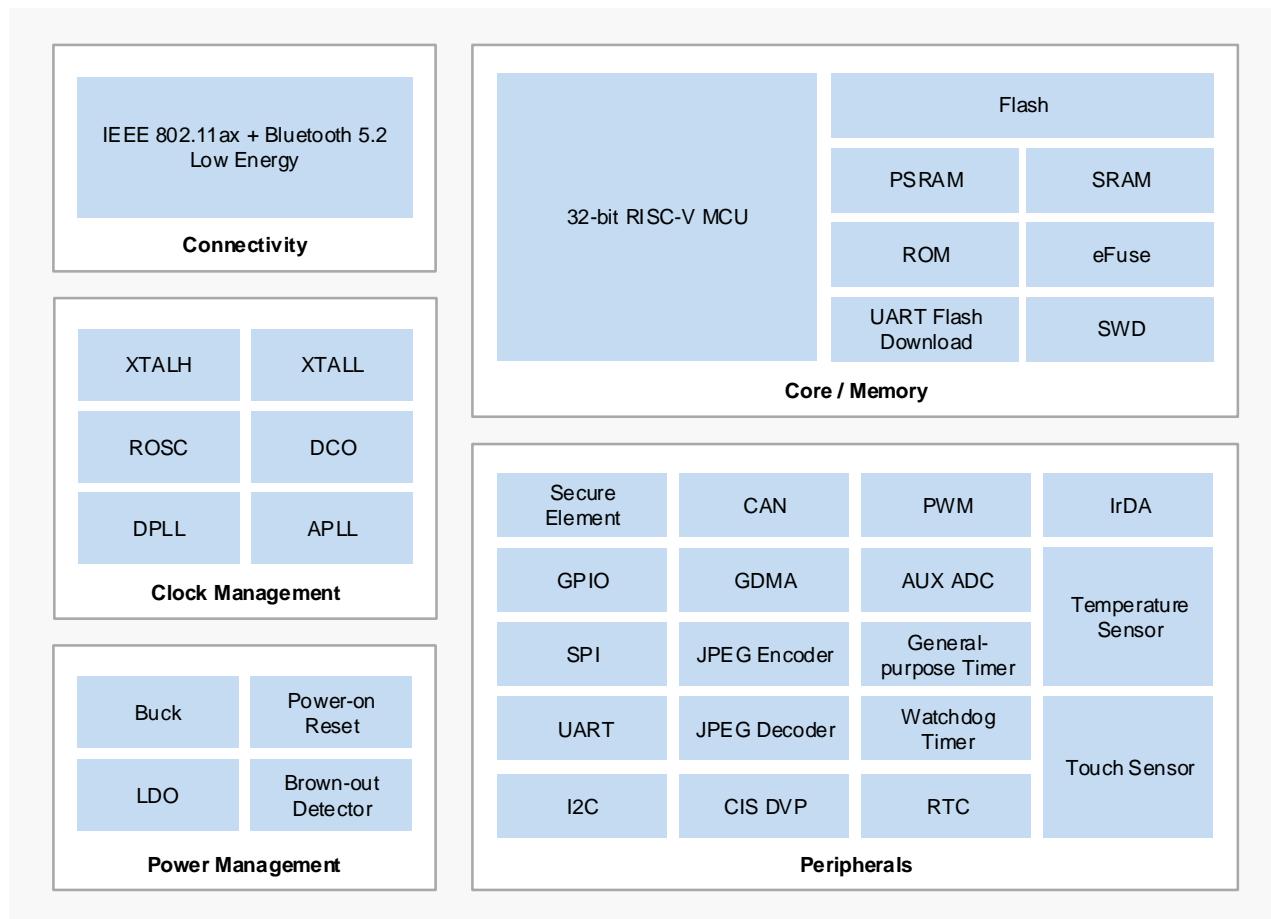
The BK7235 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth 5.2 Low Energy (LE) combo solution designed for applications that require high security and abundant resources. The integration of a 32-bit RISC-V MCU and a comprehensive set of peripherals makes the BK7235 ideal for advanced Internet of Things (IoT) applications.

The BK7235 provides state-of-the-art security based on a powerful security architecture. It offers an isolated and immutable platform root of trust to provide security services, such as secure boot and cryptographic operations, to applications running on a non-secure processing environment.

Using advanced design techniques and ultra-low power process technology, the BK7235 delivers high integration and minimal power consumption for smart lighting, smart home, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of BK7235.

**Figure 2-1 BK7235 Block Diagram**

# 3. Pin Descriptions

The BK7235 provides Wi-Fi and Bluetooth LE functionality in a 5 x 5 mm, 40-pin QFN package.

## 3.1 QFN40 Pin Descriptions

Figure 3-1 shows the pin assignments of the QFN40 package.

**Figure 3-1 QFN40 Pin Assignments**



Table 3-1 shows the pin descriptions of the QFN40 package.

**Table 3-1 QFN40 Pin Descriptions**

| Pin # | Name | I/O | Type | Description |
|-------|---------|-----|--------------|------------------------|
| 1 | VCCRXFE | - | Analog input | RF receiver power supply |

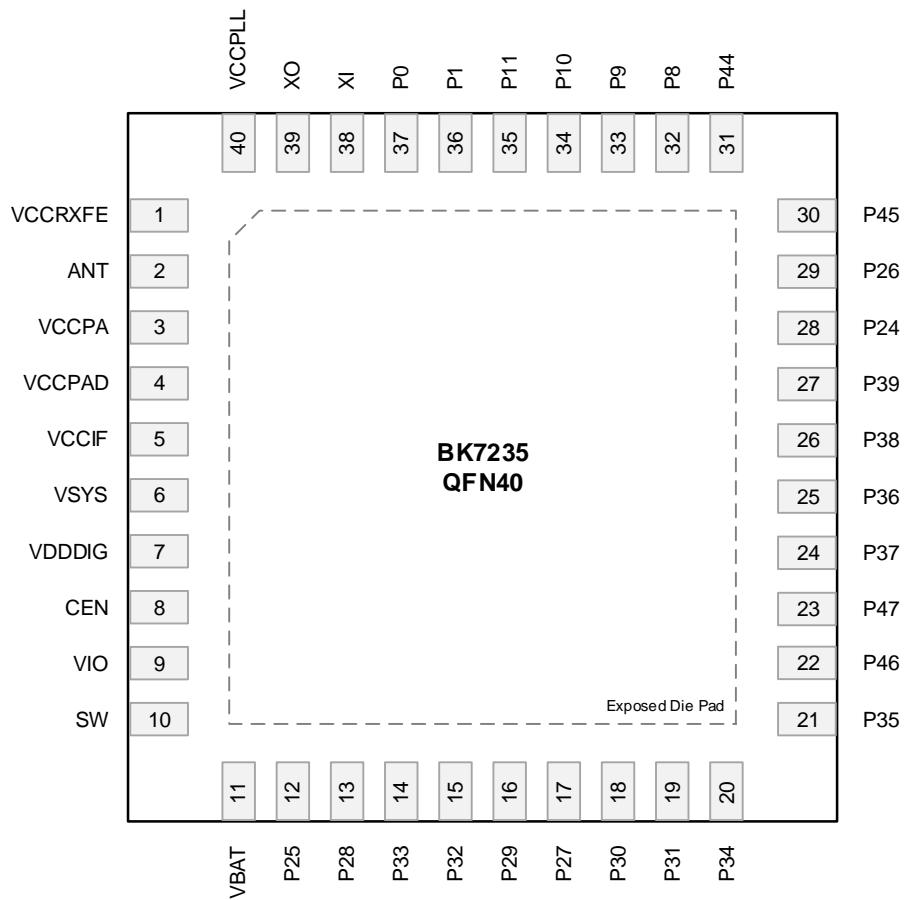| Pin # | Name | I/O | Type | Description |
|-------|------|-----|------|-------------|
| 2 | ANT | - | RF | 2.4 GHz RF signal port |
| 3 | VCCPA | - | Analog input | RF PA power supply |
| 4 | VCCPAD | - | Analog input | RF PA driver power supply |
| 5 | VCCIF | - | Analog input | IF power supply |
| 6 | VSYS | - | Analog output | System LDO output |
| 7 | VDDDIG | - | Analog output | Digital LDO output |
| 8 | CEN | - | Analog input | Chip enable, active high |
| 9 | VIO | - | Analog output | IO buck/LDO output |
| 10 | SW | - | Analog output | Buck switch output |
| 11 | VBAT | - | Power | Chip power supply |
| 12 | P25 | I/O | Digital/Analog | <ul><li>GPIO25: general-purpose I/O</li><li>IRDA: infrared data</li><li>PWM5 (differential with PWM4)</li><li>ADC1: analog input channel</li></ul> |
| 13 | P28 | I/O | Digital/Analog | <ul><li>GPIO28: general-purpose I/O</li><li>WIFI_RX_EN: Wi-Fi receive enable</li><li>I2S_MCLK: master clock</li><li>ADC4: analog input channel</li><li>TOUCH2: touch sensing I/O</li></ul> |
| 14 | P33 | I/O | Digital/Analog | <ul><li>GPIO33: general-purpose I/O</li><li>CIS_PXD1: data</li><li>PWM7 (differential with PWM6)</li><li>TOUCH7: touch sensing I/O</li><li>32K_XO: 32.768 kHz crystal output</li></ul> |
| 15 | P32 | I/O | Digital/Analog | <ul><li>GPIO32: general-purpose I/O</li><li>CIS_PXD0: data</li><li>PWM6 (differential with PWM7)</li><li>TOUCH6: touch sensing I/O</li><li>32K_XI: 32.768 kHz crystal input</li></ul> |
| 16 | P29 | I/O | Digital/Analog | <ul><li>GPIO29: general-purpose I/O</li><li>CIS_PCLK: pixel clock</li><li>TOUCH3: touch sensing I/O</li></ul> |

| Pin # | Name | I/O | Type | Description |
|-------|------|-----|------|-------------|
| 17 | P27 | I/O | Digital/Analog | <ul><li>GPIO27: general-purpose I/O</li><li>CIS_MCLK: master clock</li><li>CLK_AUXS: clock output derived from DCO/APLL/CLK_320M/CLK_480M</li></ul> |
| 18 | P30 | I/O | Digital/Analog | <ul><li>GPIO30: general-purpose I/O</li><li>CIS_HSYNC: horizontal synchronization</li><li>TOUCH4: touch sensing I/O</li></ul> |
| 19 | P31 | I/O | Digital/Analog | <ul><li>GPIO31: general-purpose I/O</li><li>CIS_VSYNC: vertical synchronization</li><li>TOUCH5: touch sensing I/O</li></ul> |
| 20 | P34 | I/O | Digital/Analog | <ul><li>GPIO34: general-purpose I/O</li><li>CIS_PXD2: data</li><li>PWM8 (differential with PWM9)</li><li>TOUCH8: touch sensing I/O</li></ul> |
| 21 | P35 | I/O | Digital/Analog | <ul><li>GPIO35: general-purpose I/O</li><li>CIS_PXD3: data</li><li>PWM9 (differential with PWM8)</li><li>TOUCH9: touch sensing I/O</li></ul> |
| 22 | P46 | I/O | Digital/Analog | <ul><li>GPIO46: general-purpose I/O</li><li>CAN_STBY: transceiver standby mode (active high)</li><li>SPI0_MOSI: master out slave in</li><li>TOUCH14: touch sensing I/O</li></ul> |
| 23 | P47 | I/O | Digital/Analog | <ul><li>GPIO47: general-purpose I/O</li><li>SPI0_MISO: master in slave out</li><li>TOUCH15: touch sensing I/O</li></ul> |
| 24 | P37 | I/O | Digital/Analog | <ul><li>GPIO37: general-purpose I/O</li><li>CIS_PXD5: data</li><li>PWM11 (differential with PWM10)</li><li>TOUCH11: touch sensing I/O</li></ul> |
| 25 | P36 | I/O | Digital/Analog | <ul><li>GPIO36: general-purpose I/O</li><li>CIS_PXD4: data</li><li>PWM10 (differential with PWM11)</li><li>TOUCH10: touch sensing I/O</li></ul> |

| Pin # | Name | I/O | Type | Description |
|-------|------|-----|------|-------------|
| 26 | P38 | I/O | Digital/Analog | • GPIO38: general-purpose I/O<br>• CIS_PXD6: data<br>• TOUCH12: touch sensing I/O |
| 27 | P39 | I/O | Digital/Analog | • GPIO39: general-purpose I/O<br>• CIS_PXD7: data<br>• TOUCH13: touch sensing I/O |
| 28 | P24 | I/O | Digital/Analog | • GPIO24: general-purpose I/O<br>• LPO_CLK: 32 kHz clock output<br>• PWM4 (differential with PWM5)<br>• ADC2: analog input channel |
| 29 | P26 | I/O | Digital | • GPIO26: general-purpose I/O<br>• WIFI_TX_EN: Wi-Fi transmit enable |
| 30 | P45 | I/O | Digital/Analog | • GPIO45: general-purpose I/O<br>• CAN_RX: receive<br>• SPI0_CSN: chip select<br>• ADC11: analog input channel |
| 31 | P44 | I/O | Digital/Analog | • GPIO44: general-purpose I/O<br>• CAN_TX: transmit<br>• SPI0_SCK: serial clock<br>• ADC10: analog input channel |
| 32 | P8 | I/O | Digital | • GPIO8: general-purpose I/O<br>• PWM2 (differential with PWM3) |
| 33 | P9 | I/O | Digital | • GPIO9: general-purpose I/O<br>• PWM3 (differential with PWM2) |
| 34 | P10 | I/O | Digital | • GPIO10: general-purpose I/O<br>• DL_UART_RX: UART Flash download receive data input<br>• UART0_RX: receive data input<br>• CLK_AUXS: clock output derived from DCO/APLL/CLK_320M/CLK_480M |
| 35 | P11 | I/O | Digital | • GPIO11: general-purpose I/O<br>• DL_UART_TX: UART Flash download transmit data output<br>• UART0_TX: transmit data output |

| Pin # | Name | I/O | Type | Description |
|-------|------|-----|------|-------------|
| 36 | P1 | I/O | Digital | • GPIO1: general-purpose I/O<br>• UART1_RX: receive data input<br>• I2C1_SDA: serial data<br>• SWDIO: serial wire data |
| 37 | P0 | I/O | Digital | • GPIO0: general-purpose I/O<br>• UART1_TX: transmit data output<br>• I2C1_SCL: serial clock<br>• SWCLK: serial wire clock |
| 38 | XI | - | Analog input | 26 MHz crystal input |
| 39 | XO | - | Analog output | 26 MHz crystal output |
| 40 | VCCPLL | - | Analog input | RF PLL power supply |
| Die pad | GND_SLUG | - | GND | Ground |

# 3.2 Pin Multiplexing

Table 3-2 shows the pin mux functions of GPIOs.

**Table 3-2 Pin Multiplexing**

| GPIO | Flash Download<br><br>UART | Alternate Functions | | | |
|------|-----------------|---------------------------------------------------------------------|------------------------------|----------------------------|--------|
| | | AF1<br><br>UART1/UART0/<br>Clock/IrDA/<br>Wi-Fi TX/RX Enable/<br>CIS DVP/CAN | AF2<br><br>I2C1/PWM/<br>Clock/SPI0 | AF3<br><br>SWD/Clock/<br>AUX ADC | AF4<br><br>TOUCH |
| GPIO0 | | UART1_TX | I2C1_SCL | SWCLK | |
| GPIO1 | | UART1_RX | I2C1_SDA | SWDIO | |
| GPIO8 | | | PWM2 | | |
| GPIO9 | | | PWM3 | | |
| GPIO10 | DL_UART_RX | UART0_RX | | CLK_AUXS | |
| GPIO11 | DL_UART_TX | UART0_TX | | | |
| GPIO24 | | LPO_CLK | PWM4 | ADC2 | |
| GPIO25 | | IRDA | PWM5 | ADC1 | |

| GPIO | Flash Download | Alternate Functions | | | |
|---|---|---|---|---|---|
| | | AF1 | AF2 | AF3 | AF4 |
| | UART | UART1/UART0/ Clock/IrDA/ Wi-Fi TX/RX Enable/ CIS DVP/CAN | I2C1/PWM/ Clock/SPI0 | SWD/Clock/ AUX ADC | TOUCH |
| GPIO26 | | WIFI_TX_EN | | | |
| GPIO27 | | CIS_MCLK | CLK_AUXS | | |
| GPIO28 | | WIFI_RX_EN | I2S_MCLK | ADC4 | TOUCH2 |
| GPIO29 | | CIS_PCLK | | | TOUCH3 |
| GPIO30 | | CIS_HSYNC | | | TOUCH4 |
| GPIO31 | | CIS_VSYNC | | | TOUCH5 |
| GPIO32 | | CIS_PXD0 | PWM6 | | TOUCH6 |
| GPIO33 | | CIS_PXD1 | PWM7 | | TOUCH7 |
| GPIO34 | | CIS_PXD2 | PWM8 | | TOUCH8 |
| GPIO35 | | CIS_PXD3 | PWM9 | | TOUCH9 |
| GPIO36 | | CIS_PXD4 | PWM10 | | TOUCH10 |
| GPIO37 | | CIS_PXD5 | PWM11 | | TOUCH11 |
| GPIO38 | | CIS_PXD6 | | | TOUCH12 |
| GPIO39 | | CIS_PXD7 | | | TOUCH13 |
| GPIO44 | | CAN_TX | SPI0_SCK | ADC10 | |
| GPIO45 | | CAN_RX | SPI0_CSN | ADC11 | |
| GPIO46 | | CAN_STBY | SPI0_MOSI | | TOUCH14 |
| GPIO47 | | | SPI0_MISO | | TOUCH15 |

# 4. Functional Description

## 4.1 Wi-Fi/Bluetooth Transceiver

The BK7235 integrates a high-performance Wi-Fi/Bluetooth transceiver. The incorporated low noise amplifier (LNA) amplifies the single-ended inputs and converts the amplified signals into differential outputs to achieve a better noise and linearity trade-off. On the transmit side, the differential outputs of the power amplifier (PA) are combined and converted to single-ended outputs using the on-chip balun, enabling transmit and receive operations with only one ANT pin connected to the antenna. The communication range can be extended by configuring GPIO26 and GPIO28 as TX_EN and RX_EN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

## 4.2 Clock Management

The primary clock sources available in the BK7235 are as follows:

- High-frequency clocks

    - 26 MHz crystal oscillator: it outputs clock signal XTALH

    - 26–360 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO

    - Digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M

- Low-frequency clocks

    - 32.768 kHz crystal oscillator: it outputs clock signal XTALL

    - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC

- Audio clock

    - Audio PLL (APLL): its default frequency is 98.304 MHz, and it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32.768 kHz crystal oscillator XTALL

- 32 kHz clock signal derived from 26 MHz crystal oscillator

- 32 kHz internal oscillator ROSC

The BK7235 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- LPO_CLK: LPO_CLK clock

- CLK_AUXS: clock derived from DCO/APLL/CLK_320M/CLK_480M

- I2S_MCLK: reference clock for external audio codec, derived from APLL

- CIS_MCLK: reference clock for external CMOS image sensor (CIS)

# 4.3 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

System power-on reset, digital power-on reset, and watchdog reset have the same reset effect on all blocks, except for the always-on logic. Any of these resets can reset the whole chip to its initial state. The always-on logic has a 32-bit timer and 16-bit retention registers, which can only be reset to initial values by a system power-on reset.

Wake-up from either shutdown mode or deep sleep mode will power on digital from power-down mode, which triggers the whole system reset procedure.

# 4.4 Power Management
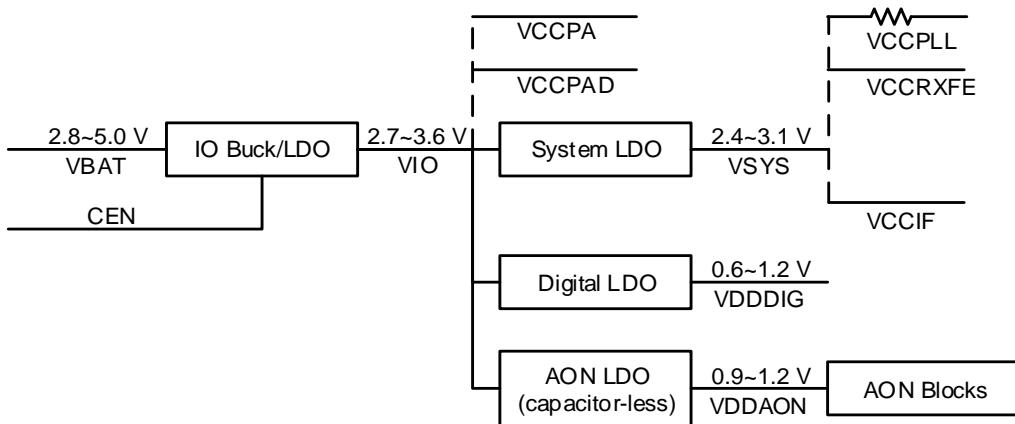
## 4.4.1 Power Scheme

The power management system on the BK7235 includes a buck converter and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

The VBAT is the external main chip supply ranging from 2.8 to 5.0 V. The VBAT generates VIO through the IO buck converter or the IO LDO regulator (default). In addition to being the power supply for Wi-Fi PA, VIO is also the input supply of other LDOs. These LDOs generate the following main power supplies:

- VSYS: power supply for RF/analog modules. It is externally connected to VCCPLL/VCCRXFE/VCCIF to supply power to Wi-Fi/Bluetooth transceiver, and internally provides power supply to DPLL, XTAL, and AUX ADC directly.

- VDDDIG: power supply for digital logic. It provides power supply for the processor, memory, Wi-Fi and Bluetooth baseband, as well as various peripherals.

- VDDAON: power supply for always-on (AON) logic. The AON logic, such as GPIOs, AON watchdog, RTC, and control logic of deep sleep wake-up, keeps working in deep sleep mode (VDDDIG off).
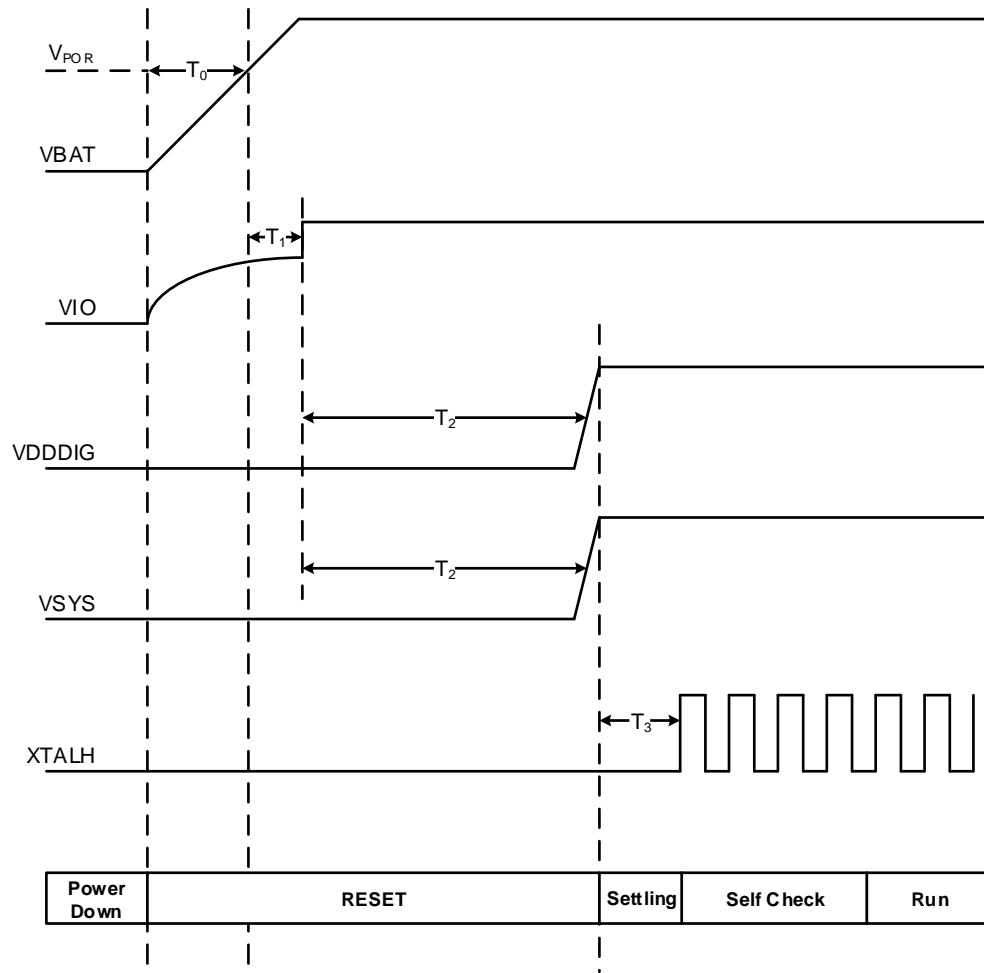
Figure 4-1 shows the power distribution of BK7235.

**Figure 4-1 Internal Power Distribution**



**Note:** For buck mode, it is recommended that the VBAT voltage be greater than 3.6 V.

**Note:** Outputs from the buck converter and LDO regulators require proper bypass capacitors to reduce supply noise.

Figure 4-2 shows the power-up sequence of BK7235.

**Figure 4-2 BK7235 Power-up Sequence**



**Table 4-1 Timing Parameters of Power-up Sequence**

| Parameter | Description | Min. | Typ. | Max. | Unit |
|-----------|-------------|------|------|------|------|
| $V_{POR}$ | VBAT POR threshold | 2.5 | 2.65 | 2.8 | V |
| $T_0$ | VBAT ready time | 200 | - | - | μs |
| $T_1$ | IO LDO output ready time | - | 150 | 300 | μs |
| $T_2$ | Digital/system LDO output ready time | - | 5 | 10 | ms |
| $T_3$ | XTALH stable time | - | 250 | 500 | μs |

## 4.4.2 Power Modes

The BK7235 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

**Shutdown Mode:** All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

**Deep Sleep Mode:** All circuits are powered down except the AON logic. GPIO interrupts, RTC interrupts, or touch sensing I/O pins can power up the system again. Retention registers can keep their contents.

**Sleep Mode:** The MCU and all digital logic stop their clocks, and their power supply decreases to a much lower retention voltage, which results in a much lower current. GPIO interrupts, RTC interrupts, touch sensing I/O pins, or interrupts triggered by Wi-Fi/Bluetooth MAC low-power counters can bring the system back to active mode with normal voltage.

**Active Mode:** The MCU is active, and all peripherals are available.

# 4.5 General-purpose I/Os (GPIO)

The BK7235 has up to 26 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions. Table 3-2 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
    - High or low level
    - Rising or falling edge

# 4.6 SPI Interface (SPI)

The BK7235 integrates an SPI interface that can operate in master or slave mode. The SPI interface allows a clock frequency up to 30 MHz in both master and slave modes.

The SPI interface supports the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase

- Programmable data order with MSB-first or LSB-first shifting

- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

# 4.7 UART Interface (UART)

The BK7235 includes two universal asynchronous receiver/transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 2 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)

- Even, odd, or none parity check

- Programmable stop bits (1 or 2 bits)

- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.

- Flash download (UART0)

# 4.8 I2C Interface (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7235 embeds an I2C interface, which can operate in master or slave mode.

The features of the I2C interface are listed below:

- Master and slave modes

- Standard mode (up to 100 kbps)

- Fast mode (up to 400 kbps)

- 7-bit and 10-bit addressing

- Bus idle and SCL low timeout condition detection

# 4.9 CAN Controller (CAN)

The BK7235 embeds a Controller Area Network (CAN) controller that uses the basic CAN principle and meets all constraints of the CAN-specification 2.0B active. Furthermore, the CAN controller can be configured to meet the specification of CAN with flexible data rate CAN FD. CAN 2.0 carries a data payload up to 8 bytes and CAN FD up to 64 bytes.

The CAN controller supports two operating modes, normal and standby, which can be selected via the CAN_STBY pin. If a high level is applied to the CAN_STBY pin, the external transceiver enters the standby mode.

# 4.10 GDMA Controller (GDMA)

The BK7235 has a general-purpose DMA controller (GDMA) with 12 DMA channels to unload CPU activity. The 12 channels are shared by peripherals that have DMA capabilities.

The GDMA controller can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). It allows peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

A selection of peripherals on the BK7235 have DMA capabilities, including UART0, SPI0, UART1, and JPEG encoder.

# 4.11 JPEG Encoder/Decoder

The BK7235 includes a JPEG encoder and decoder for encoding and decoding JPEG streams. The JPEG encoder provides a small hardware compressor for JPEG images, while the decoder provides a decompression accelerator for JPEG images. Additionally, the JPEG encoder supports up to 32 programmable quantization tables.

# 4.12 CMOS Image Sensor Interface (CIS)

The CMOS Image Sensor (CIS) Digital Video Port (DVP) interface provides an 8-bit parallel interface to sensors, together with main clock (MCLK), pixel clock (PCLK), horizontal SYNC (HSYNC), and vertical SYNC (VSYNC) signals.

The input from the YUV sensor is directly fed to the hardware JPEG encoder, and the output of the JPEG encoder is directly written to the data memory by a dedicated DMA channel.

The CIS interface features include:

- 8-bit parallel interface
- Programmable polarity for pixel clock and synchronization signals
- Crop feature
- Data formats supported:
    - YCbCr 4:2:2 (YUYV, UYVY, YYUV, and UVYY)
    - RGB565

# 4.13 PWM Group (PWMG)

The BK7235 has two PWM groups, PWMG0 and PWMG1. Each PWMG includes maximum six 32-bit up-counters driven by three 8-bit programmable prescalers.

Each PWMG module provides three pairs of PWM channels at most. Each channel can work independently (arbitrary waveform configuration), or two channels can be paired (waveforms completely opposite, timing aligned).

The main features of the PWMGs are listed here:

- 32-bit up counter

- The counter increases in one direction and automatically continues counting from 0 when it overflows to the maximum value.

- Fixed PWM base frequency with 8-bit programmable prescaler (factor between 1 and 256)

- Four channels for PWMG0 and six channels for PWMG1

- Each channel supports four modes:
    - PWM mode
    - Timer mode
    - Counter mode
    - Capture mode

- Each channel can be enabled individually, and the mode of each channel can be configured individually.

- Configurable PWM period and duty cycle for each PWM channel

- Capable of continuous counting between two rising edges, two falling edges, or any two edges in capture mode

- The real-time count value can be read in timer mode.

# 4.14 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 13-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 12.5 kHz to 650 kHz

- 13-bit resolution

- Up to five external analog input channels: ADC1/2/4/10/11

- Four internal dedicated channels:
    - VBAT monitoring channel (VBAT*0.4), connected to ADC0
    - Internal temperature sensor (TEMP), connected to ADC7
    - TSSIO, connected to ADC8
    - Touch OUT_TD, connected to ADC9

- Conversion modes:
    - One-shot mode
    - Software control mode
    - Continuous mode

# 4.15 Timer Group (TIMG)

The BK7235 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

# 4.16 Watchdog Timers (WDT)

The BK7235 has two watchdog timers, the main domain watchdog timer (DWDT) and the always-on domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz LPO_CLK clock (factor 2/4/8/16) and has a maximum programmable period up to 32.768 ($2^{16}/2$ kHz) seconds. The AWDT runs on the ROSC and has a maximum programmable period up to 65.536 ($2^{16}/1$ kHz) seconds.

# 4.17 Real-Time Counter (RTC)

The real-time counter (RTC) module features a 32-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

# 4.18 IrDA Interface (IrDA)

The BK7235 embeds a hardware IrDA interface to encode and decode signals. In addition, the interface has a capture timer capability that allows software decoding of the input signal.

The IrDA has the following features:

- Single-duplex mode

- Carrier modulation for transmission

- Integrated 512-byte RX FIFO and 512-byte TX FIFO

## 4.19 Temperature Sensor

The BK7235 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results from the sensor can be read by the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

## 4.20 Touch Sensor (TOUCH)

The BK7235 has up to 14 capacitive sensing I/Os, which immediately detect capacitance changes induced by touch or proximity of objects.

## 4.21 Secure Element

The BK7235 provides state-of-the-art security based on a powerful security architecture. It offers platform Root of Trust (RoT) based on an isolated Secure Element (SE). SE is a module that protects valuable assets, such as secret keys for embedded security sensitive applications in a Trusted Execution Environment (TEE). Using a dedicated hardware module increases security level and performance compared to a cryptographic software library.

The eFuse, ROM, and other memories inside SE allow for the secure storage of key material and other security sensitive data (assets). With functions including key derivation, non-volatile countermanagement, secure storage, asset management, and a variety of cipher and hash operations, SE acts as a vault within the embedded system. The assets are referenced by authorized users, which increases security and prevents unauthorized use and abuse.

SE embeds hardware implementations of cryptographic algorithms that support various operations and modes required by applications in a TEE.

The SE inside BK7235 is FIPS 140-2 Level 2 certified and supports all security features required for FIPS 140-2 Level 2 certification. It embeds the following algorithms:

- RSA, ECDSA

- DRBG

- Triple-DES (ECB, CBC)

- AES (ECB, CBC, CTR, XTS)

- AES-CCM, AES-CMAC

- HMAC, SHS for SHA-1, SHA-224/256, and SHA-384/512

- SM2, SM3, SM4

- Poly1305, Chacha20

- KDF

## Asset Store

The Asset Store is a securely managed memory that can store sensitive security parameters. The memory is on-chip SRAM embedded in the SE.

- Employs a safe-deposit box system that only allows asset use according to the associated ownership and policy of the asset

- Ownership keeps assets from different applications and different Hosts separated:

  – CPU Identity: 2-bit and 1-bit Normal/Secure world

  – Application Identity: 32 bits

  – Application Long-term Identity: 33 up to 224 bytes

- Root Key based security via eFuse interface

- Supports symmetric and asymmetric key storage and export using AES SIV key-blobs

- Symmetric key generation and derivation using NIST SP 800-108 algorithm:

  – Derive a KDK from a Root Key

  – Derive a KEK from a Root Key

  – Derive a Key Asset from a KDK

- Shared secret generation based on asymmetric key exchange

- KDF NIST SP 800-56A & B, HMAC and CMAC based

- Key derivation according to NIST SP 800-135. Authentication allows access control to assets.

- Authorization based on authentication state

## Timers

- Time stamping of keys

- Key lifetime and access window management based on timestamp

- Functions are based on hardware timers in a dedicated clock domain.

## True Random Number Generator (TRNG)

- FIPS 140-2&3/SP 800-90 compliant

- Hardware-based, non-deterministic RNG

- Used to internally generate session keys, IVs, nonces, cookies, public and private keys

- Random Number Generation using SP 800-90 NRBG, SHA-2 conditioning, and AES-256 CTR_DRBG

## Public Key Accelerator

- Hardware accelerated public key operations for secure boot using ECDSA-P384

- Signing and verifying using RSA-PSS, RSA-PKCS#1.5, and ECDSA

- Basic operations for DH, DSA, ECDSA, RSA, and SM2, including:

  - ECDH

  - ECDSA-P256 and ECDSA-P384

  - RSA-1024, RSA-2048, RSA-3072, and Curve25519 support

  - SM2

## Crypto Algorithms

- DES, TDES

  - ECB, CBC

- AES

  - ECB, CBC, CTR, ICM, f8, XTS

  - CMAC, CCM, GCM

  - Wrap and unwrap (NIST SP800-38F)

  - Key lengths: 128, 192 and 256 bits

- ChaCha20

  - Key lengths: 128 and 256 bits

- SM4

  - Key length: 128 bits

## Hash Algorithms

- Basic hash and HMAC modes

  - MD5

  - SHA-1

  - SHA-224 and SHA-256

  - SHA-384 and SHA-512

&ndash; Poly1305

&ndash; SM3-512

## Management of Non-Volatile Assets

- Root of Trust

- Provisioning/personalization

- Monotonic counters:

  &ndash; Short monotonic counters can be stored internally in eFuse (up to 127 states) and can be used for host firmware version numbering or other infrequently updated counters.

  &ndash; Long monotonic counters must be stored externally in non-volatile system memory.

- Private to the crypto module, read and write access

## Secure Debug

- Enables host system level secure debugging

- Bits can be enabled/disabled under the control of public key cryptography.

## Secure Boot

- Image decryption:

  &ndash; AES-CBC or AES-CTR depending on the use case

- Image signature verification:

  &ndash; ECDSA NIST P-256/384

  &ndash; SHA-256

- Helper functions:

  &ndash; Symmetric key generation

  &ndash; Key derivation

  &ndash; AES wrap

## Embedded Controller

- Flexibility through programmability

- ROM-based firmware program memory ensures system security.

## Host Command Interface

- Token-based command interface

- Four separate mailboxes for commands

- The commands and results of Normal (Non-secure) and Secure world are separated and cannot be accessed by the other world.

# 5. Electrical Characteristics

## 5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

| Parameter | Description | Min. | Max. | Unit |
|-----------|-------------|------|------|------|
| VBAT | Battery regulator supply voltage | -0.3 | 5.8 | V |
| VIO | IO buck/LDO output voltage | -0.3 | 3.6 | V |
| VCCPA | Supply voltage for PA | -0.3 | 3.6 | V |
| VCCPAD | Supply voltage for PA driver | -0.3 | 3.6 | V |
| VSYS | System LDO output voltage | -0.3 | 3.6 | V |
| VCCIF | Supply voltage for IF | -0.3 | 3.6 | V |
| VCCRXFE | Supply voltage for RX | -0.3 | 3.6 | V |
| VCCPLL | Supply voltage for RF PLL | -0.3 | 3.6 | V |
| VDDDIG | Digital LDO output voltage | -0.3 | 1.3 | V |
| $P_{RX}$ | RX input power | - | 10 | dBm |
| $T_{STR}$ | Storage temperature range | -55 | 150 | ℃ |

## 5.2 ESD Ratings

| Parameter | Description | Test Condition | Value | Unit |
|-----------|-------------|----------------|-------|------|
| ESD HBM | Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001-2017 | ANT pin | ±3000 | V |
| | | Other pins | ±4000 | V |
| ESD CDM | Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002-2018 | All pins | ±1000 | V |

# 5.3 Recommended Operating Conditions

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VBAT | Battery regulator supply voltage | 2.8 | 3.3 | 5.0 | V |
| VIO | IO buck/LDO output voltage | 2.7 | - | 3.6 | V |
| VCCPA | Supply voltage for PA | 2.7 | - | 3.6 | V |
| VCCPAD | Supply voltage for PA driver | 2.7 | - | 3.6 | V |
| VSYS | System LDO output voltage | 2.4 | - | 3.1 | V |
| VCCIF | Supply voltage for IF | 2.4 | - | 3.1 | V |
| VCCRXFE | Supply voltage for RX | 2.4 | - | 3.1 | V |
| VCCPLL | Supply voltage for RF PLL | 2.2 | - | 2.9 | V |
| VDDDIG | Digital LDO output voltage | 0.6 | 1.15 | 1.2 | V |
| $T_{OPR}$ | Operating temperature range | -40 | - | 125 | ℃ |

# 5.4 Digital I/O Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VIH | High-level input voltage | P0/P1/P10/P11 | 0.7 VBAT | - | VBAT + 0.3 | V |
| | | Other digital I/Os | 0.7 VIO | - | VIO + 0.3 | V |
| VIL | Low-level input voltage | P0/P1/P10/P11 | -0.3 | - | 0.3 VBAT | V |
| | | Other digital I/Os | -0.3 | - | 0.3 VIO | V |
| VOH | High-level output voltage | P0/P1/P10/P11 | 0.9 VBAT | - | - | V |
| | | Other digital I/Os | 0.9 VIO | - | - | V |
| VOL | Low-level output voltage | P0/P1/P10/P11 | - | - | 0.1 VBAT | V |
| | | Other digital I/Os | - | - | 0.1 VIO | V |
| $I_{DRV}$ | I/O output drive strength | - | 5 | - | 20 | mA |
| $R_{PU}$ | Weak pull-up resistor | - | - | 40 | - | kΩ |
| $R_{PD}$ | Weak pull-down resistor | - | - | 44 | - | kΩ |

## 5.5 IO Buck/LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Output voltage | IO buck/LDO output voltage | 2.7 | 3.3 | 3.6 | V |
| Load current | - | - | - | 500 | mA |
| Startup current | - | - | - | 5 | mA |
| Switching frequency | Buck modulation frequency | 0.5 | 1 | 2 | MHz |
| Output filter capacitor capacitance | - | - | 4.7 | - | μF |
| Inductor inductance | - | - | 4.7 | - | μH |
| Inductor DC resistance | - | - | - | 500 | mΩ |
| Inductor saturation current | - | 500 | - | - | mA |

## 5.6 System LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VSYS | System LDO output voltage | 2.4 | 2.8 | 3.1 | V |
| Load current | - | - | - | 200 | mA |

## 5.7 Digital LDO

| Parameter | Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VDDDIG | Digital LDO output voltage | 0.6 | 1.15 | 1.2 | V |
| Load current | - | - | - | 150 | mA |

## 5.8 26 MHz Crystal Characteristics

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| F0 | Nominal Frequency | - | - | 26 | - | MHz |
| ΔF/F0 | Frequency tolerance | 25 ℃ | -10 | - | +10 | ppm |
| TC | | -40 to 105 ℃ crystal | -20 | - | +20 | ppm |

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | Frequency stability over operating temperature | -30 to 85 ℃ crystal | -10 | - | +10 | ppm |
| CL | Load capacitance | - | 7 | 7.3 | 9 | pF |
| TS | Trim sensitivity | -40 to 105 ℃ crystal | - | 32 | - | ppm/pF |
| | | -30 to 85 ℃ crystal | - | 17 | - | ppm/pF |

# 5.9 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Active Mode** | | | | | |
| RX current | 11b: 11 Mbps DSSS | - | 86 | - | mA |
| | 11g: 54 Mbps OFDM | - | 85 | - | mA |
| | 11n: MCS7, HT20 | - | 85 | - | mA |
| | 11n: MCS7, HT40 | - | 110 | - | mA |
| | 11ax: MCS7, HE20 | - | 89 | - | mA |
| TX current | 11b: 11 Mbps DSSS @ 17 dBm | - | 230 | - | mA |
| | 11g: 54 Mbps OFDM @ 15 dBm | - | 220 | - | mA |
| | 11n: MCS7, HT20 @ 14 dBm | - | 210 | - | mA |
| | 11n: MCS7, HT40 @ 14 dBm | - | 230 | - | mA |
| | 11ax: MCS7, HE20 @ 14 dBm | - | 215 | - | mA |
| **Sleep Mode** | | | | | |
| Sleep | CPU halted, Wi-Fi MAC halted, Wi-Fi PHY off, Bluetooth off, multimedia (video) off, encryption off, SMEM3 off, XTALH off, VDDDIG=0.6 V | - | 238 | - | µA |
| Deep sleep | Only the AON domain is active. | - | 16 | - | µA |
| **Shutdown Mode** | | | | | |
| Shutdown | The chip is entirely powered off. | - | 3.4 | - | µA |

# 5.10 WLAN RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2412 | - | 2484 | MHz |
| **Sensitivity** | | | | | |
| Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU) | 1 Mbps DSSS | - | -99 | - | dBm |
| | 2 Mbps DSSS | - | -95 | - | dBm |
| | 5.5 Mbps DSSS | - | -93 | - | dBm |
| | 11 Mbps DSSS | - | -88 | - | dBm |
| Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU) | 6 Mbps OFDM | - | -91 | - | dBm |
| | 9 Mbps OFDM | - | -90 | - | dBm |
| | 12 Mbps OFDM | - | -89 | - | dBm |
| | 18 Mbps OFDM | - | -87 | - | dBm |
| | 24 Mbps OFDM | - | -83 | - | dBm |
| | 36 Mbps OFDM | - | -80 | - | dBm |
| | 48 Mbps OFDM | - | -76 | - | dBm |
| | 54 Mbps OFDM | - | -75 | - | dBm |
| Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC) | HT20, MCS0 | - | -91 | - | dBm |
| | HT20, MCS1 | - | -88 | - | dBm |
| | HT20, MCS2 | - | -86 | - | dBm |
| | HT20, MCS3 | - | -82 | - | dBm |
| | HT20, MCS4 | - | -80 | - | dBm |
| | HT20, MCS5 | - | -75 | - | dBm |
| | HT20, MCS6 | - | -74 | - | dBm |
| | HT20, MCS7 | - | -73 | - | dBm |
| Sensitivity - IEEE 802.11n, 40 MHz | HT40, MCS0 | - | -87 | - | dBm |
| | HT40, MCS1 | - | -84 | - | dBm |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| (10% PER for 4096 octet PSDU, LDPC) | HT40, MCS2 | - | -83 | - | dBm |
| | HT40, MCS3 | - | -79 | - | dBm |
| | HT40, MCS4 | - | -77 | - | dBm |
| | HT40, MCS5 | - | -72 | - | dBm |
| | HT40, MCS6 | - | -71 | - | dBm |
| | HT40, MCS7 | - | -69 | - | dBm |
| Sensitivity - IEEE 802.11ax, 20 MHz  (10% PER for 4096 octet PSDU, LDPC) | HE20, MCS0 | - | -90 | - | dBm |
| | HE20, MCS1 | - | -87 | - | dBm |
| | HE20, MCS2 | - | -85 | - | dBm |
| | HE20, MCS3 | - | -81 | - | dBm |
| | HE20, MCS4 | - | -79 | - | dBm |
| | HE20, MCS5 | - | -74 | - | dBm |
| | HE20, MCS6 | - | -73 | - | dBm |
| | HE20, MCS7 | - | -72 | - | dBm |
| Sensitivity - IEEE 802.11ax, 40 MHz  (10% PER for 4096 octet PSDU, LDPC) | HE40, MCS0 | - | -86 | - | dBm |
| | HE40, MCS1 | - | -83 | - | dBm |
| | HE40, MCS2 | - | -81 | - | dBm |
| | HE40, MCS3 | - | -77 | - | dBm |
| | HE40, MCS4 | - | -75 | - | dBm |
| | HE40, MCS5 | - | -71 | - | dBm |
| | HE40, MCS6 | - | -70 | - | dBm |
| | HE40, MCS7 | - | -69 | - | dBm |
| **Maximum Receive Level** | | | | | |
| Maximum receive level @ 2.4 GHz | 11b: 1, 2 Mbps (8% PER, 1024 octets) | - | 10 | - | dBm |
| | 11b: 5.5, 11 Mbps (8% PER, 1024 octets) | - | 10 | - | dBm |
| | 11g: 6–54 Mbps (10% PER, 1000 octets) | - | 0 | - | dBm |

| Parameter | Condition | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | 11n: MCS0–7 (10% PER, 4096 octets) | | - | 0 | - | dBm |
| | 11ax: MCS0–7 (10% PER, 4096 octets) | | - | 0 | - | dBm |
| **Adjacent Channel Rejection** | | | | | | |
| Adjacent channel (±30 MHz) rejection - IEEE 802.11b<br><br>(8% PER for 1024 octet PSDU with desired signal level as specified in Condition) | 1 Mbps DSSS | -74 dBm | - | 42 | - | dB |
| | 2 Mbps DSSS | -74 dBm | - | 51 | - | dB |
| Adjacent channel (±25 MHz) rejection - IEEE 802.11b<br><br>(8% PER for 1024 octet PSDU with desired signal level as specified in Condition) | 5.5 Mbps DSSS | -70 dBm | - | 47 | - | dB |
| | 11 Mbps DSSS | -70 dBm | - | 41 | - | dB |
| Adjacent channel (±25 MHz) rejection - IEEE 802.11g<br><br>(10% PER for 1000 octet PSDU with desired signal level as specified in Condition) | 6 Mbps OFDM | -79 dBm | - | 44 | - | dB |
| | 54 Mbps OFDM | -62 dBm | - | 26 | - | dB |
| Adjacent channel (±25 MHz) rejection - IEEE 802.11n<br><br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HT20, MCS0 | -79 dBm | - | 44 | - | dB |
| | HT20, MCS7 | -61 dBm | - | 24 | - | dB |
| Adjacent channel (±40 MHz) rejection - IEEE 802.11n<br><br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HT40, MCS0 | -76 dBm | - | 39 | - | dB |
| | HT40, MCS7 | -58 dBm | - | 18 | - | dB |
| Adjacent channel (±20 MHz) rejection - IEEE 802.11ax<br><br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HE20, MCS0 | -79 dBm | - | 45 | - | dB |
| | HE20, MCS7 | -61 dBm | - | 26 | - | dB |
| Adjacent channel (±40 MHz) rejection - IEEE 802.11ax<br><br>(10% PER for 4096 octet PSDU with desired signal level as specified in Condition) | HE40, MCS0 | -76 dBm | - | 38 | - | dB |
| | HE40, MCS7 | -58 dBm | - | 21 | - | dB |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Spurious Emissions** | | | | | |
| Spurious emissions | < 1 GHz | - | - | -60 | dBm |
| | > 1 GHz | - | - | -50 | dBm |

# 5.11 WLAN RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2412 | - | 2484 | MHz |
| **TX Power** | | | | | |
| TX power - IEEE 802.11b (SEM compliant) | 1 Mbps DSSS | - | 20 | - | dBm |
| | 11 Mbps DSSS | - | 20 | - | dBm |
| TX power - IEEE 802.11g (EVM compliant) | 6 Mbps OFDM | - | 19 | - | dBm |
| | 54 Mbps OFDM | - | 16 | - | dBm |
| TX power - IEEE 802.11n (EVM compliant) | HT20, MCS0 | - | 19 | - | dBm |
| | HT20, MCS7 | - | 15 | - | dBm |
| | HT40, MCS0 | - | 18 | - | dBm |
| | HT40, MCS7 | - | 14 | - | dBm |
| TX power - IEEE 802.11ax (EVM compliant) | HE20, MCS0 | - | 19 | - | dBm |
| | HE20, MCS7 | - | 15 | - | dBm |
| **Spurious Emissions** | | | | | |
| Spurious emissions (at maximum output power) | < 1 GHz | - | - | -50 | dBm |
| | > 1 GHz | - | - | -43 | dBm |

# 5.12 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **General** | | | | | |
| Frequency range | - | 2402 | - | 2480 | MHz |
| **Bluetooth LE 1 Mbps** | | | | | |
| Sensitivity | 30.8% PER | - | -97 | - | dBm |
| Maximum input level | 30.8% PER | -10 | | - | dBm |
| C/I co-channel | - | - | 6 | 21 | dB |
| C/I 1 MHz adjacent channel | - | - | -2 | 15 | dB |
| C/I -1 MHz adjacent channel | - | - | -4 | 15 | dB |
| C/I 2 MHz adjacent channel | - | - | -30 | -17 | dB |
| C/I -2 MHz adjacent channel | - | - | -31 | -17 | dB |
| C/I 3 MHz adjacent channel | - | - | -30 | -27 | dB |
| C/I -3 MHz adjacent channel | - | - | -31 | -27 | dB |
| C/I > 3 MHz adjacent channel | - | - | -31 | -27 | dB |
| C/I < -3 MHz adjacent channel | - | - | -32 | -27 | dB |
| Out-of-band blocking | 30–2000 MHz | -30 | - | - | dBm |
| | 2003–2399 MHz | -35 | - | - | dBm |
| | 2484–2997 MHz | -35 | - | - | dBm |
| | 3000 MHz–12.75 GHz | -30 | - | - | dBm |
| Intermodulation | - | - | - | -50 | dBm |
| **Bluetooth LE 2 Mbps** | | | | | |
| Sensitivity | 30.8% PER | - | -93 | - | dBm |
| Maximum input level | 30.8% PER | -10 | | - | dBm |
| C/I co-channel | - | - | 5 | 21 | dB |
| C/I 2 MHz adjacent channel | - | - | -3 | 15 | dB |
| C/I -2 MHz adjacent channel | - | - | -7 | 15 | dB |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| C/I 4 MHz adjacent channel | - | - | -30 | -17 | dB |
| C/I -4 MHz adjacent channel | - | - | -30 | -17 | dB |
| C/I 6 MHz adjacent channel | - | - | -30 | -27 | dB |
| C/I -6 MHz adjacent channel | - | - | -30 | -27 | dB |
| C/I > 6 MHz adjacent channel | - | - | -31 | -27 | dB |
| C/I < -6 MHz adjacent channel | - | - | -34 | -27 | dB |
| Out-of-band blocking | 30–2000 MHz | -30 | - | - | dBm |
| | 2003–2399 MHz | -35 | - | - | dBm |
| | 2484–2997 MHz | -35 | - | - | dBm |
| | 3000 MHz–12.75 GHz | -30 | - | - | dBm |
| Intermodulation | - | - | - | -50 | dBm |
| **Bluetooth LE 125 kbps** | | | | | |
| Sensitivity | 30.8% PER | - | -102 | - | dBm |
| Maximum input level | 30.8% PER | -10 | | - | dBm |
| C/I co-channel | - | - | 4 | 12 | dB |
| C/I 1 MHz adjacent channel | - | - | -22 | 6 | dB |
| C/I -1 MHz adjacent channel | - | - | -17 | 6 | dB |
| C/I 2 MHz adjacent channel | - | - | -36 | -26 | dB |
| C/I -2 MHz adjacent channel | - | - | -33 | -26 | dB |
| C/I 3 MHz adjacent channel | - | - | -42 | -36 | dB |
| C/I -3 MHz adjacent channel | - | - | -36 | -36 | dB |
| C/I > 3 MHz adjacent channel | - | - | -42 | -36 | dB |
| C/I < -3 MHz adjacent channel | - | - | -37 | -36 | dB |
| **Bluetooth LE 500 kbps** | | | | | |
| Sensitivity | 30.8% PER | - | -98 | - | dBm |
| Maximum input level | 30.8% PER | -10 | | - | dBm |
| C/I co-channel | - | - | 3 | 17 | dB |
| C/I 1 MHz adjacent channel | - | - | -4 | 11 | dB |

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| C/I -1 MHz adjacent channel | - | - | -5 | 11 | dB |
| C/I 2 MHz adjacent channel | - | - | -34 | -21 | dB |
| C/I -2 MHz adjacent channel | - | - | -35 | -21 | dB |
| C/I 3 MHz adjacent channel | - | - | -34 | -31 | dB |
| C/I -3 MHz adjacent channel | - | - | -35 | -31 | dB |
| C/I > 3 MHz adjacent channel | - | - | -35 | -31 | dB |
| C/I < -3 MHz adjacent channel | - | - | -35 | -31 | dB |

# 5.13 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Frequency range | | - | 2402 | - | 2480 | MHz |
| TX power | | - | -20 | 6 | 15 | dBm |
| **Bluetooth LE 1 Mbps** | | | | | | |
| In-band emissions | $\pm 2$ MHz offset | - | - | -47 | -20 | dBm |
| | $\pm 3$ MHz offset | - | - | -50 | -30 | dBm |
| | $>\pm 3$ MHz offset | - | - | -52 | -30 | dBm |
| Modulation characteristics | $\Delta f1avg$ | - | 225 | 245 | 275 | kHz |
| | $\Delta f2max$ | - | 185 | 230 | - | kHz |
| | $\Delta f2avg/\Delta f1avg$ | - | 0.8 | 0.9 | - | - |
| Carrier frequency offset and drift | Max $|f_n|_{n = 0, 1, 2, 3\ldots k}$ | - | - | 24 | 150 | kHz |
| | Max $|f_0 - f_n|_{n = 2, 3, 4\ldots k}$ | - | - | 3 | 50 | kHz |
| | $|f_1 - f_0|$ | - | - | 2 | 23 | kHz |
| | Max $|f_n - f_{n-5}|_{n = 6, 7, 8\ldots k}$ | - | - | 2.5 | 20 | kHz/50 µs |
| **Bluetooth LE 2 Mbps** | | | | | | |
| In-band emissions | $\pm 4$ MHz offset | - | - | -50 | -20 | dBm |

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| | ±5 MHz offset | - | - | -51 | -20 | dBm |
| | >±5 MHz offset | - | - | -53 | -30 | dBm |
| Modulation characteristics | $\Delta f1avg$ | - | 450 | 480 | 550 | kHz |
| | $\Delta f2max$ | - | 370 | 460 | - | kHz |
| | $\Delta f2avg/\Delta f1avg$ | - | 0.8 | 0.9 | - | - |
| Carrier frequency offset and drift | Max $|f_n|$ $_{n = 0, 1, 2, 3...k}$ | - | - | 24 | 150 | kHz |
| | Max $|f_0 - f_n|$ $_{n = 2, 3, 4...k}$ | - | - | 3.5 | 50 | kHz |
| | $|f_1 - f_0|$ | - | - | 2 | 23 | kHz |
| | Max $|f_n - f_{n-5}|$ $_{n = 6, 7, 8...k}$ | - | - | 2.5 | 20 | kHz/50 μs |

**Bluetooth LE 125 kbps**

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| In-band emissions | ±2 MHz offset | - | - | -45 | - | dBm |
| | ±3 MHz offset | - | - | -48 | - | dBm |
| | >±3 MHz offset | - | - | -49 | - | dBm |
| Modulation characteristics | $\Delta f1avg$ | - | 225 | 245 | 275 | kHz |
| | $\Delta f1max$ | - | 185 | 235 | - | kHz |
| Carrier frequency offset and drift | Max $|f_n|$ $_{n = 0, 1, 2, 3...k}$ | - | - | 21.5 | 150 | kHz |
| | Max $|f_0 - f_n|$ $_{n = 1, 2, 3...k}$ | - | - | 3 | 50 | kHz |
| | $|f_0 - f_3|$ | - | - | 2 | 19.2 | kHz |
| | $|f_n - f_{n-3}|$ $_{n = 7, 8, 9...k}$ | - | - | 2.5 | 19.2 | kHz/48 μs |

**Bluetooth LE 500 kbps**

| Parameter | | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| In-band emissions | ±2 MHz offset | - | - | -46 | - | dBm |
| | ±3 MHz offset | - | - | -48 | - | dBm |
| | >±3 MHz offset | - | - | -50 | - | dBm |

# 5.14 AUX ADC Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Conversion clock | - | - | - | 13 | MHz |
| Conversion time | - | - | 16 | - | Cycle |
| $V_{REF}$ | Internal | - | 1.2 | - | V |
| | External | - | VIO/2 | - | V |
| Input voltage range | - | 0 | - | VREF*2 | V |
| Input impedance | - | 10 | - | - | MΩ |
| Input capacitance (Cs) | - | - | 1 | - | pF |
| DNL | - | -1 | - | 3 | LSB |
| INL | - | -5 | - | 5 | LSB |
| ENOB | - | - | 10 | - | Bit |
| SNDR | - | - | 62 | - | dB |
| SFDR | - | - | 77 | - | dB |
| $T_{STARTUP}$ | - | - | 5 | - | μs |
| Current consumption | - | - | 200 | - | μA |

# 6. Package Information

**Figure 6-1 QFN40 5 x 5 mm Package Outline**
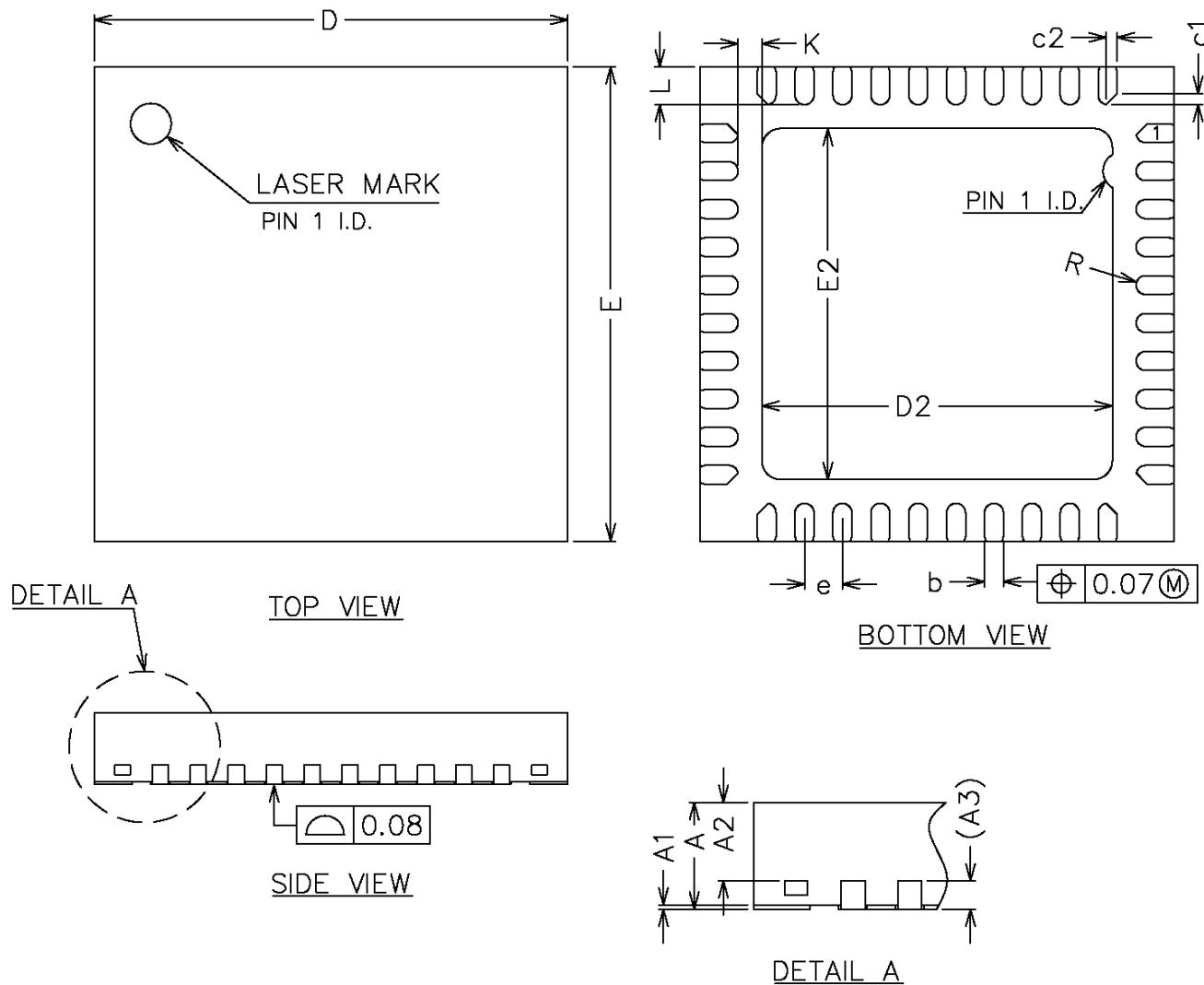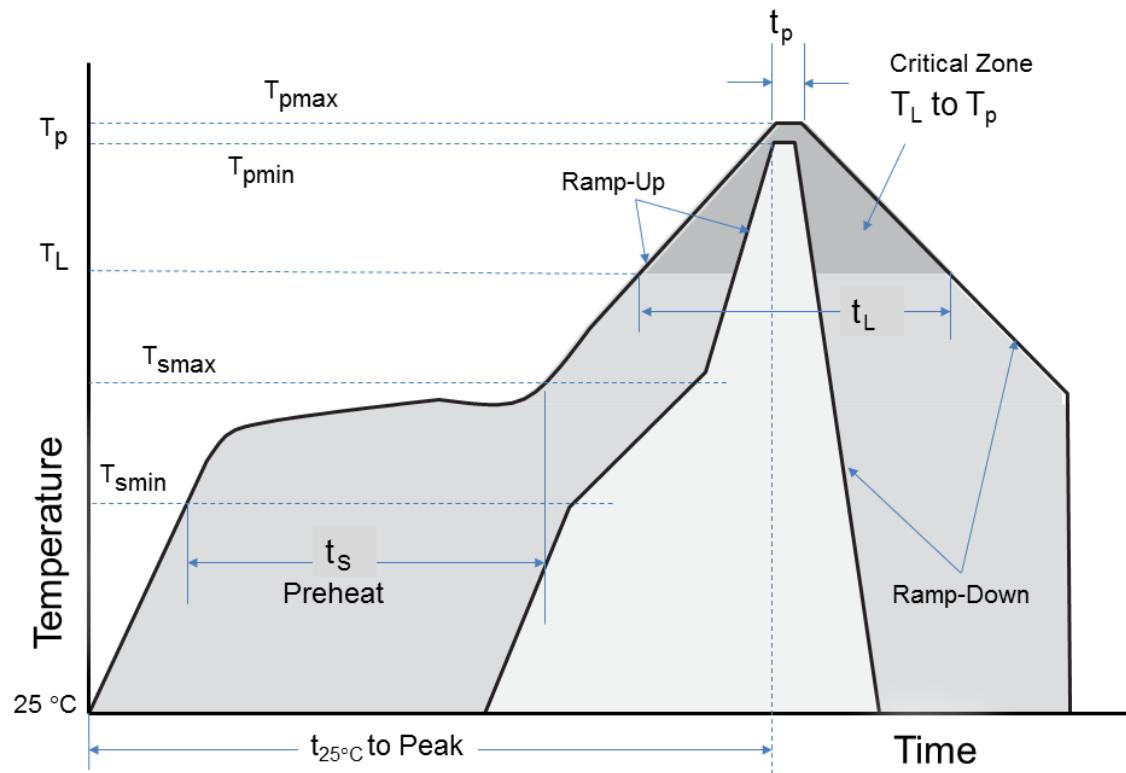


**Table 6-1 QFN40 Package Dimensions**

| Symbol | Dimensions in Millimeters | | |
|--------|------|------|------|
| | Min. | Nom. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |

| Symbol | Dimensions in Millimeters | | |
| --- | --- | --- | --- |
| | Min. | Nom. | Max. |
| A2 | 0.50 | 0.55 | 0.60 |
| A3 | 0.20 REF | | |
| b | 0.15 | 0.20 | 0.25 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| D2 | 3.60 | 3.70 | 3.80 |
| E2 | 3.60 | 3.70 | 3.80 |
| e | 0.35 | 0.40 | 0.45 |
| K | 0.20 | - | - |
| L | 0.35 | 0.40 | 0.45 |
| R | 0.075 | - | - |
| c1 | - | 0.12 | - |
| c2 | - | 0.12 | - |

# 7. Reflow Soldering Profile

**Figure 7-1 Reflow Soldering Profile**



| Profile Feature | | Specification |
|---|---|---|
| Average ramp-up rate ($T_{smax}$ to $T_p$) | | 3 °C/s max. |
| Preheat | Temperature min. ($T_{smin}$) | 150 °C |
| | Temperature max. ($T_{smax}$) | 200 °C |
| | Time ($t_s$) | 60 s to 180 s |
| Time maintained above | Temperature ($T_L$) | 217 °C |
| | Time ($t_L$) | 60 s to 150 s |
| Peak/classification temperature ($T_p$) | | 260 °C |
| Time within 5 °C of actual peak temperature ($t_p$) | | 20 s to 40 s |
| Ramp-down rate | | 6 °C/s max. |

| Profile Feature | Specification |
|---|---|
| Time 25 ℃ to peak temperature | 8 minutes max. |

## RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, and DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

## ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

## Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

# 8. Ordering Information

**Figure 8-1 Part Number Scheme**



Part number scheme blocks: BKxxxx | P | N/H or P | xx | m or N | n

- **PSRAM size (MByte)**
  0: No SiP PSRAM
- **Flash size (2^m Mbit)**
  N: No SiP Flash
- **Pin number**
- **Ambient temperature or package code 2 if no SiP Flash**
  N: Normal temperature (~85 °C)
  H: High temperature (~105 °C)
- **Package code 1**
- **Series/Family**
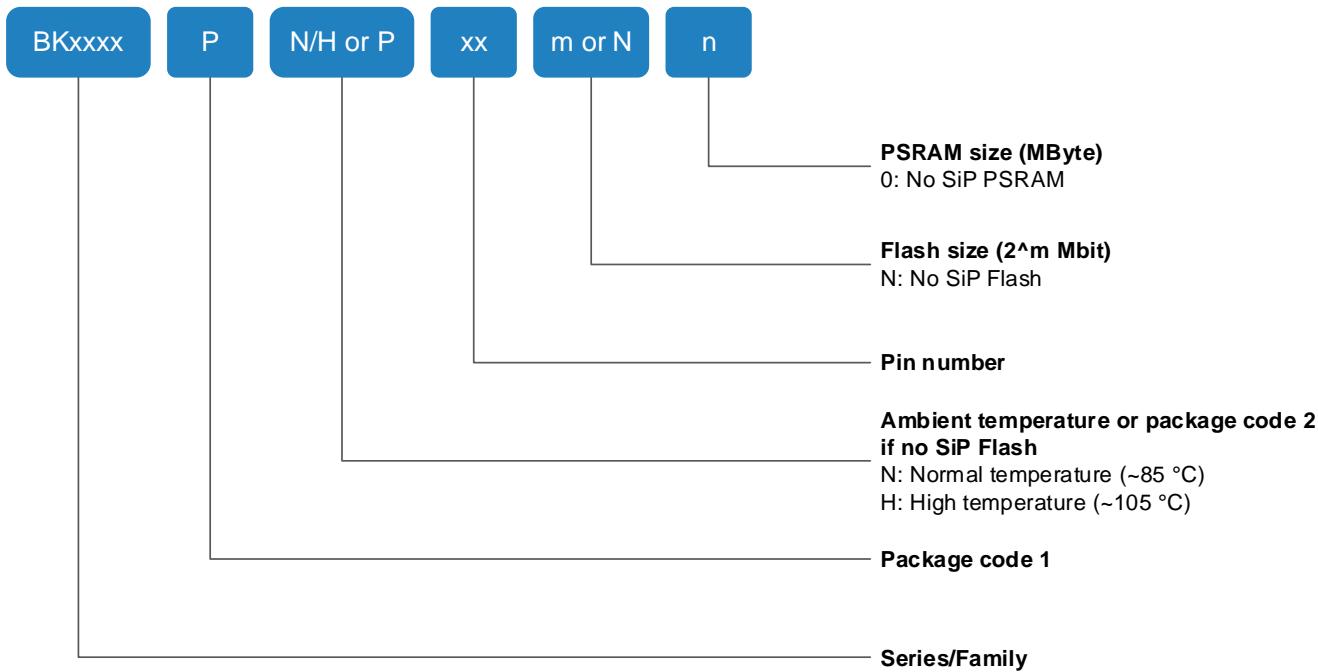
**Table 8-1 Ordering Information**

| Ordering Code | Package | SiP[a] Flash | SiP PSRAM | Packing | Minimum Ordering Qty (MOQ) |
|---|---|---|---|---|---|
| BK7235QN4050 | 5 mm x 5 mm QFN40 | 4 MB | - | Tape and Reel | 3000 |
| BK7235QH4050 | 5 mm x 5 mm QFN40 | 4 MB | - | Tape and Reel | 3000 |

a.    A system in a package (SiP) refers to Flash/PSRAM enclosed in the package.

# Revision History

| Version | Date | Description |
|---------|------|-------------|
| 0.1 | 2022/2/28 | Initial release |
| 1.0 | 2023/5/30 | • Renamed some interfaces and peripherals<br>• Updated TX power, RX sensitivity, and current consumption in Section 1 Features<br>• Updated core features in Section 1 Features<br>• Added SWD throughout the document<br>• Removed cache and eFuse throughout the document<br>• Corrected OTP size in Section 1 Features<br>• Updated secure element description and added KDF in subsection Security under Section 1 Features<br>• Updated VBAT voltage range to 2.8 to 5.0 V throughout the document<br>• Corrected the channel number of GDMA throughout the document<br>• Listed applications in Section 1 Features<br>• Updated Figure 2-1 in Section 2 Overview<br>• Added signal description for GPIOs in Section 3 Pin Description<br>• Added Section 3.2 Pin Multiplexing<br>• Updated wording for Section 4 Functional Description<br>• Updated the description of Section 4.2 Clock Management<br>• Moved the original section Modes of Operation to Section 4.4 Power Management<br>• Updated the description of power scheme and power modes in Section 4.4 Power Management<br>• Added CIS features in Section 4.12 CMOS Image Sensor Interface (CIS)<br>• Updated Section 4.15 Timer Group (TIMG), Section 4.16 Watchdog Timers, and Section 4.17 Real-Time Counter (RTC)<br>• Changed Section Security into Section 4.21 Secure Element<br>• Removed note "Values currently listed in this section are preliminary measurements and are subject to change." from Section 5 Electrical Characteristics<br>• Updated and added measurement data in Section 5 Electrical Characteristics |
| 1.1 | 2023/6/16 | • Updated applications in Section 1 Features<br>• Added CLK_AUXS and I2S_MCLK as clock signal outputs in Section 4.2 Clock Management |

| Version | Date | Description |
|---------|------|-------------|
| 1.2 | 2023/7/28 | • Renamed low-voltage sleep mode to sleep mode<br><br>• Updated Section 4.2 Clock Management<br><br>• Added ordering information for BK7235QH4050 in Section 8 Ordering Information |
| 1.3 | 2023/11/17 | • General wording fixes<br><br>• Updated OFDMA and TWT support and added Bluetooth LE features in Section 1 Features<br><br>• Removed normal sleep mode throughout document<br><br>• Added FIFO feature for IrDA interface in Section 4.18 IrDA Interface (IrDA)<br><br>• Updated the maximum value of VBAT in Section 5.1 Absolute Maximum Ratings<br><br>• Updated RoHS compliance statement in Section 7 Reflow Soldering Profile<br><br>• Updated ordering information in Section 8 Ordering Information |

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