BK7252 Data sheet

Wi-Fi Audio/Video SoC

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Contents

Revision History

Version	Description	Date	Author
V1.0	Initial release	May/15/2019	WF

1. Introduction

BK7252 is a 2.4 GHz 802.11n and BLE 4.2 comb chip with audio peripheral and image sensor interface. It integrates hardware and software component to finish a complete 802.11b/g/n audio and video application, which supports AP and STA role simultaneously, and integrates Bluetooth low energy transceiver and version 5.0 complaint protocol stack. The high speed 32-bit MCU and large embedded RAM make it able to support multiple cloud links and also suitable for audio and image application。

BK7252 has flexible peripheral such as PWM, I2S, I2C, UART, SPI, SDIO, USB and IrDA. Up to six channel 32-bit PWM outputs make it suitable for precise LED control.

BK7252 has two channel high performance audio DAC and one channel audio ADC together with line in interface.

BK7252 has I2S interface, which can work as either master or slave. The sample rate could be from 8 kHz to 48 kHz, and MCLK could be provided to external audio CODEC.

BK7252 has 8-bit DVP to get image data from CMOS sensor, which can be encoded by internal VGA grade motion JPEG codec. The integrated QSPI interface supports FLASH and RAM extension at the same time.

BK7252 provides transmit active and receive active indicators through two independent ports, to support external PA and external LNA.

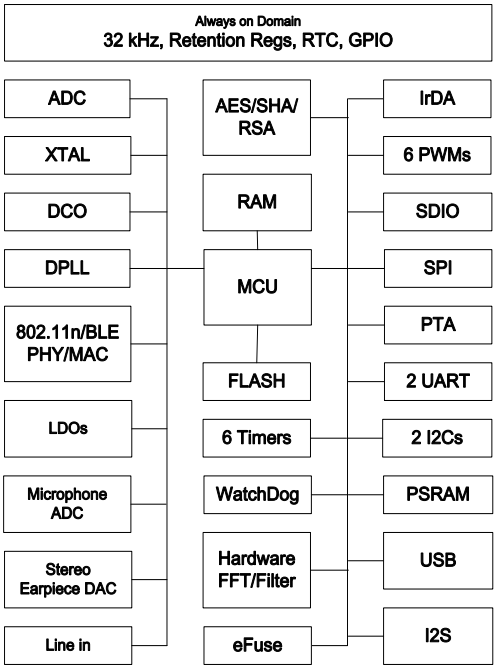
BK7252 has 32 bytes eFUSE for unique ID, code encryption and debug interface disable. The true random number generator and hardware AES/RSA/SHA support fast and security communication.

BK7252 could work with either 4.2 V battery or 5 V USB power supply.

There is a deep sleep mode with a few micro-amp current, and could be wake up by either GPIO activation or 32-bit RTC time.

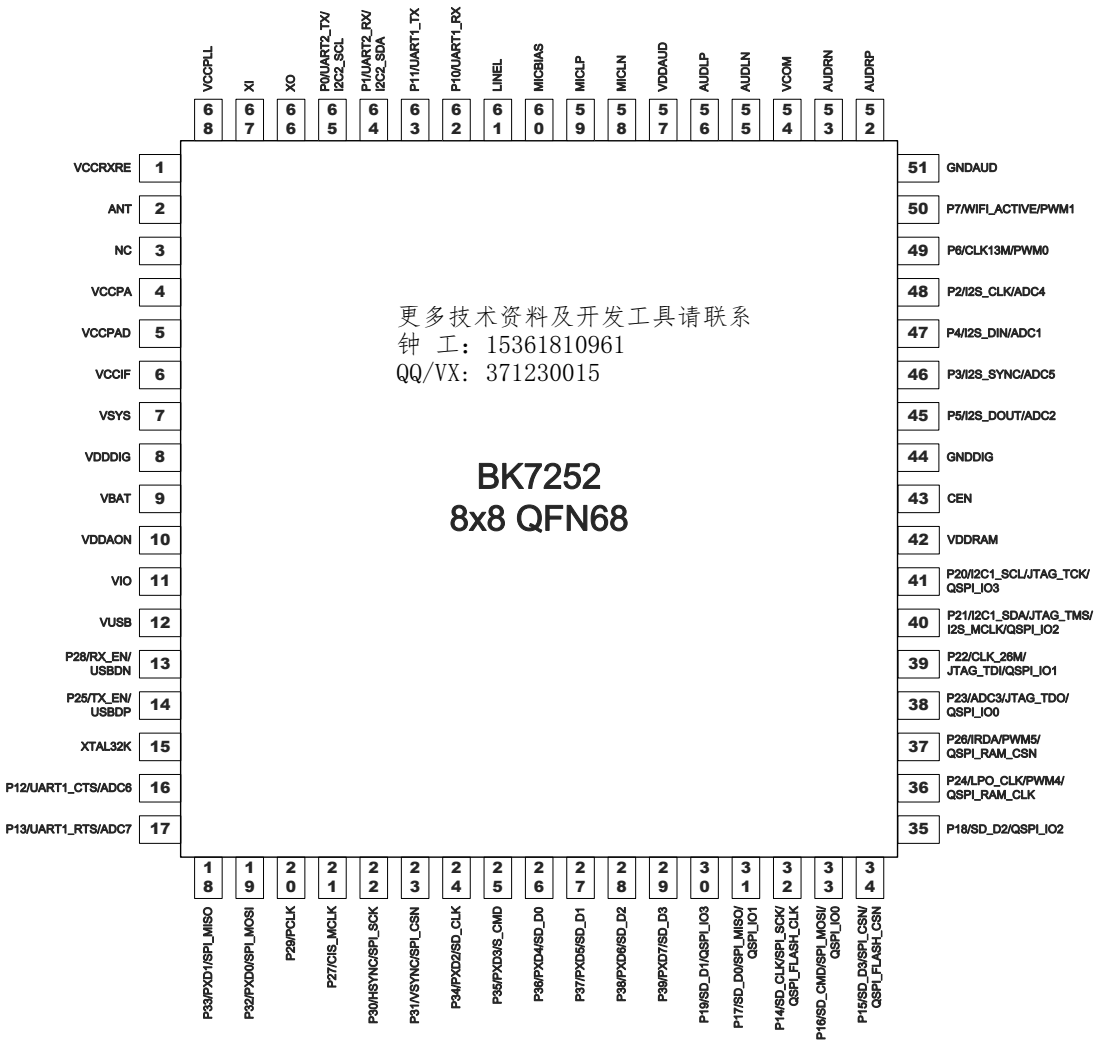
2. Features

- 802.11 b/g/n 1x1 compliant
- Up to 15 dBm output power at 54 Mbps mode
- Wide-band and narrow-band interference detection and alleviation
- 20/40 MHz bandwidth and STBC
- Working mode STA, AP, Direct
- AP and STA role simultaneously
- Bluetooth low energy 4.2
- Classic Bluetooth co-existence
- 32-bit MCU up to 180 MHz
- 512 KB internal data RAM
- QSPI for RAM and FLASH extension
- Multiplexing program download and JTAG interface
- Full speed USB host and device
- 50 MHz SDIO interface and SPI
- Dual I2C interface
- Dual high speed UART with flow control capability
- Six 32-bit timer and one always on timer
- Six 32-bit PWM with either high speed clock or low power clock
- One channel audio ADC and two channel audio DAC
- Line in input
- Multi-channel ADC with high speed 10-bits or low speed 16-bit with internal decimation filter
- CMOS sensor 8-bit DVP
- VGA Motion JPEG hardware encoder and dedicate DMA
- 32 bytes eFUSE and true random number generator
- Hardware AES/RSA/SHA
- 26 MHz and 32 KHz clock signal output



3. Pin Description

BK7252 has a QFN8x8 68pin package.



BK7252 68PIN Description

68PIN	Name	Pin Type	Description
1	VCCRXFE	I	RF receiver power supply. Supplied by VSYS
2	ANT	IO	2.4 GHz RF signal port
3	NC	X	Not connected
4	VCCPA	I	RF PA power supply. Supplied by VIO
5	VCCPAD	I	RF transmitter power supply. Supplied by VIO
6	VCCIF	I	IF power supply. Supplied by VSYS
7	VSYS	O	System LDO output, ~3.0 V
8	VDDDIG	O	Digital LDO output, ~1.2 V
9	VBAT	I	Chip power supply, 3.0~4.2 V
10	VDDAON	O	Always on LDO output, ~1.2 V
11	VIO	O	IO voltage, ~ 3.3 V
12	VUSB	I	Chip power supply, 5V
13	P28/RX_EN/USBDN	IO	GPIO or RX enable or USB DN
14	P25/TX_EN/USBDP	IO	GPIO or TX enable or USB DP
15	XTAL32K	I	32 kHz XTAL
16	P12/UART1_CTS/ADC6	IO	GPIO or UART1 CTS or ADC6
17	P13/UART1_RTS/ADC7	IO	GPIO or UART1 RTS or ADC7
18	P33/PXD1/SPI_MISO	IO	GPIO or DVP D1 or SPI MISO
19	P32/PXD0/SPI_MOSI	IO	GPIO or DVP D0 or SPI MOSI
20	P29/PCLK	IO	GPIO or DVP PCLK
21	P27/CIS_MCLK	IO	GPIO or DVP MCLK
22	P30/HSYNC/SPI_SCK	IO	GPIO or DVP HSYNC or SPI Clock
23	P31/VSYNC/SPI_CSN	IO	GPIO or DVP VSYC or SPI CSN
24	P34/PXD2/SD_CLK	IO	GPIO or DVP D2 or SDIO Clock
25	P35/PXD3/SD_CMD	IO	GPIO or DVP D3 or SDIO

			CMD
26	P36/PXD4/SD_D0	IO	GPIO or DVP D4 or SDIO Date 0
27	P37/PXD5/SD_D1	IO	GPIO or DVP D5 or SDIO Data 1
28	P38/PXD6/SD_D2	IO	GPIO or DVP D6 or SDIO Data 2
29	P39/PXD7/SD_D3	IO	GPIO or DVP D7 or SDIO Data 3
30	P19/SD_D1/QSPI_IO3	IO	GPIO or SDIO D1 or QSPI IO3
31	P17/SD_D0/SPI_MISO/QSPI_IO1	IO	GPIO or SDIO D0 or SPI MISO or QSPI IO1
32	P14/SD_CLK/SPI_SCK/QSPI_FLASH_CLK	IO	GPIO or SDIO Clock or SPI Clock or QSPI FLASH clock
33	P16/SD_CMD/SPI_MOSI/QSPI_IO0	IO	GPIO or SDIO CMD or SPI MOSI or QSPI IO0
34	P15/SD_D3/SPI_CSN/QSPI_FLASH_CSN	IO	GPIO, SDIO D3 or SPI CSN or QSPI FLASH CSN
35	P18/SD_D2/QSPI_IO2		GPIO or SDIO D2 or QSPI IO2
36	P24/LPO_CLK/PWM4/QSPI_RAM_CLK	IO	GPIO or low power clock output or PWM 4 or QSPI RAM clock
37	P26/IRDA/PWM5/QSPI_RAM_CSN	IO	GPIO or IrDA input or PWM 5 or QSPI RAM CSN
38	P23/ADC3/JTAG_TDO/QPIO_IO0	IO	GPIO or ADC or JTAG TDO, or QSPI IO0 FLASH download data output at download mode
39	P22/CLK_26M/JTAG_TDI/QSPI_IO1	IO	GPIO or Crystal clock output, or JTAG TDI or QSPI IO1 FLASH download data input at download mode
40	P21/I2C1_SDA/JTAG_TMS/QSPI_IO2	IO	GPIO or I2C1 TMS, or JTAG TMS or QSPI IO2 Flash download chip enable signal at download mode

41	P20/I2C1_SCL/JTAG_TCK/QSPI_IO3	IO	GPIO or I2C1 SCL, or JTAG TCK or QSPI IO3 Flash download port clock signal at download mode
42	VDDRAM	O	Power supply for external PSRAM,1.8V ,2.5V, or 3.3V
43	CEN	I	Chip enable, active high
44	GNDDIG	GND	Ground
45	P5/I2S_DOUT/ADC2	IO	GPIO or I2S DOUT or ADC2
46	P3/I2S_SYNC/ADC4	IO	GPIO or I2S SYNC or ADC5
47	P4/I2S_DIN/ADC1	IO	GPIO or I2S DIN or ADC1
48	P2/I2S_CLK/ADC5	IO	GPIO or I2S Clock or ADC4
49	P6/CLK13M/PWM0	IO	GPIO or Crystal Clock output divided by 1/2/4/8 or PWM 0
50	P7/WIFI_ACTIVE/PWM1	IO	GPIO or Wi-Fi active output or PWM 0
51	GNDAUD	GND	Ground
52	AUDRP	O	Audio output right channel positive
53	AUDRN	O	Audio output right channel negative
54	VCOM	O	Common mode output
55	AUDLN	O	Audio output left channel negative
56	AUDLP	O	Audio output left channel positive
57	VDDAUD	O	Audio de-coupling
58	MICLN	I	Microphone input left channel negative
59	MICLP	I	Microphone input right channel positive
60	MICBIAS	O	Microphone bias voltage output
61	LINEL	I	Line in left channel
62	P10/UART1_RX	IO	GPIO or UART1 RX

63	P11/UART1_TX	IO	GPIO or UART1 TX
64	P1/UART2_RX/I2C2_SDA	IO	GPIO or UART2 RX or I2C2 SDA
65	P0/UART2_TX/I2C2_SCL	IO	GPIO or UART2 TX or I2C2 SCL
66	XO	O	26/40 MHz Crystal output
67	XI	I	26/40 MHz Crystal input
68	VCCPLL	I	RF PLL power supply. Supplied by VSYS after RC filter

4. Wi-Fi and Bluetooth

The BK7252 supports full features of 802.11b/g/n Wi-Fi system, with both HT20 and HT40 capability. There are transmitter active indicator (GPIO25) and receiver active indication (GPIO28) for external LNA and PA to reach longer range.

The integrated Bluetooth low energy 4.2 shares the single antenna port with Wi-Fi transceiver, and both Wi-Fi and Bluetooth could work simultaneously with precise time multiplexing.

5. Clock

There are seven root clock signals in the system.

- X26M: The high speed crystal oscillator, typical frequency is 26 MHz, which is also the reference clock signal for digital PLL (DPLL) and audio PLL (I2SPLL); There is tunable load capacitance from 6 to 18 pF (both side have this capacitance) with 64 steps to tune the crystal frequency, that no external capacitance is needed; This clock signal has about one milliseconds startup time
- DCO: Internal high speed digital controlled oscillator, with frequency from 26 MHz to 180 MHz, and about +/-2 frequency variation after calibration; This clock signal has a few microsecond startup times
- X32K: The low speed crystal oscillator, typical frequency is 32.768 kHz

- D32K: 32 kHz clock signal divided from X26M
- ROSC: Internal low speed ring oscillator with ±2% variation after calibration
- DPLL: High speed 480 MHz PLL clock
- I2SPLL: PLL for audio signal, typical frequency is 1024*FS and typical FS is 44.1 kHz or 48 kHz

Low power clock (LPO_CLK) is selected from X32K, D32K or ROSC.

The MCU and peripheral clock selection option is list as follows.

	X26M	**DCO**	**DPLL**	**LPO_CLK**	**I2SPLL**
MCU	√	√	√	√	
ADC	√	√			√
SDIO	√	√			
PWM	√	√		√	
SPI	√	√			
I2C2	√	√			
IrDA	√	√			
I2C1	√	√			
UART2	√	√			
UART1	√	√			
QSPI	√	√	√		
Timer 1	√				
Timer 2				√	
I2S					√
CIS/MJPEG			√		
Watch Dog				√	
Always on timer				√	

There is also clock output capability to output clock signal for external components.

- The LPO_CLK and X26M clock could be output to GPIO for general purpose.
- 13 MHz clock divided from X26M: It is aimed to provide clock for FM receiver

- I2S MCLK: It is divided from I2SPLL and the divider number could be 1, 2, 4, 8, 16
- PCLK for CIS Sensor: It is divided from DPLL and the typical frequency is 24 MHz, 48 MHz or 96 MHz

6. Reset

System power on, digital power on and watch dog reset have the same reset effect for major blocks except always on logic, that any reset will reset the BK7252 whole chip to initial status. The always on logic has one 32 bit timer and 16 bit retention register, which could be only reset to initial value by system power on reset.

Waking up from either shut down mode or deep sleep mode will power on digital from power down mode, that trigger the whole system reset procedure.

7. Power management

To reduce power, the BK7252 can be put in three low power modes as follows.

Shutdown – In this mode all circuits are powered down when CEN = 0, and the system will power on only after CEN back and keep high for a few milliseconds. The software could also shut down the system and could wake up from GPIO13.

Deep sleep mode – In this mode all circuits are powered down except the GPIO and always on logic, that any GPIO edge transition or always on timer time out event can power up the system again. The retention register could keep it contents at this mode.

Normal Standby – In this mode the MCU stop running and all peripheral interrupt can resume MCU.

Low voltage Standby – In this mode the MCU and all digital logic stop their clock, and the power supply of them decrease to a much lower retention voltage, that the current could be much lower. In this mode, only GPIO and RTC timer could resume the system to run mode with normal voltage.

8. Peripheral

8.1. UART

BK7252 has two sets of UART. The maximum baud rate can be up to 6 Mbps. It supports 5, 6, 7 and 8 bits data mode, and supports even, odd or none parity check. The stop bit can be either 1 or 2 bits.

The UART1 supports hardware and software flow control with RTS and CTS signal.

At MCU low voltage stand-by mode, the continuously low level applied on TX or RX could wake up the MCU that the UART and MCU can resume to active mode.

8.2. SPI

BK7252 supports one high speed SPI interface with maximum 50 MHz clock speed, with only slave mode. This high speed SPI has dedicated DMA channel that could work on high speed without MCU load.

It also supports low speed SPI interface with up to 8 MHz, with both master and slave mode. The receive data could be latched on either rising edge or falling edge of clock signal. The transmit data could be set by MSB or LSB first.

8.3. SDIO

BK7252 SDIO has both master and slave mode, and one bit to four bits mode with maximum 50 MHz clock speed. SDIO could be used as master mode to read external SD card or used by external host to communicate with chip as slave mode.

SDIO has dedicated DMA channel that could work on high speed without MCU load.

8.4. I2C

BK7252 supports two sets of I2C with normal 400 kHz clock speed, with 7 bit addressing. If low level on SCL or bus idle duration is greater than a programmable threshold, it will generate interrupt to MCU.

8.5. USB

BK7252 has full speed USB 2.0, with both host and device mode. The host or device mode is selected by software register.

USB has dedicated DMA channel that could work on high speed without MCU load.

8.6. General purpose ADC

BK7252 has multi-channel general purpose ADC and supports 10-16 bits output with internal decimation filter. Single, continuously and software read mode are supported.

Besides GPIO, the system power VSYS, temperature sensor and internal calibration circuit could be also the ADC source.

8.7. PWM

BK7252 has six 32-bit PWM outputs. The PWM running clock can be either high speed clock or low power clock. Each PWM runs independently with its own duty cycle.

The PWM has capture mode that can count the cycle between two rising edges or two falling edges.

8.8. Timer

BK7252 has two group peripheral timers; each group has three 32-bit timers. The first group three timers run with crystal clock with 4-bit pre-scaler. The second group three timers run with low power clock with another 4-bit pre scaler.

The watch dog time is used to reset system as long as the software runs out of order, and it stops as long as MCU stops or power off.

The always on timer works under always on power domain, that it can keep running even MCU is power off.

8.9. GPIO

BK7252 has total 40 GPIOs and anyone could be set an interrupt source to interrupt system at active mode or wake up system from sleep mode.

The GPIO driver capability could be set to 4 mA and up to 32 mA.

The GPIO has peripheral function as table below.

GPIO	Peripheral Mode1	Peripheral Mode2	Peripheral Mode3	Peripheral Mode4	Analog Mode
GPIO0	UART2_TX	I2C2_SCL			
GPIO1	UART2_RX	I2C2_SDA			
GPIO2	I2S_CLK				ADC4
GPIO3	I2S_SYNC				ADC5
GPIO4	I2S_DIN				ADC1
GPIO5	I2S_DOUT				ADC2
GPIO6	PWM0	CLK13M			
GPIO7	PWM1	WIFI_ACTIVE			
GPIO8	PWM2	BT_ACTIVE			
GPIO9	PWM3	BT_PRIORITY			
GPIO10	UART1_RX				
GPIO11	UART1_TX				
GPIO12	UART1_CTS	PGA_INP			ADC6
GPIO13	UART1_RTS	PGA_INN			ADC7

GPIO14	SD_CLK	SPI_SCK	QSPI_FLASH_CLK		
GPIO15	SD_D3	SPI_CSN	QSPI_FLASH_CSN		
GPIO16	SD_CMD	SPI_MOSI	QSPI_IO0		
GPIO17	SD_D0	SPI_MISO	QSPI_IO1		
GPIO18	SD_D2		QSPI_IO2		
GPIO19	SD_D1		QSPI_IO3		
GPIO20	I2C1_SCL	JTAG_TCK	QSPI_IO3		
GPIO21	I2C1_SDA	JTAG_TMS	QSPIO_IO2	I2S_MCLK	
GPIO22	CLK_26M	JTAG_TDI	QSPI_IO1		
GPIO23		JTAG_TDO	QSPI_IO0		ADC3
GPIO24	LPO_CLK	PWM4	QSPI_RAM_CLK		
GPIO25	TXEN				USBDP
GPIO26	IRDA	PWM5	QSPI_RAM_CSN		
GPIO27	CIS_MCLK				
GPIO28	RX_EN				USBDN
GPIO29	PCLK				
GPIO30	HSYNC	SPI_SCK			
GPIO31	VSYNC	SPI_CSN			
GPIO32	PXD0	SPI_MOSI			
GPIO33	PXD1	SPI_MISO			
GPIO34	PXD2	SD_CLK			
GPIO35	PXD3	SD_CMD			
GPIO36	PXD4	SD_D0			
GPIO37	PXD5	SD_D1			
GPIO38	PXD6	SD_D2			
GPIO39	PXD7	SD_D3			

The peripheral function is listed as follows.

Function Name	Second Sets	Description
UART1_TX	UART2_TX	UART TX data
UART1_RX	UART2_RX	UART RX data
UART1_RTS		UART1 request to send
UART1_CTS		UART1 clear to send
I2C_SCL	I2C2_SCL	I2C clock
I2C_SDA	I2C2_SDA	I2C data

IrDA		IrDA input
USBDP		USB data positive
USBDN		USB data negative
SPI_CSN		SPI chip enable
SPI_SCK		SPI clock
SPI_MOSI		SPI master output slave input
SPI_MISO		SPI master input slave output
PWM0~5		PWM waveform output
SD_CLK		SD card clock
SD_CMD		SD card command
SD_D0		SD card data0
SD_D1		SD card data1
SD_D2		SD card data2
SD_D3		SD card data3
JTAG_TCK		JTAG clock
JTAG_TMS		JTAG TMS
JTAG_TDI		JTAG TDI
JTAG_TDO		JTAG TDO
TX_EN		Indicator of transmitter is active
RX_EN		Indicator of receiver is active
I2S_MCLK		MCLK output of I2S interface
I2S_SYNC		I2S or PCM synchronization or symbol signal
I2S_CLK		I2S or PCM bit clock signal
I2S_DIN		I2S or PCM data input signal
I2S_DOUT		I2S or PCM data output signal
QSPI_FLASH_CLK		QSPI FLASH clock
QSPI_FLASH_CSN		QSPI FLASH enable
QSPI_IO0		QSPI data IO0

QSPI_IO1		QSPI data IO1
QSPI_IO2		QSPI data IO2
QSPI_IO3		QSPI data IO3
QSPI_RAM_CLK		QSPI RAM clock
QSPI_RAM_CSN		QSPI RAM enable
WIFI_ACTIVE		Wi-Fi active indicator output
BT_ACTIVE		Bluetooth active indicator input
BT_PRIORITY		Bluetooth packet priority indicator input
CLK13M		Crystal Clock output divided by 1/2/4/8
CLK_26M		Crystal clock output
LPO_CLK		Low power clock output
ADC1~7		General purpose ADC input channel
CIS_MCLK		CMOS sensor DVP interface MCLK
PCLK		CMOS sensor DVP interface PCLK
HSYNC		CMOS sensor DVP interface HSYNC
VSYNC		CMOS sensor DVP interface VSYNC
PXD0		CMOS sensor DVP interface data 0
PXD1		CMOS sensor DVP interface data 1
PXD2		CMOS sensor DVP interface data 2
PXD3		CMOS sensor DVP interface data 3
PXD4		CMOS sensor DVP interface data 4
PXD5		CMOS sensor DVP interface data 5
PXD6		CMOS sensor DVP interface data 6
PXD7		CMOS sensor DVP interface data 7

8.10. FLASH Download

Any time the digital logic resets to active, within a few hundred milliseconds the GPIO20~GPIO23 will act as mode selection port and then back to normal GPIO mode. If there is FLASH download command, these four ports will change to FLASH download port that FLASH could be programming.

8.11. CMOS Sensor Interface and MJPEG Encoder

The CMOS sensor interface provides 8-bit parallel port interface (GPIO32~GPIO39) to VGA sensor, together with main clock (GPIO27), pixel clock (GPIO29), HSYNC (GPIO30) and VSYNC (GPIO31) signal. Supported sensor could be but not limited to be OV7676, OV7670, GC0308, GC0309, GC0329 and PAS6329.

The interface and MJPEG work with 96 MHz clock divided from DPLL, and the main clock to the sensor is integer divided from 96 MHz.

The sensor YUV input will be directly fed to hardware MJPEG encoder, and the MJPEG encoder output will be write to data memory directly by dedicate DMA.

The YUV signal format could be YUYV, UYVY, YYUV and UVYY. HSYNC and VSYNC edge could be set independently.

8.12. IrDA interface

There is a hardware IrDA decoder interface to decode the signal. Also the interface has the capture timer capability to allow software decoding the input signal.

8.13. I2S interface

The I2S interface supports both master and slave mode, with sample rate from 8 kHz to 96 kHz. The master clock can be output by GPIO21.

8.14. Audio Peripheral

The BK7252 comes with a rich set of audio peripherals. The chip includes a 5-band digital equalizer, 16 bits analog-to-digital converter (ADC) and 16 bits stereo digital-to-analog converter (DAC), microphone input amplifier and bias, line-in input, and stereo audio left and right (L/R) outputs. The DAC is capable of driving 16ohm speakers with up to 30 pF of load capacitance.

The typical sample rate of ADC and DAC is to 8 kHz、44.1 kHz and 48 kHz, but could be set to more sample rate from 8 kHz to 48 kHz.

A dedicated 5-band digital equalizer is implemented prior to digital-to-analog conversion to give users the option of customizing the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

BK7252 includes line-in inputs with 0~6 dB amplifier and 2 dB step. The digitized line-in inputs can be further processed with the 5-band equalizer prior to digital-to-analog conversion.

There is a hardware accelerator with the FFT and FIR mode, which can do either 256 points complex hardware FFT or dual channel 256 taps FIR filter. The operation speed can be same as MCU clock.

8.15. QSPI Interface

The QSPI is designed for FLASH and RAM extension. The data IO are time shared by FLASH and RAM, while dedicate clock and select signal are separately used by FLASH and RAM. The QSPI can work up to 120 MHz, and FLASH clock and RAM clock can be set different.

8.16. Security

There are a true random number generator and eFUSE for system and communication security.

The 32 byte eFUSE could be written through download port GPIO20~GPIO23 at download mode. The eFUSE has defined function mapping as follows. All bytes could be read by MCU and download port except low 16 bytes could not be read out by download port.

Byte 31	Byte 30:16	Byte 15:0
JTAG Interface Disable	User Defined such as MAC address	Code Encryption

There is hardware accelerator for AES/RSA/SHA. It supports up to AES256 with GCM mode, RSA4096 and SHA512.

8.17. Temperature Sensor

The temperature sensor has +/-3 degree precision and could detect temperature from -40 to +125 degree, and digital result could be read out from ADC.

9. Characteristics

9.1. Absolute maximum ratings

Item	Pin Name	Min.	Max.	Unit
USB power supply voltage	VUSB	4.75	5.75	V
Battery supply voltage	VBAT	-0.3	4.2	V
Digital Input Pin		-0.3	3.9	V
RX input power	ANT		10	dBm
Storage Temperature		-55	125	℃

9.2. ESD Ratings

Item	Detail	Value	Unit
ESD_HBM	Electrostatic Discharge Tolerance under Human Body Model	+/-2000	V
ESD_MM	Electrostatic Discharge Tolerance under Man Machine Model	+/-200	V
ESD_CDM	Electrostatic Discharge Tolerance under Charged Device Model	+/-250	V

9.3. Recommended operating conditions

Parameters	Condition	Min.	Typ.	Max.	Unit
Operation Voltage	VBAT-pin	3.0	3.3	4.2	V

Operation Temperature		-20		85	℃

9.4. Current Consumption

Parameters	Condition	Min.	Typ.	Max.	Unit
Transmit current	17 dBm, 802.11b 11Mbps		230		mA
Transmit current	14 dBm, 802.11g 54Mbps		200		mA
Receiver current	-10 dBm input, 802.11g 54Mbps		104		mA
Receiver current	-10 dBm input, 802.11n HT40 MCS7		124		mA
Normal Stand-By	MCU stop, Modem power Off, could be woke up by internal timer		100		uA
Low Voltage Stand-By	MCU stop with low voltage, could be only woke up by GPIO or RTC timer		40		uA
Deep-sleep current	All power off, could be only woke up by GPIO or RTC timer		10		uA
Shut-down current	CEN=0		1		uA
Note: The measurement above is at 25 degree and 3.3 V battery voltage					

9.5. WLAN Receiver Characteristics

Parameters	Condition	Min.	Typ.	Max.	Unit
Sensitivity	HT40 MCS7		-69		dBm
	HT20 MCS7		-71		dBm
	54 Mbps OFDM		-75		dBm
	6 Mbps OFDM		-92		dBm
	11 Mbps DSSS		-90		dBm
	2 Mbps DSSS		-94		dBm
ACS (25 MHz away)	54 Mbps OFDM		21		dB
	11 Mbps DSSS		31		dB

9.6. WLAN Transmitter Characteristics

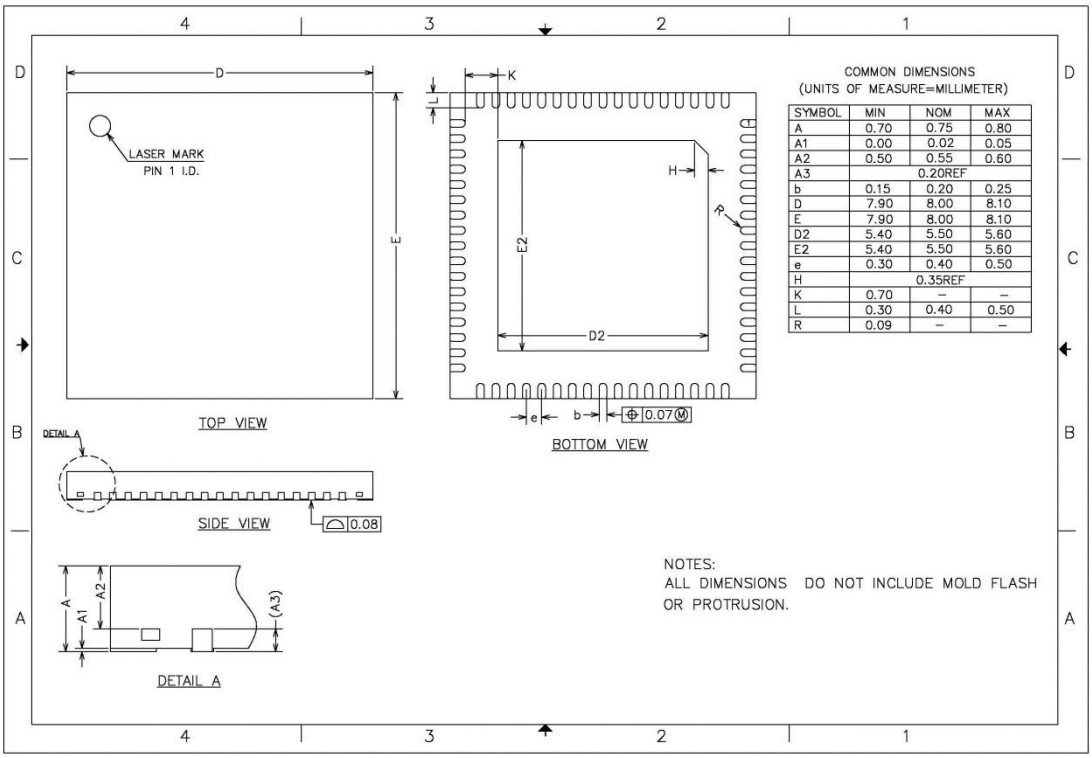
Parameters	Condition	Min.	Typ.	Max.	Unit

Transmit Power EVM and MASK Compliant	54 Mbps OFDM			15	dBm
	11 Mbps DSSS			19	dBm

9.7. Audio Characteristics

Parameter	Condition	MIN	TYP	MAX	Unit
DAC Diff. Output Amplitude	With 600ohm loading			1.1	Vrms
	With 32ohm loading		-	-	Vrms
	With 16ohm loading			0.9	Vrms
DAC Diff. Output THD	With 16 ohm loading		80		dB
	With 16 ohm loading		75		dB
DAC output SNR	1 kHz sine wave		96		dB
DAC Sample Rate		8		96	kHz
Audio Output Gain		-34		6	dB
Audio Output Gain Step			1		dB
Audio Output Channel Separation	Full Differential		90		dB
Common mode	VCOM		1.5		V
Microphone Gain		0		42	dB
Microphone Gain Step			2		dB
Microphone Reference	MICREF		2.5		V
Audio Input Channel Separation			100		dB
ADC Sample Rate		8		96	kHz
ADC SNR	1 kHz sine wave		87		dB

10. Package



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20REF	
b	0.15	0.20	0.25
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
e	0.30	0.40	0.50
H		0.35REF	
K	0.70	–	–
L	0.30	0.40	0.50
R	0.09	–	–

11. Order Information

Part number	Package	Packing	MPQ(ea)
BK7252QN68	QFN68 8mmX8mm	Tape Reel	3K