BK7258 Datasheet

DS-BK7258-E10 V1.9

2024/11/21

Contents

1. Features

Wi-Fi

- IEEE 802.11b/g/n/ax 1x1 compliant
- 20/40 MHz channel bandwidth for 2.4 GHz
- Supports downlink Multi-User Multiple-Input Multiple-Output (DL MU-MIMO)
- Supports Orthogonal Frequency Division Multiple Access (OFDMA)
- Supports Target Wake Time (TWT)
- TX and RX Low-Density Parity Check (LDPC) support for extended range
- WPA/WPA2/WPA3-Personal support for enhanced security
- Supports STA and SoftAP modes
- Supports concurrent SoftAP + STA
- Integrated Bluetooth/Wi-Fi coexistence (PTA)
- TX power up to +20 dBm
- RX sensitivity -98 dBm

Bluetooth Low Energy

- Bluetooth Low Energy (LE) 5.4
- Supports Bluetooth Low Energy 1 Mbps, 2 Mbps, and long range (125 kbps and 500 kbps)
- Supported Bluetooth Low Energy features: LE Audio, Angle of Arrival (AoA) and Angle of Departure (AoD) direction finding, 2 Mbps, advertising extensions, and long range
- Supports an antenna array with up to 16 antennas for precise positioning

Core

- Armv8-M STAR-MC1 MCU at up to 480 MHz:
  - Double-precision floating-point unit (FPU)
  - 16 KB ITCM + 16 KB DTCM
  - Embedded TrustZone
  - Supports DSP instructions with SIMD
  - 3.84 CoreMark/MHz
- UART flash download
- Serial Wire Debug (SWD) interface

Memory

- Flash (XIP): SiP flash up to 8 MB, external flash up to 16 MB
- SiP PSRAM: up to 16 MB
- Flash/PSRAM expansion: up to 4 GB via QSPI interface
- 640 KB Share SRAM
- 64 KB ROM
- eFuse

Clock Management

- External oscillators: 26 MHz crystal oscillator (XTALH), 32 kHz crystal oscillator (XTALL)
- Internal oscillators: 26–360 MHz digitally controlled oscillator (DCO), 32 kHz ring oscillator (ROSC)
- 320/480 MHz PLL (DPLL)
- Audio PLL (APLL)

Power Management

- 2.5 to 4.35 V VBAT supply
- On-chip Power-On Reset (POR) and Brown-Out Detector (BOD)
- Embedded buck (DC-DC) converters and LDO regulators
- Low power consumption:
  - Active mode RX: 17.5 mA
  - Sleep mode: 43 µA
  - Deep sleep mode: 16 µA
  - Shutdown mode: 2.5 µA

Peripherals

- GPIOs: 56 in QFN88, 46 in QFN68
- 2x SPI
- 2x QSPI
- 3x UART, 1 with hardware flow control and flash download support
- 1x Smart Card controller (SC)
- 1x SDIO
- 2x I2C
- 1x high-speed USB2.0 (HS)
- 1x CAN controller with CAN FD (CAN)

- 1x LIN controller (LIN)
- 2x general-purpose DMA controller (GDMA), each with 8 channels
- 1x DMA2D controller (DMA2D)
- 1x rotation module (ROTT)
- 2x scaling module (SCALE)
- 1x display controller supporting RGB and 8080 interfaces (DISPLAY)
- 1x segment LCD controller for up to 8 x 28 segments (SLCD)
- 1x JPEG hardware encoder
- 1x JPEG hardware decoder
- 1x 8-bit CIS DVP interface (CIS)
- 1x 720p H.264 video encoder (H.264)
- 1x Ethernet MAC interface (ENET)
- 12x 32-bit PWM channel
- 3x I2S
- 1x four-band digital hardware equalizer (EQ)
- 2x audio ADC
- 1x audio DAC
- 1x DMIC
- 1x SBC accelerator (SBC)
- 12-bit AUX ADC, up to 11 channels
- 6x 32-bit general-purpose timer
- 2x watchdog timer (WDT)
- 1x real-time counter (RTC)
- 1x IrDA
- 1x temperature sensor
- 1x touch sensor (TOUCH), up to 16 touch sensing I/Os

Packaging

- QFN88 package, 9 x 9 mm
- QFN68 package, 8 x 8 mm
- Operating temperature range: -40 to +85 °C

Applications

- HMI (Human Machine Interface) applications
- Home appliance
  - Refrigerator
  - Air conditioner
  - Thermostat
  - Washing machine
  - Robot cleaner
- Smart plug
- Smart lighting
  - Light bulb
  - Light switch
  - Ceiling light
  - Stand light
- Others
  - Remote controller
  - Toy
  - Drone
  - Industrial terminal
  - Factory automation sensor/switch
  - Smart meter
  - Payment terminal
  - Industrial computer
  - Medical devices
  - Kitchen appliances
  - Home automation switch/sensor
  - Door lock
  - Door camera

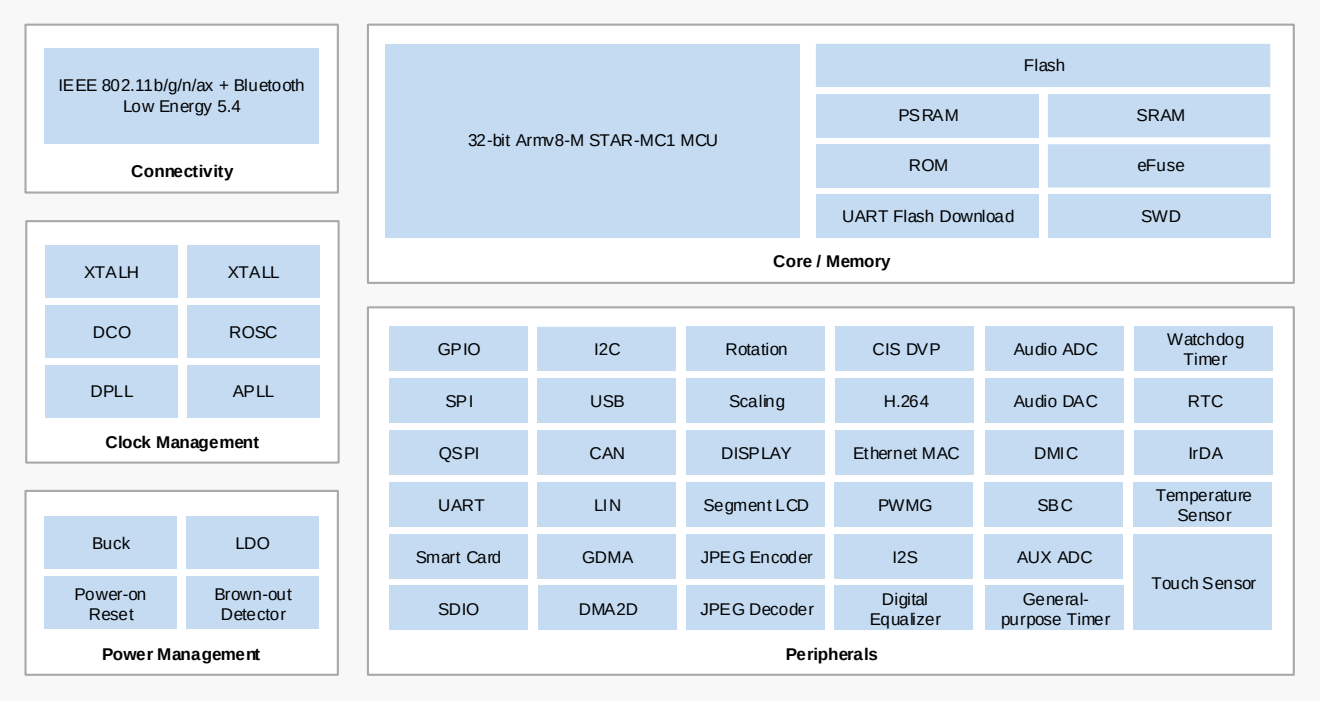
2. Overview

The BK7258 is a highly integrated 1x1 single-band 2.4 GHz Wi-Fi 6 (802.11b/g/n/ax) and Bluetooth Low Energy (LE) 5.4 combo solution designed for applications that require abundant resources and low power consumption. The integration of a 32-bit Armv8-M STAR-MC1 MCU and a comprehensive set of peripherals makes the BK7258 ideal for advanced Internet of Things (IoT) applications.

Using advanced design techniques and ultra-low power process technology, the BK7258 delivers high integration and minimal power consumption for IP cameras, HMI applications, smart locks, and other advanced IoT applications.

Figure 2-1 shows the general block diagram of the BK7258.

Figure 2-1 BK7258 Block Diagram



The BK7258 devices are offered in two packages. The set of included peripherals varies depending on the package. Table 2-1 shows the list of peripherals available on each package.

Table 2-1 Device Options and Features

Feature	QFN88	QFN68
Flash	8 MB	4 MB
PSRAM	8 MB or 16 MB	4 MB

Feature		QFN88	QFN68
GPIO		56	46
SPI	Master/Slave	2	2
QSPI		2	2
UART		3	3
Smart Card controller		1	1
SDIO		1	1
I2C	Master/Slave	2	2
USB		1	1
CAN		1	1
LIN		1	1
GDMA		2	2
DMA2D		1	1
Rotation module		1	1
Scaling Module		2	2
DISPLAY		1	1
Segment LCD controller		1	1
JPEG encoder		1	1
JPEG decoder		1	1
CIS DVP interface		1	-
H.264 video encoder		1	1
Ethernet MAC interface		1	1
PWM	PWM0–11	12	8
I2S	Master/Slave	3	3
Digital equalizer		1	1
Audio ADC		2	-
Audio DAC		Mono	Mono
DMIC		1	1
SBC accelerator		1	1

Feature		QFN88	QFN68
AUX ADC	12 bits	1	1
	Number of channels	11	11
General-purpose timer		6	6
Watchdog timer (WDT)		2	2
Real-time counter (RTC)		1	1
IrDA		1	1
Temperature sensor		1	1
Touch sensing I/O		16	7
Package		9 x 9 mm QFN88	8 x 8 mm QFN68
Operating voltage		2.5 to 4.35 V	
Operating temperature		-40 to +85 ℃	

3. Pin Descriptions

The BK7258 provides Wi-Fi and Bluetooth LE functionality in two packages ranging from 68 pins to 88 pins.

3.1 QFN88 Pin Descriptions

Figure 3-1 shows the pin assignments of the 9 x 9 mm, 88-pin QFN package.

Figure 3-1 QFN88 Pin Assignments

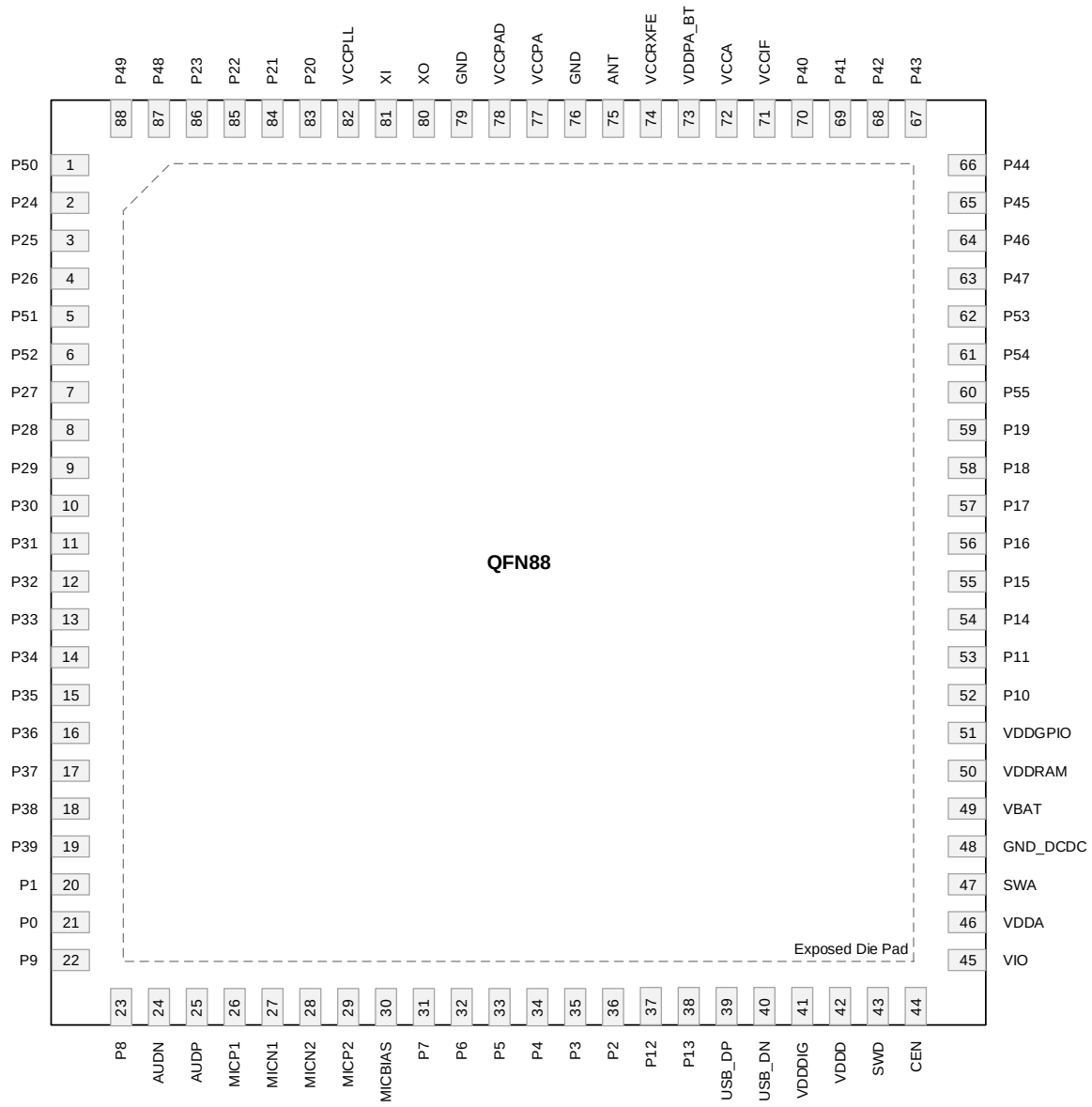


Table 3-1 shows the pin descriptions of the QFN88 package.

Table 3-1 QFN88 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P50	I/O	Digital	• GPIO50: general-purpose I/O • ENET_RXD1: receive data • RGB_R0: red data
2	P24	I/O	Digital/Analog	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWMG0_PWM4: PWMG0 channel PWM4 • ADC2: analog input channel • QSPI0_IO0: data • RGB_G7: green data • I8080_RSX: data/command select • SEG6: segment
3	P25	I/O	Digital/Analog	• GPIO25: general-purpose I/O • IRDA: infrared data • PWMG0_PWM5: PWMG0 channel PWM5 • ADC1: analog input channel • QSPI0_IO1: data • RGB_G6: green data • I8080_WRX: write enable • SEG5: segment
4	P26	I/O	Digital/Analog	• GPIO26: general-purpose I/O • WIFI_TX_EN: Wi-Fi transmit enable • QSPI0_IO2: data • RGB_G5: green data • I8080_RDX: read enable • SEG4: segment
5	P51	I/O	Digital	• GPIO51: general-purpose I/O • ENET_RXDV: receive data valid • RGB_G1: green data
6	P52	I/O	Digital	• GPIO52: general-purpose I/O • ENET_TXD0: transmit data

Pin #	Name	I/O	Type	Description
				• RGB_G0: green data
7	P27	I/O	Digital/Analog	• GPIO27: general-purpose I/O • CIS_MCLK: master clock • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) • ENET_PHY_INT: PHY interrupt • QSPI0_IO3: data • SEG17: segment
8	P28	I/O	Digital/Analog	• GPIO28: general-purpose I/O • WIFI_RX_EN: Wi-Fi receive enable • I2S_MCLK: master clock • ADC4: analog input channel • TOUCH2: touch sensing I/O • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) • SEG18: segment
9	P29	I/O	Digital/Analog	• GPIO29: general-purpose I/O • CIS_PCLK: pixel clock • ENET_MDC: management data clock • TOUCH3: touch sensing I/O • SEG19: segment
10	P30	I/O	Digital/Analog	• GPIO30: general-purpose I/O • CIS_HSYNC: horizontal synchronization • UART2_RX: receive data input • LIN_RXD: receive data input • TOUCH4: touch sensing I/O • SC_CLK: clock • SEG20: segment
11	P31	I/O	Digital/Analog	• GPIO31: general-purpose I/O • CIS_VSYNC: vertical synchronization • UART2_TX: transmit data output • LIN_TXD: transmit data output • TOUCH5: touch sensing I/O • SC_IO: data input/output

Pin #	Name	I/O	Type	Description
				• SEG21: segment
12	P32	I/O	Digital/Analog	• GPIO32: general-purpose I/O • CIS_PXD0: data • PWMG1_PWM0: PWMG1 channel PWM0 • ENET_MDIO: management data • TOUCH6: touch sensing I/O • SC_RSTN: reset • SEG22: segment
13	P33	I/O	Digital/Analog	• GPIO33: general-purpose I/O • CIS_PXD1: data • PWMG1_PWM1: PWMG1 channel PWM1 • ENET_RXD0: receive data • TOUCH7: touch sensing I/O • SPI0_SCK: serial clock • SEG23: segment
14	P34	I/O	Digital/Analog	• GPIO34: general-purpose I/O • CIS_PXD2: data • PWMG1_PWM2: PWMG1 channel PWM2 • ENET_RXD1: receive data • TOUCH8: touch sensing I/O • SPI0_CSN: chip select • SEG24: segment
15	P35	I/O	Digital/Analog	• GPIO35: general-purpose I/O • CIS_PXD3: data • PWMG1_PWM3: PWMG1 channel PWM3 • ENET_RXDV: receive data valid • TOUCH9: touch sensing I/O • SPI0_MOSI: master out slave in • SEG25: segment
16	P36	I/O	Digital/Analog	• GPIO36: general-purpose I/O • CIS_PXD4: data • PWMG1_PWM4: PWMG1 channel

Pin #	Name	I/O	Type	Description
				PWM4 • ENET_TXD0: transmit data • TOUCH10: touch sensing I/O • SPI0_MISO: master in slave out • SEG26: segment
17	P37	I/O	Digital/Analog	• GPIO37: general-purpose I/O • CIS_PXD5: data • PWMG1_PWM5: PWMG1 channel PWM5 • ENET_TXD1: transmit data • TOUCH11: touch sensing I/O • SEG27: segment
18	P38	I/O	Digital/Analog	• GPIO38: general-purpose I/O • CIS_PXD6: data • I2C1_SCL: serial clock • ENET_TXEN: transmit data enable • TOUCH12: touch sensing I/O • COM4: common • SEG28: segment
19	P39	I/O	Digital/Analog	• GPIO39: general-purpose I/O • CIS_PXD7: data • I2C1_SDA: serial data • ENET_REF_CLK: RMII reference clock • TOUCH13: touch sensing I/O • COM5: common • SEG29: segment
20	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data • SWDIO: serial wire data • SC_CLK: clock • ADC13: analog input channel • LIN_RXD: receive data input
21	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • UART1_TX: transmit data output

Pin #	Name	I/O	Type	Description
				• I2C1_SCL: serial clock • SWCLK: serial wire clock • SC_IO: data input/output • ADC12: analog input channel • LIN_TXD: transmit data output
22	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O • BT_PRIOPRITY: Bluetooth priority • PWMG0_PWM3: PWMG0 channel PWM3 • I2S0_DOUT: serial data output • DMIC_DAT: data • 32K_XI: 32.768 kHz crystal input
23	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • BT_ACTIVE: Bluetooth active • PWMG0_PWM2: PWMG0 channel PWM2 • I2S0_DIN: serial data input • DMIC_CLK: clock • ADC10: analog input channel • 32K_XO: 32.768 kHz crystal output
24	AUDN	-	Analog output	Audio channel negative output
25	AUDP	-	Analog output	Audio channel positive output
26	MICP1	-	Analog input	Microphone 1 positive input
27	MICN1	-	Analog input	Microphone 1 negative input
28	MICN2	-	Analog input	Microphone 2 negative input
29	MICP2	-	Analog input	Microphone 2 positive input
30	MICBIAS	-	Analog output	Microphone bias output
31	P7	I/O	Digital	• GPIO7: general-purpose I/O • WIFI_ACTIVE: Wi-Fi active • PWMG0_PWM1: PWMG0 channel PWM1 • I2S0_SYNC: frame synchronization • QSPI1_IO3: data
32	P6	I/O	Digital	• GPIO6: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• CLK13M: 26 MHz clock output (divide by 1/2/4/8) • PWMG0_PWM0: PWMG0 channel PWM0 • I2S0_SCK: serial clock • QSPI1_IO2: data
33	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • SPI1_MISO: master in slave out • SDIO_DATA1: data • COM7: common • QSPI1_IO1: data • SEG31: segment
34	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O • SPI1_MOSI: master out slave in • SDIO_DATA0: data • COM6: common • QSPI1_IO0: data • SEG30: segment
35	P3	I/O	Digital	• GPIO3: general-purpose I/O • SPI1_CSN: chip select • SDIO_CMD: command/response • SC_VCC: power supply to the smart card • QSPI1_CS: chip select
36	P2	I/O	Digital	• GPIO2: general-purpose I/O • SPI1_SCK: serial clock • SDIO_CLK: clock • SC_RSTN: reset • LIN_SLEEP: transceiver sleep mode (active low) • QSPI1_SCK: serial clock
37	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • UART0_RTS: request to send • TOUCH0: touch sensing I/O • ADC14: analog input channel
38	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• UART0_CTS: clear to send • TOUCH1: touch sensing I/O • ADC15: analog input channel
39	USB_DP	I/O	Digital	USB D+
40	USB_DN	I/O	Digital	USB D-
41	VDDDIG	-	Analog output	Digital core LDO output
42	VDDD	-	Analog output	Digital buck/LDO output
43	SWD	-	Analog output	Digital buck switch output
44	CEN	-	Analog input	Chip enable, active high
45	VIO	-	Analog output	IO LDO output
46	VDDA	-	Analog output	Analog buck/LDO output
47	SWA	-	Analog output	Analog buck switch output
48	GND_DCDC	-	GND	Buck ground
49	VBAT	-	Power	Chip power supply
50	VDDRAM	-	Analog output	EXMEM LDO output
51	VDDGPIO	-	Analog output	Power supply for GPIOs
52	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input • UART0_RX: receive data input • SDIO_DATA2: data • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
53	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output • UART0_TX: transmit data output • SDIO_DATA3: data
54	P14	I/O	Digital/Analog	• GPIO14: general-purpose I/O • SDIO_CLK: clock • SPI0_SCK: serial clock • BT_ANT0: Bluetooth antenna select

Pin #	Name	I/O	Type	Description
				• I2C1_SCL: serial clock • RGB_DCLK: clock output • I8080_D15: data • SEG16: segment
55	P15	I/O	Digital/Analog	• GPIO15: general-purpose I/O • SDIO_CMD: command/response • SPI0_CSN: chip select • BT_ANT1: Bluetooth antenna select • I2C1_SDA: serial data • RGB_DISP: display on enable • I8080_D14: data • SEG15: segment
56	P16	I/O	Digital/Analog	• GPIO16: general-purpose I/O • SDIO_DATA0: data • SPI0_MOSI: master out slave in • BT_ANT2: Bluetooth antenna select • RGB_DE: data enable • I8080_D13: data • SEG14: segment
57	P17	I/O	Digital/Analog	• GPIO17: general-purpose I/O • SDIO_DATA1: data • SPI0_MISO: master in slave out • BT_ANT3: Bluetooth antenna select • RGB_HSYNC: horizontal synchronization • I8080_D12: data • SEG13: segment
58	P18	I/O	Digital/Analog	• GPIO18: general-purpose I/O • SDIO_DATA2: data • PWMG0_PWM0: PWMG0 channel PWM0 • RGB_VSYNC: vertical synchronization • I8080_D11: data • SEG12: segment
59	P19	I/O	Digital/Analog	• GPIO19: general-purpose I/O • SDIO_DATA3: data

Pin #	Name	I/O	Type	Description
				• PWMG0_PWM1: PWMG0 channel PWM1 • RGB_R7: red data • I8080_D10: data • SEG11: segment
60	P55	I/O	Digital	• GPIO55: general-purpose I/O • ENET_REF_CLK: RMII reference clock • RGB_B0: blue data
61	P54	I/O	Digital	• GPIO54: general-purpose I/O • ENET_TXEN: transmit data enable • RGB_B1: blue data
62	P53	I/O	Digital	• GPIO53: general-purpose I/O • ENET_TXD1: transmit data • RGB_B2: blue data
63	P47	I/O	Digital/Analog	• GPIO47: general-purpose I/O • SPI0_MISO: master in slave out • ENET_MDC: management data clock • TOUCH15: touch sensing I/O • RGB_B3: blue data • I8080_D0: data • COM0: common • I2S2_DOUT: serial data output
64	P46	I/O	Digital/Analog	• GPIO46: general-purpose I/O • CAN_STBY: transceiver standby mode (active high) • SPI0_MOSI: master out slave in • ENET_PHY_INT: PHY interrupt • TOUCH14: touch sensing I/O • RGB_B4: blue data • I8080_D1: data • COM1: common • I2S2_DIN: serial data input
65	P45	I/O	Digital/Analog	• GPIO45: general-purpose I/O • CAN_RX: receive • SPI0_CSN: chip select

Pin #	Name	I/O	Type	Description
				• RGB_B5: blue data • I8080_D2: data • COM2: common • I2S2_SYNC: frame synchronization
66	P44	I/O	Digital/Analog	• GPIO44: general-purpose I/O • CAN_TX: transmit • SPI0_SCK: serial clock • RGB_B6: blue data • I8080_D3: data • COM3: common • I2S2_SCK: serial clock
67	P43	I/O	Digital/Analog	• GPIO43: general-purpose I/O • I2C1_SDA: serial data • I2S1_DOUT: serial data output • SC_VCC: power supply to the smart card • RGB_B7: blue data • I8080_D4: data • SEG0: segment
68	P42	I/O	Digital/Analog	• GPIO42: general-purpose I/O • I2C1_SCL: serial clock • I2S1_DIN: serial data input • LIN_SLEEP: transceiver sleep mode (active low) • SC_RSTN: reset • RGB_G2: green data • I8080_D5: data • SEG1: segment
69	P41	I/O	Digital/Analog	• GPIO41: general-purpose I/O • UART2_TX: transmit data output • I2S1_SYNC: frame synchronization • LIN_TXD: transmit data output • SC_IO: data input/output • RGB_G3: green data • I8080_D6: data • SEG2: segment

Pin #	Name	I/O	Type	Description
70	P40	I/O	Digital/Analog	• GPIO40: general-purpose I/O • UART2_RX: receive data input • I2S1_SCK: serial clock • LIN_RXD: receive data input • SC_CLK: clock • RGB_G4: green data • I8080_D7: data • SEG3: segment
71	VCCIF	-	Analog input	IF power supply
72	VCCA	-	Analog input	Analog power supply
73	VDDPA_BT	-	Analog output	Bluetooth RF PA LDO output
74	VCCRXFE	-	Analog input	RF receiver power supply
75	ANT	-	RF	2.4 GHz RF signal port
76	GND	-	GND	Ground
77	VCCPA	-	Analog input	RF PA power supply
78	VCCPAD	-	Analog input	RF PA driver power supply
79	GND	-	GND	Ground
80	XO	-	Analog output	26 MHz crystal output
81	XI	-	Analog input	26 MHz crystal input
82	VCCPLL	-	Analog input	RF PLL power supply
83	P20	I/O	Digital/Analog	• GPIO20: general-purpose I/O • I2C0_SCL: serial clock • SWCLK: serial wire clock • RGB_R6: red data • I8080_D9: data • SEG10: segment
84	P21	I/O	Digital/Analog	• GPIO21: general-purpose I/O • I2C0_SDA: serial data • SWDIO: serial wire data • ADC6: analog input channel • RGB_R5: red data • I8080_D8: data

Pin #	Name	I/O	Type	Description
				• SEG9: segment
85	P22	I/O	Digital/Analog	• GPIO22: general-purpose I/O • CLK26M: 26 MHz clock output • PWMG0_PWM2: PWMG0 channel PWM2 • ADC5: analog input channel • QSPI0_SCK: serial clock • RGB_R4: red data • I8080_CSX: chip select • SEG8: segment
86	P23	I/O	Digital/Analog	• GPIO23: general-purpose I/O • PWMG0_PWM3: PWMG0 channel PWM3 • ADC3: analog input channel • QSPI0_CS: chip select • RGB_R3: red data • I8080_RESET: reset • SEG7: segment
87	P48	I/O	Digital	• GPIO48: general-purpose I/O • ENET_MDIO: management data • RGB_R2: red data • I8080_D16: data
88	P49	I/O	Digital	• GPIO49: general-purpose I/O • ENET_RXD0: receive data • RGB_R1: red data • I8080_D17: data
Die pad	GND_SLUG	-	GND	Ground

3.2 QFN68 Pin Descriptions

Figure 3-2 shows the pin assignments of the 8 x 8 mm, 68-pin QFN package.

Figure 3-2 QFN68 Pin Assignments

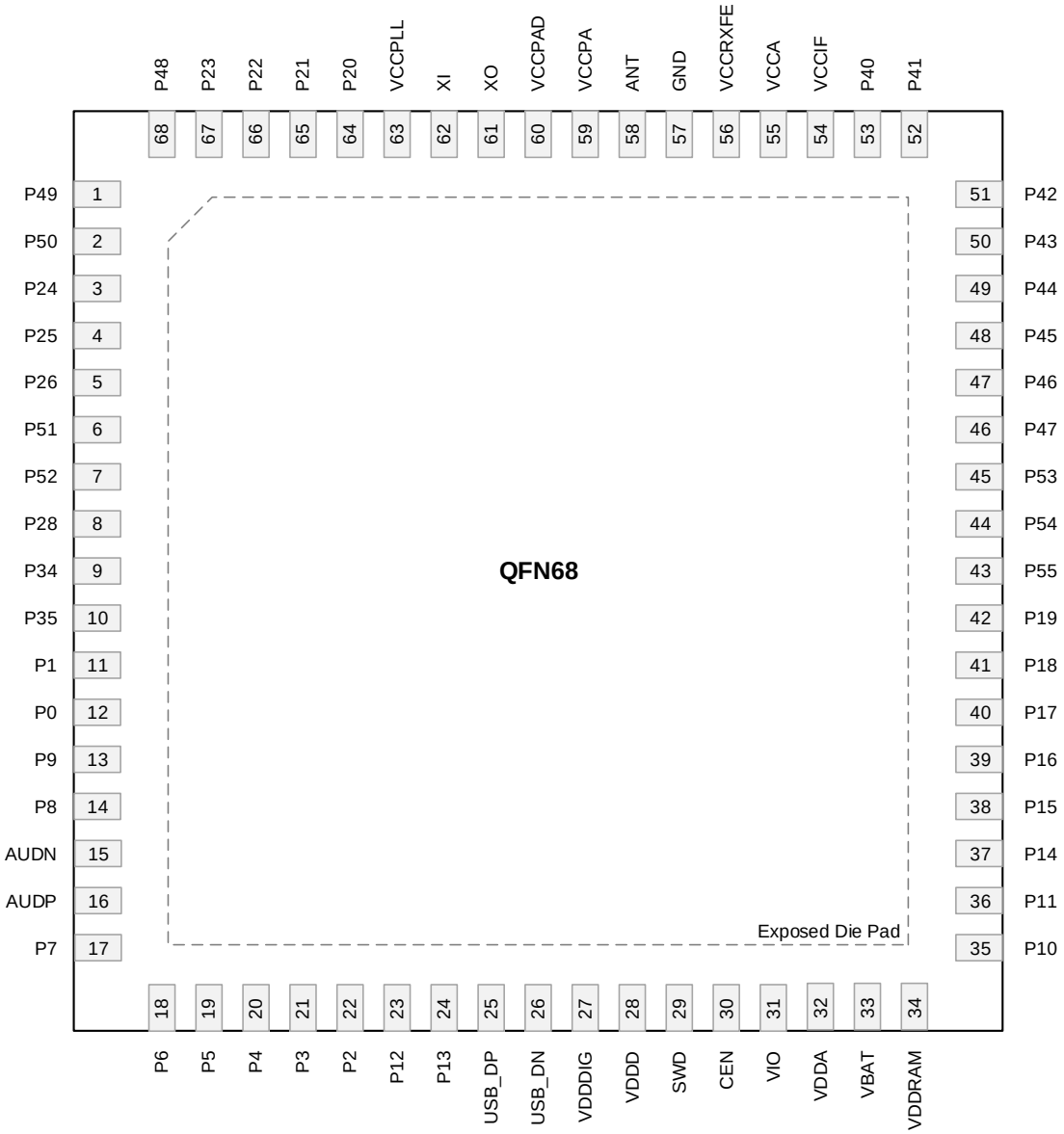


Table 3-2 shows the pin descriptions of the QFN68 package.

Table 3-2 QFN68 Pin Descriptions

Pin #	Name	I/O	Type	Description
1	P49	I/O	Digital	• GPIO49: general-purpose I/O • ENET_RXD0: receive data • RGB_R1: red data • I8080_D17: data

Pin #	Name	I/O	Type	Description
2	P50	I/O	Digital	• GPIO50: general-purpose I/O • ENET_RXD1: receive data • RGB_R0: red data
3	P24	I/O	Digital/Analog	• GPIO24: general-purpose I/O • LPO_CLK: 32 kHz clock output • PWMG0_PWM4: PWMG0 channel PWM4 • ADC2: analog input channel • QSPI0_IO0: data • RGB_G7: green data • I8080_RSX: data/command select • SEG6: segment
4	P25	I/O	Digital/Analog	• GPIO25: general-purpose I/O • IRDA: infrared data • PWMG0_PWM5: PWMG0 channel PWM5 • ADC1: analog input channel • QSPI0_IO1: data • RGB_G6: green data • I8080_WRX: write enable • SEG5: segment
5	P26	I/O	Digital/Analog	• GPIO26: general-purpose I/O • WIFI_TX_EN: Wi-Fi transmit enable • QSPI0_IO2: data • RGB_G5: green data • I8080_RDX: read enable • SEG4: segment
6	P51	I/O	Digital	• GPIO51: general-purpose I/O • ENET_RXDV: receive data valid • RGB_G1: green data
7	P52	I/O	Digital	• GPIO52: general-purpose I/O • ENET_TXD0: transmit data • RGB_G0: green data
8	P28	I/O	Digital/Analog	• GPIO28: general-purpose I/O • WIFI_RX_EN: Wi-Fi receive enable

Pin #	Name	I/O	Type	Description
				• I2S_MCLK: master clock • ADC4: analog input channel • TOUCH2: touch sensing I/O • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M) • SEG18: segment
9	P34	I/O	Digital/Analog	• GPIO34: general-purpose I/O • PWMG1_PWM2: PWMG1 channel PWM2 • ENET_RXD1: receive data • TOUCH8: touch sensing I/O • SPI0_CSN: chip select • SEG24: segment
10	P35	I/O	Digital/Analog	• GPIO35: general-purpose I/O • PWMG1_PWM3: PWMG1 channel PWM3 • ENET_RXDV: receive data valid • TOUCH9: touch sensing I/O • SPI0_MOSI: master out slave in • SEG25: segment
11	P1	I/O	Digital/Analog	• GPIO1: general-purpose I/O • UART1_RX: receive data input • I2C1_SDA: serial data • SWDIO: serial wire data • SC_CLK: clock • ADC13: analog input channel • LIN_RXD: receive data input
12	P0	I/O	Digital/Analog	• GPIO0: general-purpose I/O • UART1_TX: transmit data output • I2C1_SCL: serial clock • SWCLK: serial wire clock • SC_IO: data input/output • ADC12: analog input channel • LIN_TXD: transmit data output
13	P9	I/O	Digital/Analog	• GPIO9: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• BT_PRIOPRITY: Bluetooth priority • PWMG0_PWM3: PWMG0 channel PWM3 • I2S0_DOUT: serial data output • DMIC_DAT: data • 32K_XI: 32.768 kHz crystal input
14	P8	I/O	Digital/Analog	• GPIO8: general-purpose I/O • BT_ACTIVE: Bluetooth active • PWMG0_PWM2: PWMG0 channel PWM2 • I2S0_DIN: serial data input • DMIC_CLK: clock • ADC10: analog input channel • 32K_XO: 32.768 kHz crystal output
15	AUDN	-	Analog output	Audio channel negative output
16	AUDP	-	Analog output	Audio channel positive output
17	P7	I/O	Digital	• GPIO7: general-purpose I/O • WIFI_ACTIVE: Wi-Fi active • PWMG0_PWM1: PWMG0 channel PWM1 • I2S0_SYNC: frame synchronization • QSPI1_IO3: data
18	P6	I/O	Digital	• GPIO6: general-purpose I/O • CLK13M: 26 MHz clock output (divide by 1/2/4/8) • PWMG0_PWM0: PWMG0 channel PWM0 • I2S0_SCK: serial clock • QSPI1_IO2: data
19	P5	I/O	Digital/Analog	• GPIO5: general-purpose I/O • SPI1_MISO: master in slave out • SDIO_DATA1: data • COM7: common • QSPI1_IO1: data • SEG31: segment
20	P4	I/O	Digital/Analog	• GPIO4: general-purpose I/O

Pin #	Name	I/O	Type	Description
				• SPI1_MOSI: master out slave in • SDIO_DATA0: data • COM6: common • QSPI1_IO0: data • SEG30: segment
21	P3	I/O	Digital	• GPIO3: general-purpose I/O • SPI1_CSN: chip select • SDIO_CMD: command/response • SC_VCC: power supply to the smart card • QSPI1_CS: chip select
22	P2	I/O	Digital	• GPIO2: general-purpose I/O • SPI1_SCK: serial clock • SDIO_CLK: clock • SC_RSTN: reset • LIN_SLEEP: transceiver sleep mode (active low) • QSPI1_SCK: serial clock
23	P12	I/O	Digital/Analog	• GPIO12: general-purpose I/O • UART0_RTS: request to send • TOUCH0: touch sensing I/O • ADC14: analog input channel
24	P13	I/O	Digital/Analog	• GPIO13: general-purpose I/O • UART0_CTS: clear to send • TOUCH1: touch sensing I/O • ADC15: analog input channel
25	USB_DP	I/O	Digital	USB D+
26	USB_DN	I/O	Digital	USB D-
27	VDDDIG	-	Analog output	Digital core LDO output
28	VDDD	-	Analog output	Digital buck/LDO output
29	SWD	-	Analog output	Digital buck switch output
30	CEN	-	Analog input	Chip enable, active high
31	VIO	-	Analog output	IO LDO output
32	VDDA	-	Analog output	Analog buck/LDO output

Pin #	Name	I/O	Type	Description
33	VBAT	-	Power	Chip power supply
34	VDDRAM	-	Analog output	EXMEM LDO output
35	P10	I/O	Digital	• GPIO10: general-purpose I/O • DL_UART_RX: UART flash download receive data input • UART0_RX: receive data input • SDIO_DATA2: data • CLK_AUXS_CIS: CIS master clock (derived from DCO/APLL/CLK_320M/ CLK_480M)
36	P11	I/O	Digital	• GPIO11: general-purpose I/O • DL_UART_TX: UART flash download transmit data output • UART0_TX: transmit data output • SDIO_DATA3: data
37	P14	I/O	Digital/Analog	• GPIO14: general-purpose I/O • SDIO_CLK: clock • SPI0_SCK: serial clock • BT_ANT0: Bluetooth antenna select • I2C1_SCL: serial clock • RGB_DCLK: clock output • I8080_D15: data • SEG16: segment
38	P15	I/O	Digital/Analog	• GPIO15: general-purpose I/O • SDIO_CMD: command/response • SPI0_CSN: chip select • BT_ANT1: Bluetooth antenna select • I2C1_SDA: serial data • RGB_DISP: display on enable • I8080_D14: data • SEG15: segment
39	P16	I/O	Digital/Analog	• GPIO16: general-purpose I/O • SDIO_DATA0: data • SPI0_MOSI: master out slave in • BT_ANT2: Bluetooth antenna select

Pin #	Name	I/O	Type	Description
				• RGB_DE: data enable • I8080_D13: data • SEG14: segment
40	P17	I/O	Digital/Analog	• GPIO17: general-purpose I/O • SDIO_DATA1: data • SPI0_MISO: master in slave out • BT_ANT3: Bluetooth antenna select • RGB_HSYNC: horizontal synchronization • I8080_D12: data • SEG13: segment
41	P18	I/O	Digital/Analog	• GPIO18: general-purpose I/O • SDIO_DATA2: data • PWMG0_PWM0: PWMG0 channel PWM0 • RGB_VSYNC: vertical synchronization • I8080_D11: data • SEG12: segment
42	P19	I/O	Digital/Analog	• GPIO19: general-purpose I/O • SDIO_DATA3: data • PWMG0_PWM1: PWMG0 channel PWM1 • RGB_R7: red data • I8080_D10: data • SEG11: segment
43	P55	I/O	Digital	• GPIO55: general-purpose I/O • ENET_REF_CLK: RMII reference clock • RGB_B0: blue data
44	P54	I/O	Digital	• GPIO54: general-purpose I/O • ENET_TXEN: transmit data enable • RGB_B1: blue data
45	P53	I/O	Digital	• GPIO53: general-purpose I/O • ENET_TXD1: transmit data • RGB_B2: blue data
46	P47	I/O	Digital/Analog	• GPIO47: general-purpose I/O • SPI0_MISO: master in slave out

Pin #	Name	I/O	Type	Description
				• ENET_MDC: management data clock • TOUCH15: touch sensing I/O • RGB_B3: blue data • I8080_D0: data • COM0: common • I2S2_DOUT: serial data output
47	P46	I/O	Digital/Analog	• GPIO46: general-purpose I/O • CAN_STBY: transceiver standby mode (active high) • SPI0_MOSI: master out slave in • ENET_PHY_INT: PHY interrupt • TOUCH14: touch sensing I/O • RGB_B4: blue data • I8080_D1: data • COM1: common • I2S2_DIN: serial data input
48	P45	I/O	Digital/Analog	• GPIO45: general-purpose I/O • CAN_RX: receive • SPI0_CSN: chip select • RGB_B5: blue data • I8080_D2: data • COM2: common • I2S2_SYNC: frame synchronization
49	P44	I/O	Digital/Analog	• GPIO44: general-purpose I/O • CAN_TX: transmit • SPI0_SCK: serial clock • RGB_B6: blue data • I8080_D3: data • COM3: common • I2S2_SCK: serial clock
50	P43	I/O	Digital/Analog	• GPIO43: general-purpose I/O • I2C1_SDA: serial data • I2S1_DOUT: serial data output • SC_VCC: power supply to the smart card • RGB_B7: blue data

Pin #	Name	I/O	Type	Description
				• I8080_D4: data • SEG0: segment
51	P42	I/O	Digital/Analog	• GPIO42: general-purpose I/O • I2C1_SCL: serial clock • I2S1_DIN: serial data input • LIN_SLEEP: transceiver sleep mode (active low) • SC_RSTN: reset • RGB_G2: green data • I8080_D5: data • SEG1: segment
52	P41	I/O	Digital/Analog	• GPIO41: general-purpose I/O • UART2_TX: transmit data output • I2S1_SYNC: frame synchronization • LIN_TXD: transmit data output • SC_IO: data input/output • RGB_G3: green data • I8080_D6: data • SEG2: segment
53	P40	I/O	Digital/Analog	• GPIO40: general-purpose I/O • UART2_RX: receive data input • I2S1_SCK: serial clock • LIN_RXD: receive data input • SC_CLK: clock • RGB_G4: green data • I8080_D7: data • SEG3: segment
54	VCCIF	-	Analog input	IF power supply
55	VCCA	-	Analog input	Analog power supply
56	VCCRXFE	-	Analog input	RF receiver power supply
57	GND	-	GND	Ground
58	ANT	-	RF	2.4 GHz RF signal port
59	VCCPA	-	Analog input	RF PA power supply

Pin #	Name	I/O	Type	Description
60	VCCPAD	-	Analog input	RF PA driver power supply
61	XO	-	Analog output	26 MHz crystal output
62	XI	-	Analog input	26 MHz crystal input
63	VCCPLL	-	Analog input	RF PLL power supply
64	P20	I/O	Digital/Analog	• GPIO20: general-purpose I/O • I2C0_SCL: serial clock • SWCLK: serial wire clock • RGB_R6: red data • I8080_D9: data • SEG10: segment
65	P21	I/O	Digital/Analog	• GPIO21: general-purpose I/O • I2C0_SDA: serial data • SWDIO: serial wire data • ADC6: analog input channel • RGB_R5: red data • I8080_D8: data • SEG9: segment
66	P22	I/O	Digital/Analog	• GPIO22: general-purpose I/O • CLK26M: 26 MHz clock output • PWMG0_PWM2: PWMG0 channel PWM2 • ADC5: analog input channel • QSPI0_SCK: serial clock • RGB_R4: red data • I8080_CSX: chip select • SEG8: segment
67	P23	I/O	Digital/Analog	• GPIO23: general-purpose I/O • PWMG0_PWM3: PWMG0 channel PWM3 • ADC3: analog input channel • QSPI0_CS: chip select • RGB_R3: red data • I8080_RESET: reset • SEG7: segment

Pin #	Name	I/O	Type	Description
68	P48	I/O	Digital	• GPIO48: general-purpose I/O • ENET_MDIO: management data • RGB_R2: red data • I8080_D16: data
Die pad	GND_SLUG	-	GND	Ground

3.3 Pin Multiplexing

Table 3-3 shows the pin mux functions of GPIOs.

Table 3-3 Pin Multiplexing

GPIO	Flash Download	Alternate Functions							
		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
	UART	UART1/SPI1/Clock /PTA/UART0/SDIO /I2C0/IrDA/ Wi-Fi TX/RX Enable/CIS DVP/ UART2/I2C1/CAN	I2C1/SDIO/ PWMG0/SPI0/ SWD/Clock/ UART2/PWMG1/ I2S1	SWD/I2S0/Clock/ AoA/AoD/AUX ADC/Ethernet MAC/LIN	Smart Card/DMIC/ TOUCH/I2C1/ QSPI0	AUX ADC/LIN/Segment LCD/DISPLAY/Clock/ Smart Card/SPI0	LIN	QSPI1/XTALL/ Segment LCD	Segment LCD/I2S2
GPIO0		UART1_TX	I2C1_SCL	SWCLK	SC_IO	ADC12	LIN_TXD		
GPIO1		UART1_RX	I2C1_SDA	SWDIO	SC_CLK	ADC13	LIN_RXD		
GPIO2		SPI1_SCK	SDIO_CLK		SC_RSTN	LIN_SLEEP		QSPI1_SCK	
GPIO3		SPI1_CSN	SDIO_CMD		SC_VCC			QSPI1_CS	
GPIO4		SPI1_MOSI	SDIO_DATA0			COM6		QSPI1_IO0	SEG30
GPIO5		SPI1_MISO	SDIO_DATA1			COM7		QSPI1_IO1	SEG31
GPIO6		CLK13M	PWMG0_PWM0	I2S0_SCK				QSPI1_IO2	
GPIO7		WIFI_ACTIVE	PWMG0_PWM1	I2S0_SYNC				QSPI1_IO3	
GPIO8		BT_ACTIVE	PWMG0_PWM2	I2S0_DIN	DMIC_CLK	ADC10		32K_XO	
GPIO9		BT_PRIOPRITY	PWMG0_PWM3	I2S0_DOUT	DMIC_DAT			32K_XI	

GPIO	Flash Download	Alternate Functions							
		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
	UART	UART1/SPI1/Clock /PTA/UART0/SDIO /I2C0/IrDA/ Wi-Fi TX/RX Enable/CIS DVP/ UART2/I2C1/CAN	I2C1/SDIO/ PWMG0/SPI0/ SWD/Clock/ UART2/PWMG1/ I2S1	SWD/I2S0/Clock/ AoA/AoD/AUX ADC/Ethernet MAC/LIN	Smart Card/DMIC/ TOUCH/I2C1/ QSPI0	AUX ADC/LIN/Segment LCD/DISPLAY/Clock/ Smart Card/SPI0	LIN	QSPI1/XTALL/ Segment LCD	Segment LCD/I2S2
GPIO10	DL_UART_RX	UART0_RX	SDIO_DATA2	CLK_AUXS_CIS					
GPIO11	DL_UART_TX	UART0_TX	SDIO_DATA3						
GPIO12		UART0_RTS			TOUCH0	ADC14			
GPIO13		UART0_CTS			TOUCH1	ADC15			
GPIO14		SDIO_CLK	SPI0_SCK	BT_ANT0	I2C1_SCL	RGB_DCLK/I8080_D15			SEG16
GPIO15		SDIO_CMD	SPI0_CSN	BT_ANT1	I2C1_SDA	RGB_DISP/I8080_D14			SEG15
GPIO16		SDIO_DATA0	SPI0_MOSI	BT_ANT2		RGB_DE/I8080_D13			SEG14
GPIO17		SDIO_DATA1	SPI0_MISO	BT_ANT3		RGB_HSYNC/I8080_D12			SEG13
GPIO18		SDIO_DATA2	PWMG0_PWM0			RGB_VSYNC/I8080_D11			SEG12
GPIO19		SDIO_DATA3	PWMG0_PWM1			RGB_R7/I8080_D10			SEG11
GPIO20		I2C0_SCL	SWCLK			RGB_R6/I8080_D9			SEG10
GPIO21		I2C0_SDA	SWDIO	ADC6		RGB_R5/I8080_D8			SEG9
GPIO22		CLK26M	PWMG0_PWM2	ADC5	QSPI0_SCK	RGB_R4/I8080_CSX			SEG8
GPIO23			PWMG0_PWM3	ADC3	QSPI0_CS	RGB_R3/I8080_RESET			SEG7
GPIO24		LPO_CLK	PWMG0_PWM4	ADC2	QSPI0_IO0	RGB_G7/I8080_RSX			SEG6

GPIO	Flash Download	Alternate Functions							
		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
	UART	UART1/SPI1/Clock /PTA/UART0/SDIO /I2C0/IrDA/ Wi-Fi TX/RX Enable/CIS DVP/ UART2/I2C1/CAN	I2C1/SDIO/ PWMG0/SPI0/ SWD/Clock/ UART2/PWMG1/ I2S1	SWD/I2S0/Clock/ AoA/AoD/AUX ADC/Ethernet MAC/LIN	Smart Card/DMIC/ TOUCH/I2C1/ QSPI0	AUX ADC/LIN/Segment LCD/DISPLAY/Clock/ Smart Card/SPI0	LIN	QSPI1/XTALL/ Segment LCD	Segment LCD/I2S2
GPIO25		IRDA	PWMG0_PWM5	ADC1	QSPI0_IO1	RGB_G6/I8080_WRX			SEG5
GPIO26		WIFI_TX_EN			QSPI0_IO2	RGB_G5/I8080_RDX			SEG4
GPIO27		CIS_MCLK	CLK_AUXS_CIS	ENET_PHY_INT	QSPI0_IO3				SEG17
GPIO28		WIFI_RX_EN	I2S_MCLK	ADC4	TOUCH2	CLK_AUXS_CIS			SEG18
GPIO29		CIS_PCLK		ENET_MDC	TOUCH3				SEG19
GPIO30		CIS_HSYNC	UART2_RX	LIN_RXD	TOUCH4	SC_CLK			SEG20
GPIO31		CIS_VSYNC	UART2_TX	LIN_TXD	TOUCH5	SC_IO			SEG21
GPIO32		CIS_PXD0	PWMG1_PWM0	ENET_MDIO	TOUCH6	SC_RSTN			SEG22
GPIO33		CIS_PXD1	PWMG1_PWM1	ENET_RXD0	TOUCH7	SPI0_SCK			SEG23
GPIO34		CIS_PXD2	PWMG1_PWM2	ENET_RXD1	TOUCH8	SPI0_CSN			SEG24
GPIO35		CIS_PXD3	PWMG1_PWM3	ENET_RXDV	TOUCH9	SPI0_MOSI			SEG25
GPIO36		CIS_PXD4	PWMG1_PWM4	ENET_TXD0	TOUCH10	SPI0_MISO			SEG26
GPIO37		CIS_PXD5	PWMG1_PWM5	ENET_TXD1	TOUCH11				SEG27
GPIO38		CIS_PXD6	I2C1_SCL	ENET_TXEN	TOUCH12			COM4	SEG28
GPIO39		CIS_PXD7	I2C1_SDA	ENET_REF_CLK	TOUCH13			COM5	SEG29

GPIO	Flash Download	Alternate Functions							
		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
	UART	UART1/SPI1/Clock /PTA/UART0/SDIO /I2C0/IrDA/ Wi-Fi TX/RX Enable/CIS DVP/ UART2/I2C1/CAN	I2C1/SDIO/ PWMG0/SPI0/ SWD/Clock/ UART2/PWMG1/ I2S1	SWD/I2S0/Clock/ AoA/AoD/AUX ADC/Ethernet MAC/LIN	Smart Card/DMIC/ TOUCH/I2C1/ QSPI0	AUX ADC/LIN/Segment LCD/DISPLAY/Clock/ Smart Card/SPI0	LIN	QSPI1/XTALL/ Segment LCD	Segment LCD/I2S2
GPIO40		UART2_RX	I2S1_SCK	LIN_RXD	SC_CLK	RGB_G4/I8080_D7			SEG3
GPIO41		UART2_TX	I2S1_SYNC	LIN_TXD	SC_IO	RGB_G3/I8080_D6			SEG2
GPIO42		I2C1_SCL	I2S1_DIN	LIN_SLEEP	SC_RSTN	RGB_G2/I8080_D5			SEG1
GPIO43		I2C1_SDA	I2S1_DOUT		SC_VCC	RGB_B7/I8080_D4			SEG0
GPIO44		CAN_TX	SPI0_SCK			RGB_B6/I8080_D3		COM3	I2S2_SCK
GPIO45		CAN_RX	SPI0_CSN			RGB_B5/I8080_D2		COM2	I2S2_SYNC
GPIO46		CAN_STBY	SPI0_MOSI	ENET_PHY_INT	TOUCH14	RGB_B4/I8080_D1		COM1	I2S2_DIN
GPIO47			SPI0_MISO	ENET_MDC	TOUCH15	RGB_B3/I8080_D0		COM0	I2S2_DOUT
GPIO48				ENET_MDIO		RGB_R2/I8080_D16			
GPIO49				ENET_RXD0		RGB_R1/I8080_D17			
GPIO50				ENET_RXD1		RGB_R0			
GPIO51				ENET_RXDV		RGB_G1			
GPIO52				ENET_TXD0		RGB_G0			
GPIO53				ENET_TXD1		RGB_B2			
GPIO54				ENET_TXEN		RGB_B1			

GPIO	Flash Download	Alternate Functions							
		AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
	UART	UART1/SPI1/Clock /PTA/UART0/SDIO /I2C0/IrDA/ Wi-Fi TX/RX Enable/CIS DVP/ UART2/I2C1/CAN	I2C1/SDIO/ PWMG0/SPI0/ SWD/Clock/ UART2/PWMG1/ I2S1	SWD/I2S0/Clock/ AoA/AoD/AUX ADC/Ethernet MAC/LIN	Smart Card/DMIC/ TOUCH/I2C1/ QSPI0	AUX ADC/LIN/Segment LCD/DISPLAY/Clock/ Smart Card/SPI0	LIN	QSPI1/XTALL/ Segment LCD	Segment LCD/I2S2
GPIO55				ENET_REF_CLK		RGB_B0			

4. Functional Description

4.1 Wi-Fi/Bluetooth Transceiver

The BK7258 integrates a high-performance Wi-Fi/Bluetooth transceiver. The transceiver incorporates two on-chip baluns. On the receive side, the on-chip balun converts the single-ended (unbalanced) RF signal from the antenna into a differential (balanced) signal and the low noise amplifier (LNA) amplifies the differential signal to achieve a better noise and linearity trade-off. On the transmit side, the power amplifier (PA) amplifies the differential signal and the on-chip balun converts the differential signal to a single-ended signal for feeding the antenna. This enables transmit and receive operations with only one ANT pin connected to the antenna. The communication range can be extended by configuring GPIO26 and GPIO28 as TX_EN and RX_EN function to control external PA and LNA. The frequency synthesizer is fully integrated, eliminating the need for any external components.

4.2 Bluetooth/Wi-Fi Coexistence

The built-in packet traffic arbitration (PTA) ensures stable Bluetooth and Wi-Fi dual connectivity and enables efficient sharing of over-the-air resources.

4.3 Clock Management

The primary clock sources available in the BK7258 are as follows:

- High-frequency clocks
  - 26 MHz crystal oscillator: it outputs clock signal XTALH
  - 26–360 MHz internal digitally controlled oscillator (DCO): it outputs clock signal CLK_DCO
  - Digital PLL (DPLL): it generates 320 MHz clock CLK_320M and 480 MHz clock CLK_480M
- Low-frequency clocks
  - 32 kHz (32.768 kHz) crystal oscillator: it outputs clock signal XTALL
  - 32 kHz internal ring oscillator (ROSC): it outputs clock signal CLK_ROSC
- Audio clock
  - Audio PLL (APLL): its default frequency is 98.304 MHz, and it outputs clock signal CLK_APLL

The system generates a low-power clock source LPO_CLK for standby. The LPO_CLK can be selected from the following clocks:

- 32 kHz crystal oscillator XTALL
- 32 kHz clock signal derived from 26 MHz crystal oscillator
- 32 kHz internal oscillator ROSC

The BK7258 also has a clock output capability, which allows clock signals to be output to external components through GPIOs. GPIOs can output the following clock signals:

- CLK13M: clock derived from CLK_XTAL (factor 1/2/4/8)
- CLK26M: high-frequency crystal clock CLK_XTAL, generally 26 MHz
- LPO_CLK: LPO_CLK clock
- I2S_MCLK: reference clock for external audio codec, derived from APLL
- CLK_AUXS_CIS: reference clock for external CMOS image sensor (CIS)
- CIS_MCLK: reference clock for external CMOS image sensor (CIS)

4.4 Reset

A reset can be triggered by the following sources: power-on reset, brown-out reset, watchdog reset, and wake-up from shutdown mode or deep sleep mode.

Power-on reset, brown-out reset, and AWDT watchdog reset reset the whole chip to its initial state. The DWDT watchdog reset's reset scope is configurable and can be configured to reset the whole chip.

Wake-up from shutdown mode triggers the whole system reset, while wake-up from deep sleep mode triggers the reset of digital blocks.

4.5 Power Management

4.5.1 Power Scheme

The power management system on the BK7258 includes two buck converters and several internal LDO regulators to provide voltage and noise isolation to various parts of the chip.

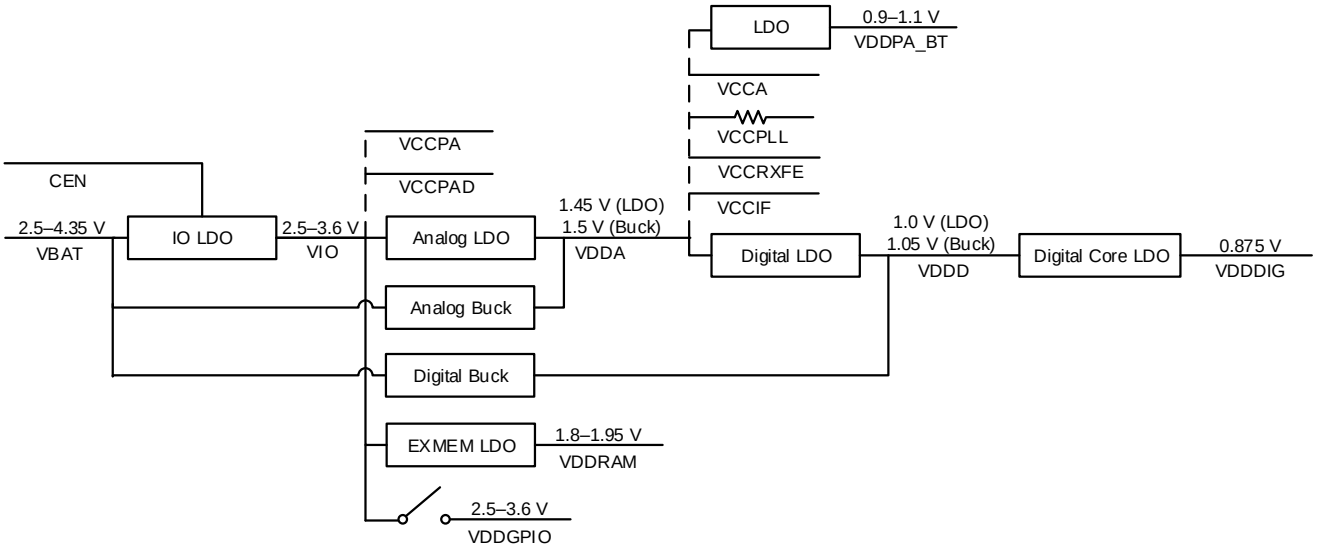
The VBAT is the external main chip supply ranging from 2.5 to 4.35 V. The VBAT generates VIO through the IO LDO regulator. In addition to being the power supply for Wi-Fi PA and GPIOs, the VIO is also the input supply of analog LDO, analog buck, digital buck, and EXMEM LDO. The VBAT also generates VDDA and VDDD through the analog buck converter and the digital buck converter, respectively. The LDOs and bucks generate the following main power supplies:

- VDDA: power supply for RF/analog blocks. It is externally connected to VCCA/VCCPLL/VCCRXFE/ VCCIF to supply power to Wi-Fi/Bluetooth transceiver, and internally provides power supply to XTAL and AUDIO directly.

- VDDDIG: power supply for digital domain. It provides power supply for the processor, memory, Wi-Fi and Bluetooth baseband, as well as various peripherals.
- VDDRAM: power supply for PSRAM.

Figure 4-1 shows the power distribution of the BK7258.

Figure 4-1 Internal Power Distribution



Note: Outputs from the buck converters and LDO regulators require proper bypass capacitors to reduce supply noise. Please refer to the hardware schematic for details on selecting bypass capacitors.

Figure 4-2 shows the power-up sequence of the BK7258.

Figure 4-2 BK7258 Power-up Sequence

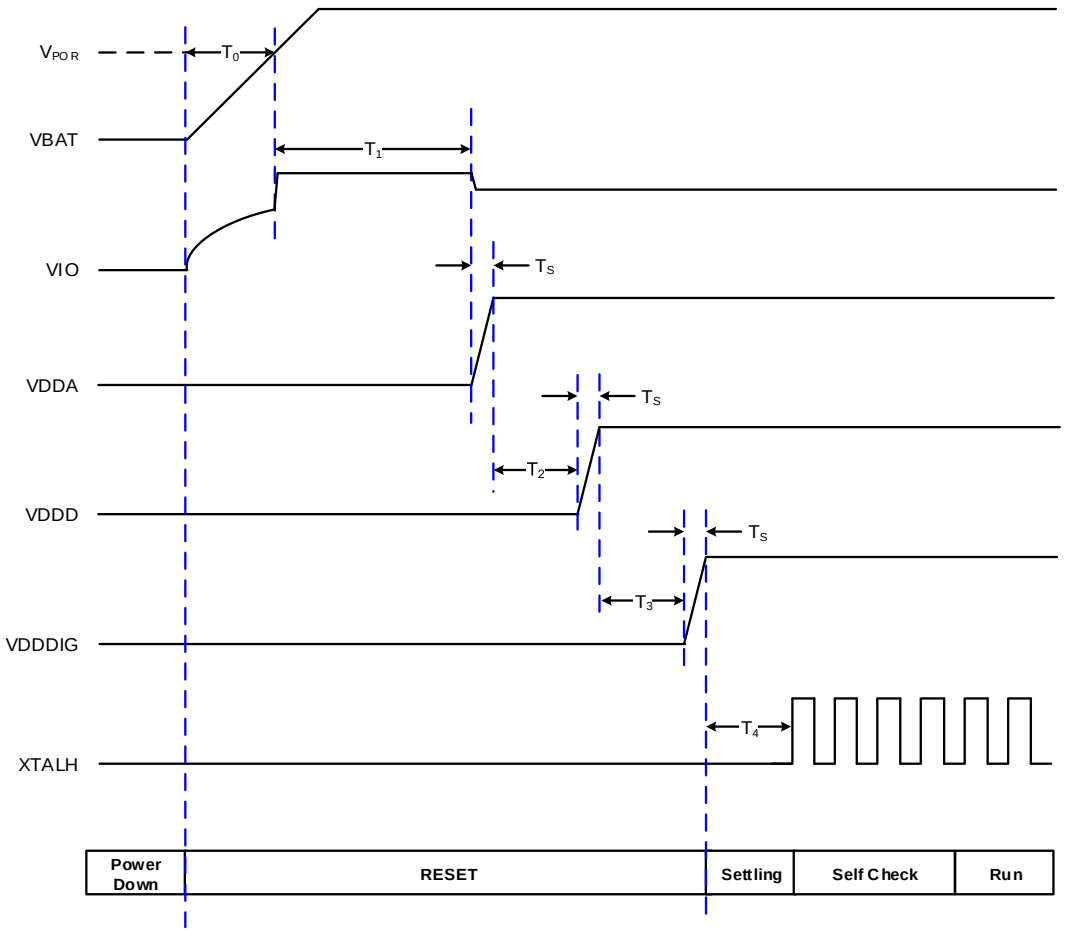


Table 4-1 Timing Parameters of Power-up Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{POR}	VBAT POR threshold	-	1.95	-	V
T_0	IO LDO settle time	200	-	-	µs
T_1(1)	IO LDO ready time	-	-	500	µs
T_2	Analog buck/LDO ready time	-	240	500	µs
T_3	Digital buck/LDO ready time	-	240	500	µs
T_4	Digital core LDO ready time/XTALH stable time	100	-	-	µs
T_S	LDO (excl. IO LDO) settle time	0	-	-	µs

(1) If the VBAT slew rate is greater than 3.3 kV/s, VIO will overshoot.

Figure 4-3 shows the power-down sequence of BK7258.

Figure 4-3 BK7258 Power-down Sequence

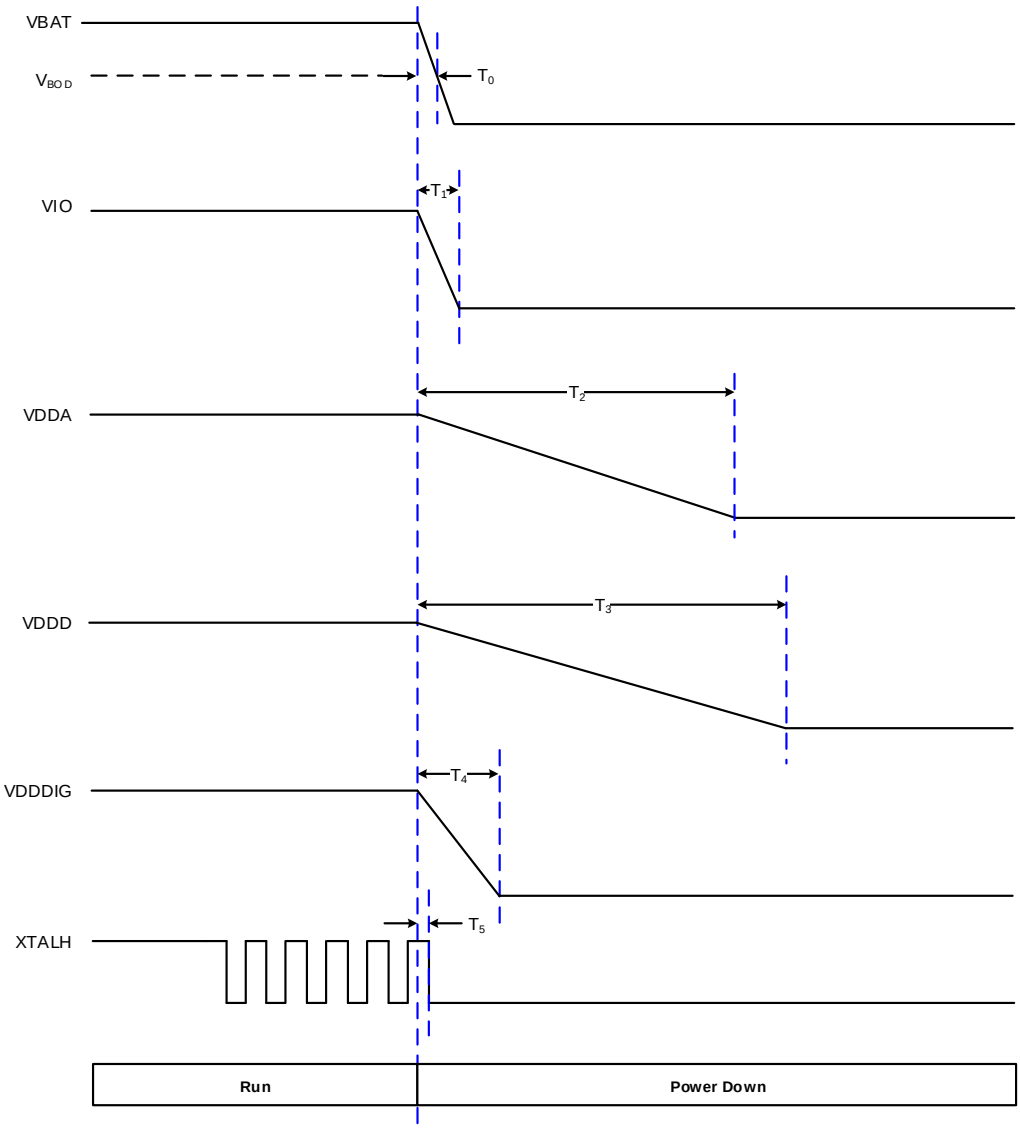


Table 4-2 Timing Parameters of Power-down Sequence

Parameter	Description	Min.	Typ.	Max.	Unit
V_{BOD}	VBAT BOD threshold	-	1.85	-	V
T_0	VBAT power-down time	-	400	-	μs
T_1	IO LDO power-down time	-	600	-	μs
T_2	Analog buck/LDO power-down time	-	400	-	ms

Parameter	Description	Min.	Typ.	Max.	Unit
T_3	Digital buck/LDO power-down time	-	500	-	ms
T_4	Digital core LDO power-down time	-	3.5	-	ms
T_5	XTALH power-down time	-	100	-	µs

4.5.2 Power Modes

The BK7258 supports three low-power modes except active mode, namely shutdown mode, deep sleep mode, and sleep mode, among which the shutdown mode has the lowest power consumption.

Shutdown Mode: All circuits are turned off. A high level on the CEN pin will bring the system to active mode.

Deep Sleep Mode: All circuits are powered down except the AON block. GPIO interrupts, RTC interrupts, or interrupts triggered by touch sensing I/O pins can power up the system again. The retention register holds its content.

Sleep Mode: The MCU and all digital blocks stop their clocks. GPIO interrupts, RTC interrupts, interrupts triggered by touch sensing I/O pins, or interrupts triggered by Wi-Fi/Bluetooth MAC low-power counters can bring the system back to active mode with normal voltage.

Active Mode: The MCU is active, and all peripherals are available.

4.6 General-purpose I/Os (GPIO)

The BK7258 has up to 56 GPIOs, which can be configured as either input or output. All GPIOs are shared with alternate functions. Table 3-3 Pin Multiplexing provides the mux functions of GPIOs.

The main features of GPIOs include:

- Push-pull
- Internal pull-up/down resistors
- Configurable drive strength
- Alternate function
- Interrupt generation:
  - High or low level
  - Rising or falling edge

4.7 SPI Interfaces (SPI)

The BK7258 integrates two SPI interfaces that can operate in master or slave mode. The SPI interfaces allow a clock frequency up to 40 MHz in both master and slave modes.

The SPI interfaces support the following features:

- 4-wire or 3-wire full-duplex synchronous communication
- Configurable 8-bit or 16-bit data width
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Embedded 64-depth RX FIFO and 64-depth TX FIFO with DMA capability

4.8 Quad SPI Interfaces (QSPI)

The BK7258 embeds two Quad SPI interfaces that provide support for communicating with external flash, PSRAM, or AMOLED display. The QSPI interfaces allow communicating up to 80 MHz.

The features of the QSPI interfaces are listed below:

- Single, dual, or quad SPI input/output
- Two functional modes: indirect mode and memory-mapped mode
- Fully programmable opcode and frame format
- Integrated RX FIFO and TX FIFO
- Supports 8, 16, and 32-bit data accesses

4.9 UART Interfaces (UART)

The BK7258 includes three Universal Asynchronous Receiver/Transmitter (UART) interfaces, which support full-duplex, asynchronous serial communication at a baud rate up to 6 Mbps.

The UART interfaces offer the features below:

- Configurable data length (5, 6, 7, or 8 bits)
- Even, odd, or none parity check
- Programmable stop bits (1 or 2 bits)
- Each UART embeds a 128-byte TX FIFO and a 128-byte RX FIFO. FIFO mode is disabled by default and can be enabled by software.
- Hardware flow control with RTS and CTS signals (UART0)

- Flash download (UART0)
- Programmable digital filter

4.10 Smart Card Controller (SC)

The Smart Card controller (SC) is a communication controller that transmits data between the superior system and the Smart Card. The controller can perform a complete smart card session, including card activation, card deactivation, cold/warm reset, Answer to Reset (ATR) response reception, data transfers, etc.

The features of the Smart Card controller (SC) are listed below:

- Supports the ISO/IEC 7816-3:2006 and EMV 4.3 specifications
- Performs functions needed for complete smart card sessions, including:
  - Card activation and deactivation
  - Cold/warm reset
  - Answer to Reset (ATR) response reception
  - Data transfers to and from the card
- Extensive interrupt support system
- Adjustable clock rate and bit (baud) rate
- Configurable automatic byte repetition
- Handles commonly used communication protocols:
  - T=0 for asynchronous half-duplex character transmission, and
  - T=1 for asynchronous half-duplex block transmission
- Automatic convention detection
- Adjustable FIFOs for Receive and Transmit buffers (64 bytes) with threshold
- Configurable timing functions:
  - Smart card activation time
  - Smart card reset time
  - Guard time
  - Timeout timers

4.11 SDIO Interface (SDIO)

A secure digital input/output (SDIO) host/slave interface is available on the BK7258. It can be used as a host to read external SD cards or used by an external host as a slave to communicate with chips. The SDIO interface allows a maximum clock speed of 80 MHz.

The SDIO features include the following:

- SD memory card specification version 2.0 compliant
- SDIO card specification version 2.0 compliant
- Two data bus modes: 1-bit mode (default) and 4-bit mode
- Data transfer up to 40 Mbyte/s for the host mode and 20 Mbyte/s for the slave mode
- Supports DMA capability, allowing high-speed transfer without CPU load

4.12 I2C Interfaces (I2C)

I2C is a popular inter-IC interface that requires only two bus lines, the serial data line (SDA) and the serial clock line (SCL). The BK7258 embeds two I2C interfaces, which can operate in master or slave mode.

The features of the I2C interfaces are listed below:

- Master and slave modes
- Standard mode (up to 100 kbps)
- Fast mode (up to 400 kbps)
- 7-bit and 10-bit addressing
- Bus idle and SCL low timeout condition detection
- Embedded 16-byte TX FIFO and 16-byte RX FIFO

4.13 USB Controller (USB)

The BK7258 embeds a USB high-speed (up to 480 Mbps) controller with an integrated transceiver. It can operate as a host or a device.

The USB controller features are the following:

- Compliant with the Universal Serial Bus Specification Rev 1.1 and 2.0
- Full-speed (FS) operation (up to 12 Mbps) and high-speed operation (up to 480 Mbps)
- One bidirectional control endpoint0
- Seven IN/OUT endpoints configurable to support bulk, interrupt or isochronous data transfer

- A FIFO of 8 Kbytes configurable to be allocated to 8 endpoints
- USB 2.0 Link Power Management (LPM) support

4.14 CAN Controller (CAN)

The BK7258 embeds a Controller Area Network (CAN) controller that uses the basic CAN principle and meets all constraints of the CAN-specification 2.0B active. Furthermore, the CAN controller can be configured to meet the specification of CAN with flexible data rate CAN FD. CAN 2.0 carries a data payload up to 8 bytes and CAN FD up to 64 bytes.

The CAN controller supports two operating modes, normal and standby, which can be selected via the CAN_STBY pin. If a high level is applied to the CAN_STBY pin, the external transceiver enters the standby mode.

4.15 LIN Controller (LIN)

The Local Interconnect Network (LIN) controller is a communication controller that performs serial communication. It implements the data link layer of the LIN Protocol Specification. The LIN protocol uses a single master/multiple slave concept for the frame transfer between nodes of the LIN network.

The LIN controller supports Sleep mode. If a low level is applied to the LIN_SLEEP pin, the external transceiver enters the Sleep mode.

The features of the LIN controller are listed here:

- Support of LIN specification 2.2A
- Backward compatibility to LIN 1.3
- Configurable for support of master or slave functionality
- Programmable data rate between 1 kbit/s and 20 kbit/s (for master)
- Automatic bit rate detection (for slave)
- 8-byte data buffer
- 8-bit host controller interface

4.16 GDMA Controllers (GDMA)

The BK7258 has two general-purpose DMA controllers (GDMA) with 8 DMA channels each to unload CPU activity. The 8 channels are shared by peripherals that have DMA capabilities.

The GDMA controllers can perform single block transfers and repeated block transfers. Data width for destination and source can be configured as 8 bits (byte), 16 bits (half-word), or 32 bits (word). The GDMA controllers allow peripheral to memory, memory to memory, and memory to peripheral data transfers at a high speed.

The GDMA controllers support channel isolation. The DMA channels can be configured as secure/non-secure and as privileged/unprivileged channels:

- A non-secure channel performs non-secure DMA transfers
- A secure channel can perform secure or non-secure DMA transfers, with
  - Secure or non-secure data read from the source address
  - Secure or non-secure data write to the destination address
  - Via a TrustZone-aware DMA AHB master port
- An unprivileged channel performs unprivileged DMA transfers
- A privileged channel performs privileged DMA transfers

A selection of peripherals on the BK7258 have DMA capabilities, including UART0, UART1, UART2, SPI0, SPI1, SDIO, AUDIO, I2S0, I2S1, I2S2, JPEG encoder, DISPLAY, AUX ADC, H.264, and DMIC.

4.17 DMA2D Controller (DMA2D)

The BK7258 has a specialized DMA controller (DMA2D) dedicated to image processing, offering direct memory transfer and 2D graphical acceleration without CPU intervention. It can perform the following operations:

- Filling a part or the whole of a destination image with a fixed color
- Copying a part or the whole of a source image into a part or the whole of a destination image
- Copying a part or the whole of a source image into a part or the whole of a destination image with a pixel format conversion
- Blending a part or two complete source images with a different pixel format and copying the result into a part or the whole of a destination image with a different color format

The DMA2D controller supports six operating modes:

- Register to memory
- Memory to memory
- Memory to memory with pixel format conversion
- Memory to memory with pixel format conversion and blending
- Memory to memory with pixel format conversion, blending and fixed color foreground layer
- Memory to memory with pixel format conversion, blending and fixed color background layer

Up to 12 input color modes are supported from 4-bit up to 32-bit per pixel with indexed or direct color coding. Six output color modes including RGB, ARGB, and YUV are supported. The DMA2D features dedicated memories for color lookup table (CLUT) storage.

An interrupt can be generated on the following events:

- Configuration error
- CLUT transfer completion
- CLUT access error
- Watermark on a user programmable destination line
- Transfer completion
- Transfer error

4.18 Rotation Module (ROTT)

The rotation module (ROTT) is capable of performing the following operations:

- Convert a YUV422 image stored in memory to a RGB565 image.
- Rotate a YUV422 or RGB565 image by 90° in either clockwise or counterclockwise direction.
- Store the converted or rotated image into the target memory.

4.19 Scaling Modules (SCALE)

The BK7258 has two scaling modules (SCALE) that can scale images of Y0UY1V, RGB565, or RGB888 format without changing the data format.

4.20 Display Controller (DISPLAY)

The TFT LCD display controller (DISPLAY) provides a 24-bit parallel digital RGB (Red, Green, Blue) and outputs all signals to interfaces of various LCD and TFT panels. It supports both RGB and Intel 8080 interfaces.

The display controller has the following features:

- Supports RGB and Intel 8080 interfaces
- RGB interface: up to 24-bit RGB parallel pixel output
- 8080 interface: up to 18-bit data output
- Three input color formats:
  - RGB888

  - RGB565
  - YUV422
- Three output color formats for RGB interface:
  - RBG888
  - RBG666
  - RBG565
- Three output color formats for 8080 interface:
  - 8- or 16-bit RGB888
  - 18-bit RGB666
  - 8-bit RGB565
- RGB interface and 8080 interface share a FIFO (1K x 32-bit)
- Programmable clocks for different display panels
- Up to five programmable interrupt events
- Configurable window position and size
- AHB master interface with burst of 64 words

4.21 Segment LCD Controller (SLCD)

The segment LCD controller (SLCD) is a digital driver for monochrome passive-matrix liquid crystal display (LCD). The controller drives up to 8 common terminals and 32 segment terminals to drive up to 224 (8x28) pixels. When using 4 common terminals, it supports 1/4 duty. The bias mode can be configured as 1/3 bias or 1/4 bias.

4.22 JPEG Encoder/Decoder

The BK7258 includes a JPEG encoder and a JPEG decoder for encoding and decoding JPEG streams. The JPEG encoder provides a small hardware compressor for JPEG images, while the decoder provides a decompression accelerator for JPEG images. Additionally, the JPEG encoder supports up to 32 programmable quantization tables.

4.23 CMOS Image Sensor Interface (CIS)

The CMOS Image Sensor (CIS) Digital Video Port (DVP) interface provides an 8-bit parallel interface to sensors, together with master clock (MCLK), pixel clock (PCLK), horizontal SYNC (HSYNC), and vertical SYNC (VSYNC) signals.

The input from the YUV sensor is directly fed to the hardware JPEG encoder, and the output of the JPEG encoder is directly written to the data memory by a dedicated DMA channel.

The CIS interface features include:

- 8-bit parallel interface
- Programmable polarity for pixel clock and synchronization signals
- Crop feature
- Data formats supported:
  - YCbCr 4:2:2 (YUYV, UYVY, YYUV, and UVYY)
  - RGB565

4.24 H.264 Encoder (H.264)

The H.264 video encoder allows fast and simple video compression. It performs the H.264 video compression algorithm on an incoming video stream. The encoded bitstream can be decoded by a Baseline, Mainprofile decoder. The input is raster 4:2:0 YUV video data. This data is compressed into H.264-compliant byte stream NAL units.

The H.264 supports the following features:

- Fully compatible with the ITU-T H.264 specification
- Level 1 to 4.1, encoded stream can be decoded by Baseline, Main profile decoder
- Supports up to 720p (1280x720 @ 30 fps)
- Constant Bit Rate and partial Variable Bit Rate mode support
- Motion vector up to –16.00/+15.75 pixels (search area is 32x32 pixels wide down to quarter pixel)
- Support for all intra16x16 and all but two of intra4x4 prediction modes
- Block skipping logic for lower bitrate
- Supports picture cropping for image sizes that are not a multiple of 16 pixels
- Supports Chroma Quantization Parameter offset for increased compression
- Requires no external memory by using Compressed framestore (CFS) for reference frame storage

4.25 Ethernet MAC Interface (ENET)

The BK7258 provides a media access controller (MAC) for Ethernet LAN communications through a reduced medium-independent interface (RMII). The Ethernet MAC interface (ENET) is compliant with the IEEE 802.3-2015 specification and can be used in applications such as network interface cards, and data center bridges and nodes. The BK7258 requires an external physical interface device (PHY) to connect to the physical LAN bus. The PHY is connected to the device RMII port using 9 signals, and can be clocked using the 25 MHz from BK7258 or 25/50 MHz from an external crystal oscillator.

The ENET includes the following features:

- 10 and 100 Mbps data transfer rates
- Half-duplex (CSMA/CD) and full-duplex operation
- 32-bit CRC generation and removal
- Tagged MAC frame support (VLAN support)
- Dedicated DMA controller allowing high-speed transfers between the system memory and the internal FIFOs
- Embedded TX FIFO and RX FIFO to buffer transmit and receive frames. Both FIFOs are 2 Kbytes.
- MAC control sublayer (control frames) support
- Different types of address filtering for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Supports hardware PTP (precision time protocol) in accordance with IEEE 1588-2008 (version 2)
- Triggers interrupt when system time becomes greater than target time

4.26 PWM Groups (PWMG)

The BK7258 has two advanced-control PWM groups (PWMG). Each PWMG consists of four independent 32-bit auto-reload counters driven by four programmable prescalers. The PWMGs can generate pulse width modulated signals for a variety of purposes, including input capture, pulse edge counting, or generation of output waveforms (output compare).

The features of one PWMG are listed here:

- Four 32-bit up, down, or up-and-down auto-reload counters:
  - PWM0 has a counter.
  - PWM1 has a counter (up-counting mode only).
  - PWM2 and PWM3 share a counter.
  - PWM4 and PWM5 share a counter.
- Four 8-bit programmable prescalers capable of dividing the clock frequency of each counter by any factor between 1 and 256
- Four independent channels, among which:
  - PWM0/2/4
  - Input capture
  - Pulse edge counting
  - PWM generation (edge or center-aligned mode)
  - PWM1

  - Independent simple waveform generation (up-counting mode)
  - Coupled waveform (reverse or identical) generation when coupled with PWM0
- Two channels PWM3/5 capable of generating coupled waveforms (reverse or identical) when coupled with PWM2/4
- Complementary outputs with programmable dead-time and configurable dead-time mode
- Synchronization circuit to control the counter with external signals and to interconnect several counters together
- Repetition counter to update the registers only after a given number of cycles of the counter
- Interrupt generation on the following events:
  - Update: counter overflow or underflow, counter initialization (by software or internal/external trigger)
  - Counter start
  - Input capture
  - Output compare
- Change of polarity, duty cycle, and base frequency on every PWM period
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes

Table 4-3 below provides the description of PWM signals.

Table 4-3 PWM Signals

GPIO	PWM Pin Name	Signal Type	Description
PWMG0			
GPIO6/GPIO18	PWMG0_PWM0	I/O	PWMG0 channel PWM0
GPIO7/GPIO19	PWMG0_PWM1	I/O	PWMG0 channel PWM1 PWM1 can work independently to generate simple waveforms or couple with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0.
GPIO8(1)/GPIO22(1)	PWMG0_PWM2	I/O	PWMG0 channel PWM2(2)
GPIO9/GPIO23(1)	PWMG0_PWM3	I/O	PWMG0 channel PWM3(2) PWM3 can couple with PWM2 (with deadtime insertion) to generate reverse or identical waveforms of PWM2.
GPIO24	PWMG0_PWM4	I/O	PWMG0 channel PWM4(3)
GPIO25	PWMG0_PWM5	I/O	PWMG0 channel PWM5(3) PWM5 can couple with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4.
PWMG1			
GPIO32	PWMG1_PWM0	I/O	PWMG1 channel PWM0

GPIO	PWM Pin Name	Signal Type	Description
GPIO33	PWMG1_PWM1	I/O	PWMG1 channel PWM1 PWM1 can work independently to generate simple waveforms or couple with PWM0 (with deadtime insertion) to generate reverse or identical waveforms of PWM0.
GPIO34	PWMG1_PWM2	I/O	PWMG1 channel PWM2(2)
GPIO35	PWMG1_PWM3	I/O	PWMG1 channel PWM3(2) PWM3 can couple with PWM2 (with deadtime insertion) to generate reverse or identical waveforms of PWM2.
GPIO36	PWMG1_PWM4	I/O	PWMG1 channel PWM4(3)
GPIO37	PWMG1_PWM5	I/O	PWMG1 channel PWM5(3) PWM5 can couple with PWM4 (with deadtime insertion) to generate reverse or identical waveforms of PWM4.

(1) It is not recommended to use GPIO8, GPIO22, and GPIO23 for LED and motor control.

(2) When PWM2 and PWM3 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

(3) When PWM4 and PWM5 are enabled simultaneously, they cannot generate waveforms with different duty cycles.

4.27 I2S Interfaces (I2S)

The BK7258 integrates three I2S interfaces that support master and slave modes with sampling rates from 8 kHz to 384 kHz.

The I2S interfaces support both PCM mono channel mode and I2S stereo channel mode.

Listed here are the I2S features:

- Master or slave mode
- Full duplex or half-duplex communication
- Various sampling rates
- 12-bit programmable prescaler
- Multiple I2S protocols supported:
  - I2S Philips standard
  - MSB-Justified standard (Left-Justified)
  - LSB-Justified standard (Right-Justified)
  - PCM standard
- Programmable data order with LSB first or MSB first
- Programmable data width between 1 and 32 bits
- Programmable clock polarity

- Integrated 32-bit RX FIFO and 32-bit TX FIFO, both with a depth of 32 x 3 channels
- Master clock can be output to drive external audio devices.

4.28 Audio Peripherals

The BK7258 comes with a rich set of audio peripherals to enhance the listening experience. The chip includes a four-band digital equalizer, two analog-to-digital converters (ADC), a digital-to-analog converter (DAC), two microphone input amplifiers and a bias generator, an audio amplifier, a DMIC interface, an SBC decoder accelerator, etc.

4.28.1 Four-band Digital Equalizer (EQ)

A dedicated four-band digital equalizer is implemented prior to digital-to-analog conversion, allowing the user to customize the frequency response of the audio output. The equalizer is implemented in hardware to reduce overall chip power consumption.

4.28.2 Audio ADCs and DAC

The BK7258 contains two 16-bit ADCs with sampling rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz. The chip also integrates a 16-bit DAC with sampling rates of 8 kHz, 16 kHz, 44.1 kHz, or 48 kHz.

4.28.3 Microphone Input Amplifiers and Bias Generator

The BK7258 contains two fully differential analog microphone input amplifiers and a low-noise microphone bias generator, allowing the microphone to interface with passive resistors and capacitors.

The microphone signal can be amplified with the amplifier over a 0 to 32 dB gain range with a 2 dB step size.

4.28.4 Audio Amplifier

The BK7258 provides a high-quality audio amplifier capable of driving a 16 Ω speaker with load capacitance up to 30 pF.

4.28.5 Digital Microphone Interface (DMIC)

The BK7258 has a digital microphone interface that supports two digital microphones. The PDM performs 8:1 CIC decimation, and the PCM sampling rate can be up to 384 kHz when the PDM clock frequency is 3.072 MHz.

4.29 Auxiliary ADC (AUX ADC)

The auxiliary ADC (AUX ADC) is a 12-bit successive approximation analog-to-digital converter. The AUX ADC has multiple external analog input channels and internal dedicated channels. The AUX ADC supports A/D conversion performed in one-shot, software control, or continuous mode.

The AUX ADC module has the following features:

- Programmable sampling rate from 12.5 to 812.5 kHz
- 12-bit resolution
- Up to 11 external analog input channels: ADC1/2/3/4/5/6/10/12/13/14/15
- Five internal dedicated channels:
  - VBAT monitoring channel (VBAT/2, VBAT/3, VBAT/5, or VBAT/7), connected to ADC0
  - Internal temperature sensor (TEMP), connected to ADC7
  - TSSIO, connected to ADC8
  - Touch OUT_TD, connected to ADC9
  - Internal debug channel, connected to ADC11
- Conversion modes:
  - One-shot mode
  - Software control mode
  - Continuous mode

4.30 Timer Groups (TIMG)

The BK7258 includes two general-purpose timer groups (TIMG). Each group has three 32-bit timers. Each group consists of three 32-bit counters driven by a 4-bit prescaler.

Each TIMG module has the following features:

- Three timers (Timer0/1/2)
- Three 32-bit up counters
- 4-bit prescaler, factor between 1 and 16
- Capable of reading the real-time value of the counter

4.31 Watchdog Timers (WDT)

The BK7258 has two watchdog timers, the digital power domain watchdog timer (DWDT) and the AON power domain watchdog timer (AWDT). The purpose of the watchdog timers is to detect and recover from failures or malfunctions. The watchdog timers trigger a reset on expiry of a specified time period.

The DWDT runs on the 32 kHz LPO_CLK clock (factor 2/4/8/16) and has a maximum programmable period of up to 32.768 (2^16/2 kHz) seconds. The AWDT runs on the ROSC and has a maximum programmable period of up to 65.536 (2^16/1 kHz) seconds.

4.32 Real-time Counter (RTC)

The real-time counter (RTC) module features a 64-bit counter and a tick event generator. The RTC runs on the 32 kHz LPO_CLK clock. It is used for low-power timing, and it can keep running even when the system is in deep sleep mode.

4.33 IrDA Interface (IRDA)

The BK7258 embeds a hardware IrDA interface that supports waveform analysis and waveform generation. It monitors the start of infrared signals, records the sequence of infrared waveforms, stores the waveforms in the RX FIFO for software analysis, and writes the waveforms to be sent to the TX FIFO when sending, thereby enabling the analysis and transmission of any infrared protocol.

The IrDA has the following features:

- Single-duplex mode
- Carrier modulation for transmission
- Integrated 512-byte RX FIFO and 512-byte TX FIFO

4.34 Temperature Sensor

The BK7258 integrates an on-chip temperature sensor that can measure on-chip temperature over -40 to +125 °C with an accuracy of ±5 °C. The digital results can be read from the ADC.

Usually, the software initiates the calibration of a specific module based on the temperature value, narrowing the difference in chip performance at different temperatures. The host can also read the on-chip temperature and decide whether to reduce transmit power or suspend operation at high temperatures.

4.35 Touch Sensor (TOUCH)

The BK7258 has up to 16 capacitive sensing I/Os, which immediately detect capacitance changes induced by touch or proximity of objects.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute-maximum-rated conditions for prolonged periods may affect the reliability of the device.

Parameter	Description	Min.	Max.	Unit
VBAT	Chip power supply voltage	-0.3	4.35	V
VIO	IO LDO output voltage	-0.3	4.0	V
VCCPA	Supply voltage for PA	-0.3	4.0	V
VCCPAD	Supply voltage for PA driver	-0.3	4.0	V
VCCIF	Supply voltage for IF	-0.3	1.8	V
VCCRXFE	Supply voltage for RX	-0.3	1.8	V
VCCPLL	Supply voltage for RF PLL	-0.3	1.8	V
VCCA	Supply voltage for analog	-0.3	1.8	V
VDDPA_BT	Bluetooth RF PA LDO output voltage	-0.3	1.2	V
VDDA	Analog buck/LDO output voltage	-0.3	1.8	V
VDDD	Digital buck/LDO output voltage	-0.3	1.2	V
VDDDIG	Digital core LDO output voltage	-0.3	1.1	V
VDDGPIO	Supply voltage for GPIOs	-0.3	4.0	V
VDDRAM	EXMEM LDO output voltage	-0.3	2.1	V
SWA	Analog buck switch output voltage	-0.3	4.35	V
SWD	Digital buck switch output voltage	-0.3	4.35	V
MICBIAS	Microphone bias output voltage	-0.3	4.0	V
P_{RX}	RX input power	-	10	dBm
T_{STR}	Storage temperature range	-55	150	℃

5.2 ESD Ratings

Parameter	Description	Test Condition	Value	Unit
ESD HBM	Electrostatic discharge voltage (human body model), per ANSI/ESDA/JEDEC JS-001	-	±3000	V
ESD CDM	Electrostatic discharge voltage (charge device model), per ANSI/ESDA/JEDEC JS-002	-	±500	V

5.3 Recommended Operating Conditions

Parameter	Description	Min.(1)	Typ.	Max.	Unit
VBAT(2)	Chip power supply voltage	2.5	3.3	4.35	V
VBAT slew rate	-	300	-	-	mV/ms
VIO	IO LDO output voltage	2.5	-	3.6	V
VCCPA(2)	Supply voltage for PA	2.5	-	3.6	V
VCCPAD(2)	Supply voltage for PA driver	2.5	-	3.6	V
VCCIF	Supply voltage for IF	-	1.45	-	V
VCCRXFE	Supply voltage for RX	-	1.45	-	V
VCCPLL	Supply voltage for RF PLL	-	1.45	-	V
VCCA	Supply voltage for analog	-	1.45	-	V
VDDPA_BT	Bluetooth RF PA LDO output voltage	0.9	-	1.1	V
VDDA	Analog LDO output voltage	-	1.45	-	V
	Analog buck output voltage	-	1.5	-	V
VDDD	Digital LDO output voltage	-	1.0	-	V
	Digital buck output voltage	-	1.05	-	V
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
VDDGPIO	Supply voltage for GPIOs	2.5	-	3.6	V
VDDRAM	EXMEM LDO output voltage	1.8	-	1.95	V
MICBIAS	Microphone bias output voltage	1.8	-	2.4	V
T_{OPR}	Operating temperature range	-40	-	85	℃

(1) The minimum voltage specified includes the ripple on the supply voltage and all other transient dips. Care must be taken when

Parameter	Description	Min.(1)	Typ.	Max.	Unit

operating at the minimum specified voltage.

(2) To ensure WLAN performance, the ripple on the supply must be less than Vpp = 100 mV.

5.4 Digital I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIH	High-level input voltage	-	0.7 VIO	-	VIO + 0.3	V
VIL	Low-level input voltage	-	-0.3	-	0.3 VIO	V
VOH	High-level output voltage	-	0.9 VIO	-	-	V
VOL	Low-level output voltage	-	-	-	0.1 VIO	V
I_{DRV}	I/O output drive strength	-	5	-	20	mA
R_{PU}	Weak pull-up resistor	-	-	40	-	kΩ
R_{PD}	Weak pull-down resistor	-	-	44	-	kΩ

5.5 IO LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VIO	IO LDO output voltage	2.5	3.3	3.6	V
Load current	-	-	-	500	mA

5.6 Analog LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog LDO output voltage	-	1.45	-	V
Load current	-	-	-	150	mA

5.7 Digital LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital LDO output voltage	-	1.0	-	V

Parameter	Description	Min.	Typ.	Max.	Unit
Load current	-	-	-	100	mA

5.8 Core LDO

Parameter	Description	Min.	Typ.	Max.	Unit
VDDDIG	Digital core LDO output voltage	-	0.875	-	V
Load current	-	-	-	100	mA

5.9 Analog Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDA	Analog buck output voltage	-	1.5	-	V
Load current	-	-	-	150	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ
Inductor saturation current	-	200	-	-	mA

5.10 Digital Buck

Parameter	Description	Min.	Typ.	Max.	Unit
VDDD	Digital buck output voltage	-	1.05	-	V
Load current	-	-	-	100	mA
Switching frequency	Buck modulation frequency	0.5	1	2	MHz
Output filter capacitor capacitance	-	-	4.7	-	μF
Inductor inductance	-	-	4.7	-	μH
Inductor DC resistance	-	-	-	500	mΩ

Parameter	Description	Min.	Typ.	Max.	Unit
Inductor saturation current	-	200	-	-	mA

5.11 26 MHz Crystal Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
F0	Nominal frequency	-	-	26	-	MHz
ΔF/F0	Frequency tolerance	25 ℃	-10	-	+10	ppm
TC	Frequency stability over operating temperature	-40 to 105 ℃ crystal	-20	-	+20	ppm
		-30 to 85 ℃ crystal	-10	-	+10	ppm
CL	Load capacitance	-	7	7.3	12	pF
TS	Trim sensitivity	-40 to 105 ℃ crystal	-	32	-	ppm/pF
		-30 to 85 ℃ crystal	-	17	-	ppm/pF

5.12 Current Consumption

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
QFN88 Current Consumption					
Active Mode					
RX current	11b: 11 Mbps DSSS	-	17.5	-	mA
	11g: 54 Mbps OFDM	-	17.5	-	mA
	11n: MCS7, HT20	-	17.5	-	mA
	11n: MCS7, HT40	-	18.5	-	mA
	11ax: MCS7, HE20	-	17.5	-	mA
TX current	11b: 11 Mbps DSSS @ 19 dBm	-	235	-	mA
	11g: 54 Mbps OFDM @ 17 dBm	-	200	-	mA
	11n: MCS7, HT20 @ 16 dBm	-	189	-	mA
	11n: MCS7, HT40 @15 dBm	-	182	-	mA
	11ax: MCS7, HE20 @ 16 dBm	-	188	-	mA

Parameter	Condition	Min.	Typ.	Max.	Unit
Sleep Mode					
Sleep	-	-	43	-	µA
Deep sleep	-	-	16	-	µA
Shutdown Mode					
Shutdown	-	-	2.5	-	µA

5.13 WLAN RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
Sensitivity					
Sensitivity - IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps DSSS	-	-98	-	dBm
	2 Mbps DSSS	-	-94.5	-	dBm
	5.5 Mbps DSSS	-	-92	-	dBm
	11 Mbps DSSS	-	-89	-	dBm
Sensitivity - IEEE 802.11g (10% PER for 1000 octet PSDU)	6 Mbps OFDM	-	-92	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-85	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77.5	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
Sensitivity - IEEE 802.11n, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HT20, MCS0	-	-92	-	dBm
	HT20, MCS1	-	-91	-	dBm
	HT20, MCS2	-	-88	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	HT20, MCS3	-	-86	-	dBm
	HT20, MCS4	-	-82	-	dBm
	HT20, MCS5	-	-78	-	dBm
	HT20, MCS6	-	-76.5	-	dBm
	HT20, MCS7	-	-75	-	dBm
Sensitivity - IEEE 802.11n, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HT40, MCS0	-	-87.5	-	dBm
	HT40, MCS1	-	-87	-	dBm
	HT40, MCS2	-	-85	-	dBm
	HT40, MCS3	-	-82.5	-	dBm
	HT40, MCS4	-	-79	-	dBm
	HT40, MCS5	-	-75	-	dBm
	HT40, MCS6	-	-74	-	dBm
	HT40, MCS7	-	-71.5	-	dBm
Sensitivity - IEEE 802.11ax, 20 MHz (10% PER for 4096 octet PSDU, LDPC)	HE20, MCS0	-	-92	-	dBm
	HE20, MCS1	-	-90.5	-	dBm
	HE20, MCS2	-	-87.5	-	dBm
	HE20, MCS3	-	-85	-	dBm
	HE20, MCS4	-	-81	-	dBm
	HE20, MCS5	-	-77.5	-	dBm
	HE20, MCS6	-	-75.5	-	dBm
	HE20, MCS7	-	-74	-	dBm
Sensitivity - IEEE 802.11ax, 40 MHz (10% PER for 4096 octet PSDU, LDPC)	HE40, MCS0	-	-88.5	-	dBm
	HE40, MCS1	-	-87.5	-	dBm
	HE40, MCS2	-	-85.5	-	dBm
	HE40, MCS3	-	-82	-	dBm
	HE40, MCS4	-	-77	-	dBm
	HE40, MCS5	-	-75	-	dBm
	HE40, MCS6	-	-74	-	dBm

Parameter	Condition		Min.	Typ.	Max.	Unit
	HE40, MCS7		-	-72	-	dBm
Maximum Receive Level						
Maximum receive level @ 2.4 GHz	11b: 1, 2 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11b: 5.5, 11 Mbps (8% PER, 1024 octets)		-	10	-	dBm
	11g: 6–54 Mbps (10% PER, 1000 octets)		-	0	-	dBm
	11n: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
	11ax: MCS0–7 (10% PER, 4096 octets)		-	0	-	dBm
Adjacent Channel Rejection						
Adjacent channel (±30 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	1 Mbps DSSS	-74 dBm	-	50	-	dB
	2 Mbps DSSS	-74 dBm	-	45	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11b (8% PER for 1024 octet PSDU with desired signal level as specified in Condition)	5.5 Mbps DSSS	-70 dBm	-	43	-	dB
	11 Mbps DSSS	-70 dBm	-	40	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11g (10% PER for 1000 octet PSDU with desired signal level as specified in Condition)	6 Mbps OFDM	-79 dBm	-	43	-	dB
	54 Mbps OFDM	-62 dBm	-	27	-	dB
Adjacent channel (±25 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT20, MCS0	-79 dBm	-	43	-	dB
	HT20, MCS7	-61 dBm	-	21	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11n (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HT40, MCS0	-76 dBm	-	TBD	-	dB
	HT40, MCS7	-58 dBm	-	TBD	-	dB

Parameter	Condition		Min.	Typ.	Max.	Unit
Adjacent channel (±20 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE20, MCS0	-79 dBm	-	43	-	dB
	HE20, MCS7	-61 dBm	-	26	-	dB
Adjacent channel (±40 MHz) rejection - IEEE 802.11ax (10% PER for 4096 octet PSDU with desired signal level as specified in Condition)	HE40, MCS0	-76 dBm	-	TBD	-	dB
	HE40, MCS7	-58 dBm	-	TBD	-	dB
Spurious Emissions						
Spurious emissions	< 1 GHz		-	-60	-	dBm
	> 1 GHz		-	-50	-	dBm

5.14 WLAN RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2412	-	2484	MHz
TX power					
TX power - IEEE 802.11b (SEM compliant)	1 Mbps DSSS	-	20	-	dBm
	11 Mbps DSSS	-	20	-	dBm
TX power - IEEE 802.11g (EVM compliant)	6 Mbps OFDM	-	18	-	dBm
	54 Mbps OFDM	-	18	-	dBm
TX power - IEEE 802.11n (EVM compliant)	HT20, MCS0	-	17	-	dBm
	HT20, MCS7	-	17	-	dBm
	HT40, MCS0	-	16	-	dBm
	HT40, MCS7	-	16	-	dBm
TX power - IEEE 802.11ax (EVM compliant)	HE20, MCS0	-	17	-	dBm
	HE20, MCS7	-	17	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
	HE40, MCS0	-	16	-	dBm
	HE40, MCS7	-	16	-	dBm
Spurious Emissions					
Spurious emissions (at maximum output power)	< 1 GHz	-	-50	-	dBm
	> 1 GHz	-	-45	-	dBm

5.15 Bluetooth LE RF Receiver Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter	Condition	Min.	Typ.	Max.	Unit
General					
Frequency range	-	2402	-	2480	MHz
Bluetooth LE 1 Mbps					
Sensitivity	30.8% PER	-	-97	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	8	-	dB
C/I 1 MHz adjacent channel	-	-	0	-	dB
C/I -1 MHz adjacent channel	-	-	0	-	dB
C/I 2 MHz adjacent channel	-	-	-26	-	dB
C/I -2 MHz adjacent channel	-	-	-27	-	dB
C/I 3 MHz adjacent channel	-	-	-28	-	dB
C/I -3 MHz adjacent channel	-	-	-29	-	dB
C/I > 3 MHz adjacent channel	-	-	-50	-	dB
C/I < -3 MHz adjacent channel	-	-	-50	-	dB
Out-of-band blocking	30–2000 MHz	-10	-	-	dBm
	2003–2399 MHz	-12	-	-	dBm
	2484–2997 MHz	-12	-	-	dBm
	3000 MHz–12.75 GHz	-2	-	-	dBm

Parameter	Condition	Min.	Typ.	Max.	Unit
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 2 Mbps					
Sensitivity	30.8% PER	-	-94	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	7	-	dB
C/I 2 MHz adjacent channel	-	-	0	-	dB
C/I -2 MHz adjacent channel	-	-	3	-	dB
C/I 4 MHz adjacent channel	-	-	-26	-	dB
C/I -4 MHz adjacent channel	-	-	-30	-	dB
C/I 6 MHz adjacent channel	-	-	-30	-	dB
C/I -6 MHz adjacent channel	-	-	-39	-	dB
C/I > 6 MHz adjacent channel	-	-	-22	-	dB
C/I < -6 MHz adjacent channel	-	-	-22	-	dB
Out-of-band blocking	30–2000 MHz	-	-30	-	dBm
	2003–2399 MHz	-	-35	-	dBm
	2484–2997 MHz	-	-35	-	dBm
	3000 MHz–12.75 GHz	-	-17	-	dBm
Intermodulation	-	-	TBD	-	dBm
Bluetooth LE 125 kbps					
Sensitivity	30.8% PER	-	-102	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	3	-	dB
C/I 1 MHz adjacent channel	-	-	-15	-	dB
C/I -1 MHz adjacent channel	-	-	-16	-	dB
C/I 2 MHz adjacent channel	-	-	-34	-	dB
C/I -2 MHz adjacent channel	-	-	-40	-	dB
C/I 3 MHz adjacent channel	-	-	-42	-	dB
C/I -3 MHz adjacent channel	-	-	-43	-	dB

Parameter	Condition	Min.	Typ.	Max.	Unit
C/I > 3 MHz adjacent channel	-	-	-41	-	dB
C/I < -3 MHz adjacent channel	-	-	-42	-	dB
Bluetooth LE 500 kbps					
Sensitivity	30.8% PER	-	-99	-	dBm
Maximum input level	30.8% PER	-	0	-	dBm
C/I co-channel	-	-	5	-	dB
C/I 1 MHz adjacent channel	-	-	-2	-	dB
C/I -1 MHz adjacent channel	-	-	-3	-	dB
C/I 2 MHz adjacent channel	-	-	-30	-	dB
C/I -2 MHz adjacent channel	-	-	-31	-	dB
C/I 3 MHz adjacent channel	-	-	-31	-	dB
C/I -3 MHz adjacent channel	-	-	-40	-	dB
C/I > 3 MHz adjacent channel	-	-	-36	-	dB
C/I < -3 MHz adjacent channel	-	-	-36	-	dB

5.16 Bluetooth LE RF Transmitter Characteristics

Measured with T = 25 °C, VBAT = 3.3 V unless otherwise stated.

Parameter		Condition	Min.	Typ.	Max.	Unit
General						
Frequency range		-	2402	-	2480	MHz
TX power		-	-20	6	15	dBm
Bluetooth LE 1 Mbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	> ±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf2max	-	185	235	-	kHz

Parameter		Condition	Min.	Typ.	Max.	Unit
	Δf2avg/Δf1avg	-	0.8	0.93	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	2	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 2 Mbps						
In-band emissions	±4 MHz offset	-	-	-50	-	dBm
	±5 MHz offset	-	-	-51	-	dBm
	> ±5 MHz offset	-	-	-52	-	dBm
Modulation characteristics	Δf1avg	-	-	488	-	kHz
	Δf2max	-	-	469	-	kHz
	Δf2avg/Δf1avg	-	-	0.93	-	-
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	3	150	kHz
	Max $\|f_0 - f_n\|$ n = 2, 3, 4…k	-	-	2.5	50	kHz
	$\|f_1 - f_0\|$	-	-	1.5	23	kHz
	Max $\|f_n - f_{n-5}\|$ n = 6, 7, 8…k	-	-	2.5	20	kHz/50 μs
Bluetooth LE 125 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	> ±3 MHz offset	-	-	-50	-	dBm
Modulation characteristics	Δf1avg	-	225	245	275	kHz
	Δf1max	-	185	246	-	kHz
Carrier frequency offset and drift	Max $\|f_n\|$ n = 0, 1, 2, 3…k	-	-	1.5	150	kHz
	Max $\|f_0 - f_n\|$ n = 1, 2, 3…k	-	-	1.5	50	kHz
	$\|f_0 - f_3\|$	-	-	1.5	19.2	kHz
	$\|f_n - f_{n-3}\|$ n = 7, 8, 9…k	-	-	1.5	19.2	kHz/48 μs

Parameter		Condition	Min.	Typ.	Max.	Unit
Bluetooth LE 500 kbps						
In-band emissions	±2 MHz offset	-	-	-47	-	dBm
	±3 MHz offset	-	-	-49	-	dBm
	>±3 MHz offset	-	-	-50	-	dBm

5.17 Audio Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
DAC differential output	With 600 Ohm load	-	1	-	Vrms
	With 16 Ohm load	-	0.8	-	Vrms
DAC differential output THD	With 0.7 Vrms @ 600 Ohm load	-	-	-80	dB
	With 0.65 Vrms @ 16 Ohm load	-	-	-80	dB
DAC output SNR	1 kHz sine wave	-	104	-	dB
DAC sampling rate	-	8	-	48	kHz
ADC SNR	1 kHz sine wave	-	100	-	dB
ADC sampling rate	-	8	-	48	kHz

5.18 AUX ADC Characteristics

Parameter	Condition	Min.	Typ.	Max.	Unit
Conversion clock	-	0.2	-	13	MHz
Conversion time	-	-	16	-	Cycle
V_{REF}	Internal	-	1.1	-	V
	External	-	VIO/3	-	V
Input voltage range	-	0	-	V_{REF}*N(1)	V
Input impedance	-	10	-	-	MΩ
Input capacitance (Cs)	-	-	1	-	pF
DNL	-	-1	-	3	LSB
INL	-	-5	-	5	LSB

Parameter	Condition	Min.	Typ.	Max.	Unit
ENOB	-	-	10	-	Bit
SNDR	-	-	62	-	dB
SFDR	-	-	77	-	dB
$T_{STARTUP}$	-	-	5	-	μs
Current consumption	-	-	200	-	μA

(1) N is the input voltage division factor. N=1, 2, 3, or 4.

6. Package Information

6.1 QFN88 9 x 9 mm Package

Figure 6-1 QFN88 9 x 9 mm Package Outline

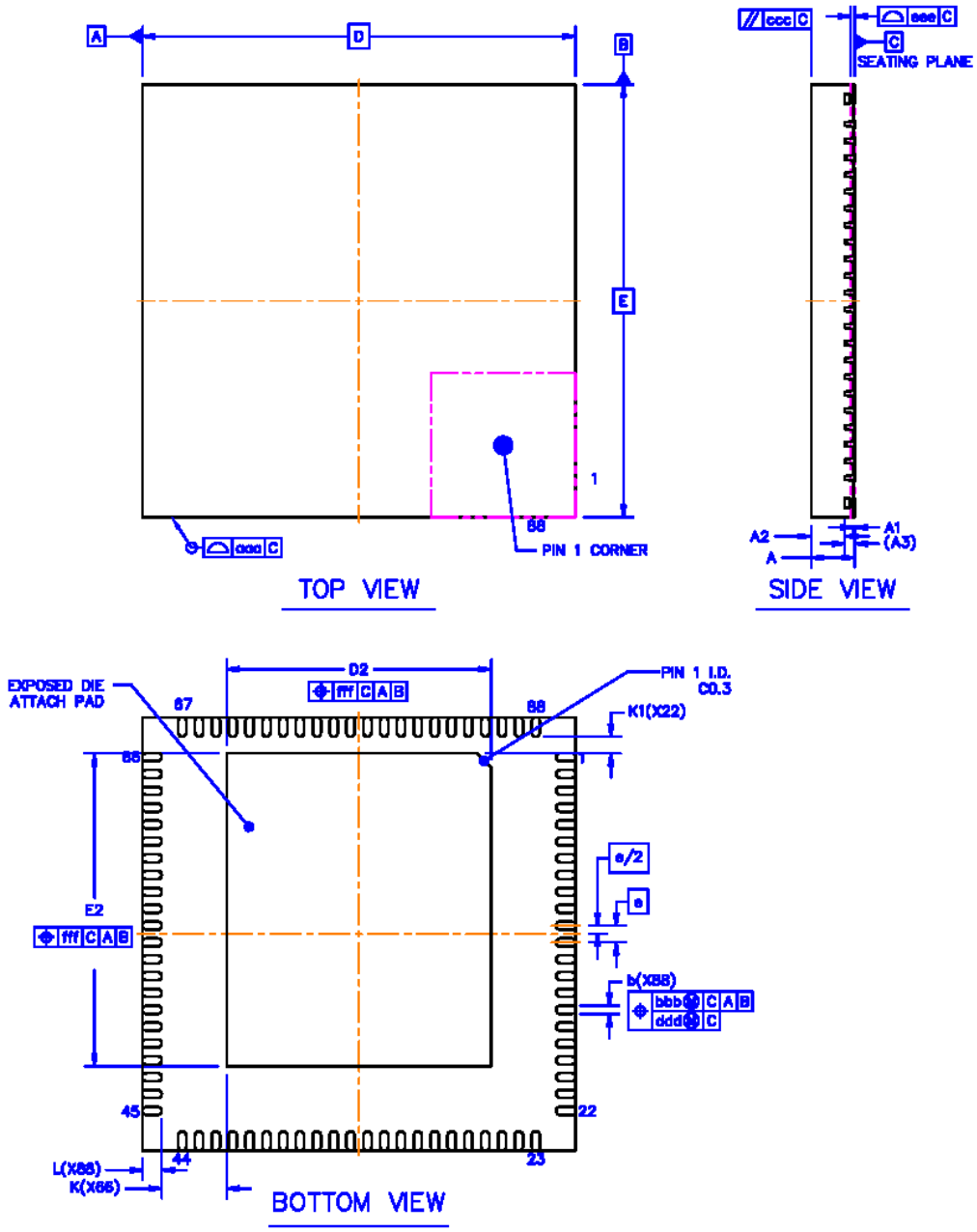


Table 6-1 QFN88 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
A2	-	0.70	-
A3	0.203 REF		
b	0.12	0.17	0.22
D	9.00 BSC		
E	9.00 BSC		
e	0.35 BSC		
D2	5.40	5.50	5.60
E2	6.40	6.50	6.60
L	0.30	0.40	0.50
K	1.35 REF		
K1	0.35 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

6.2 QFN68 8 x 8 mm Package

Figure 6-2 QFN68 8 x 8 mm Package Outline

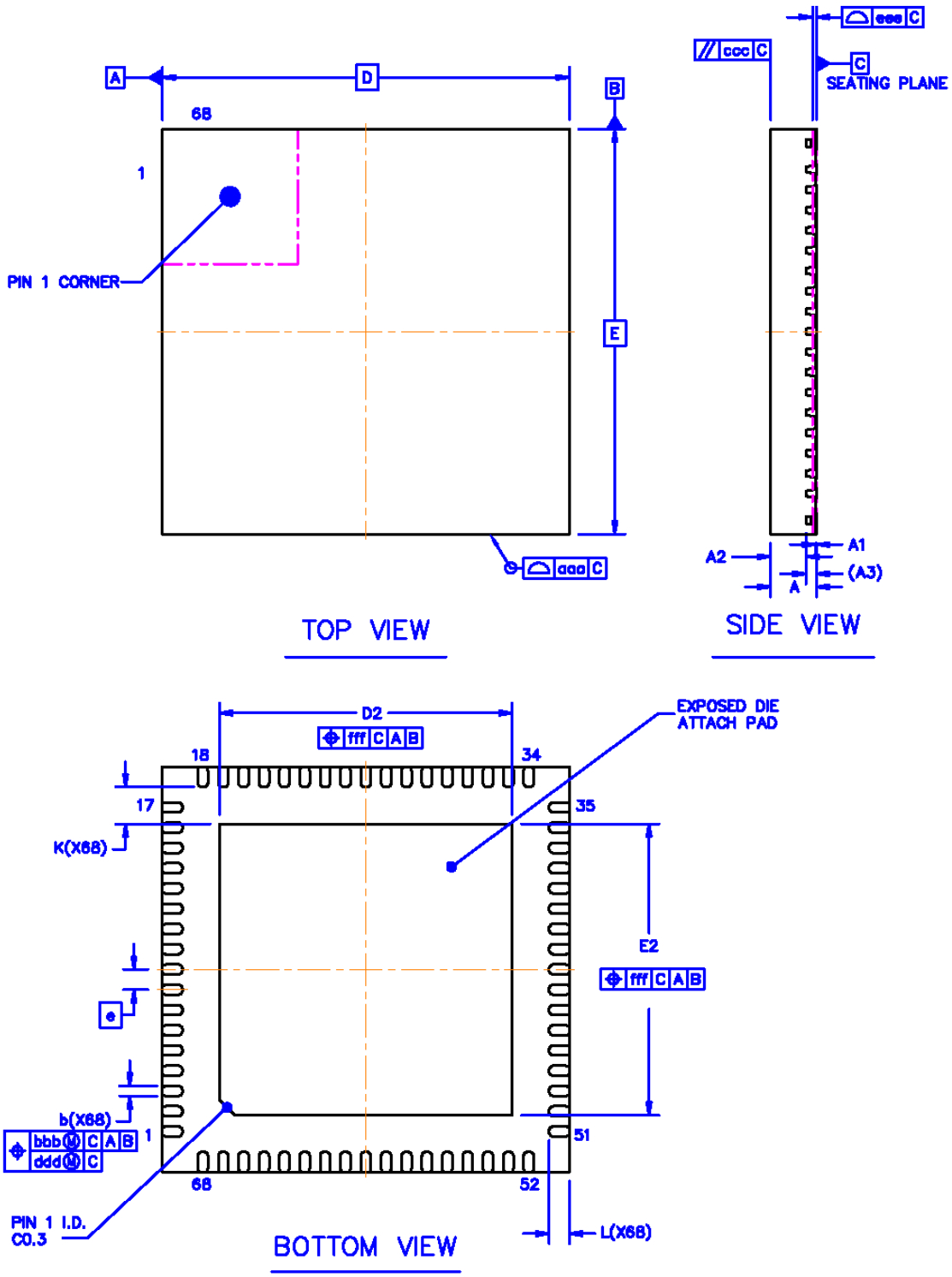
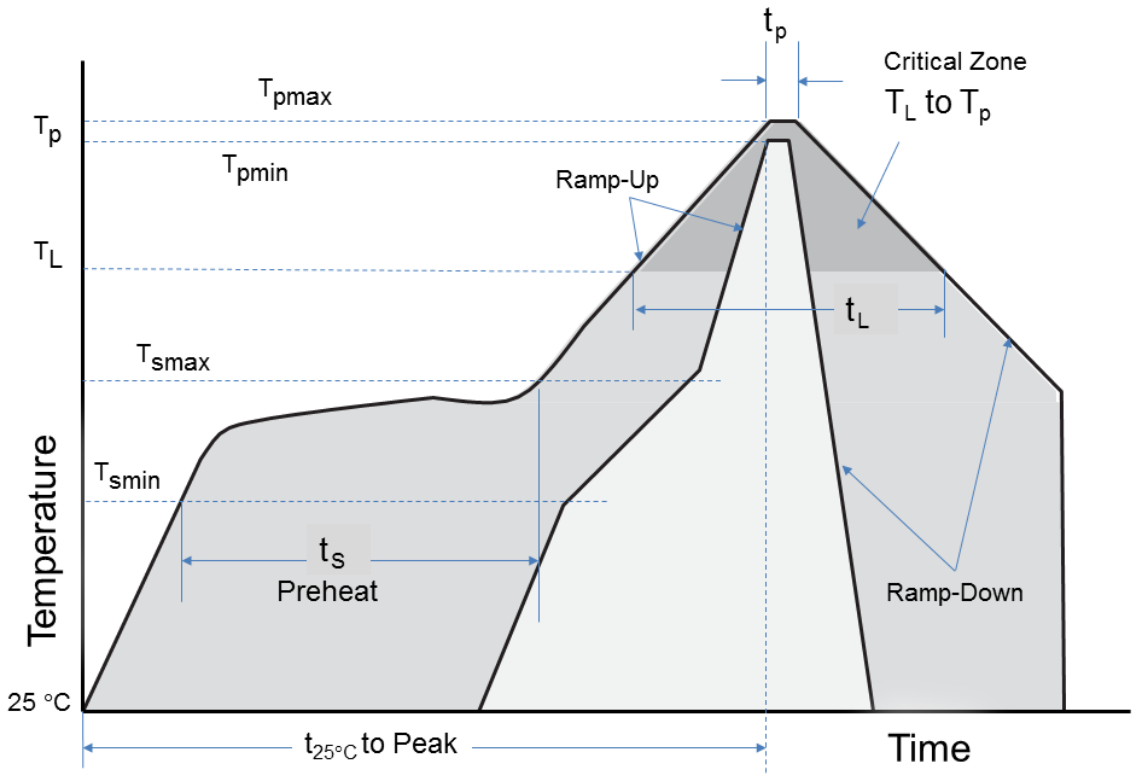


Table 6-2 QFN68 Package Dimensions

Symbol	Dimensions in Millimeters		
	Min.	Nom.	Max.
A	0.85	0.90	0.95
A1	0.00	0.02	0.05
A2	-	0.70	-
A3	0.203 REF		
b	0.15	0.20	0.25
D	8.00 BSC		
E	8.00 BSC		
e	0.40 BSC		
D2	5.65	5.75	5.85
E2	5.65	5.75	5.85
L	0.30	0.40	0.50
K	0.725 REF		
aaa	0.10		
ccc	0.10		
eee	0.08		
bbb	0.07		
ddd	0.05		
fff	0.10		

7. Reflow Soldering Profile

Figure 7-1 Reflow Soldering Profile



Profile Feature		Specification
Average ramp-up rate (T_{smax} to T_p)		3 ℃/s max.
Preheat	Temperature min. (T_{smin})	150 ℃
	Temperature max. (T_{smax})	200 ℃
	Time (t_s)	60 s to 180 s
Time maintained above	Temperature (T_L)	217 ℃
	Time (t_L)	60 s to 150 s
Peak/classification temperature (T_p)		260 ℃
Time within 5 ℃ of actual peak temperature (t_p)		20 s to 40 s

Profile Feature	Specification
Ramp-down rate	6 ℃/s max.
Time 25 ℃ to peak temperature	8 minutes max.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, PBB, PBDE, DEHP, BBP, DBP, or DIBP content in accordance with EU RoHS Directive (EU) 2015/863 amending Annex II to Directive 2011/65/EU.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Moisture Sensitivity Level

The product is qualified to moisture sensitivity level MSL3 in accordance with IPC/JEDEC J-STD-020.

8. Ordering Information

Figure 8-1 Ordering Code Scheme

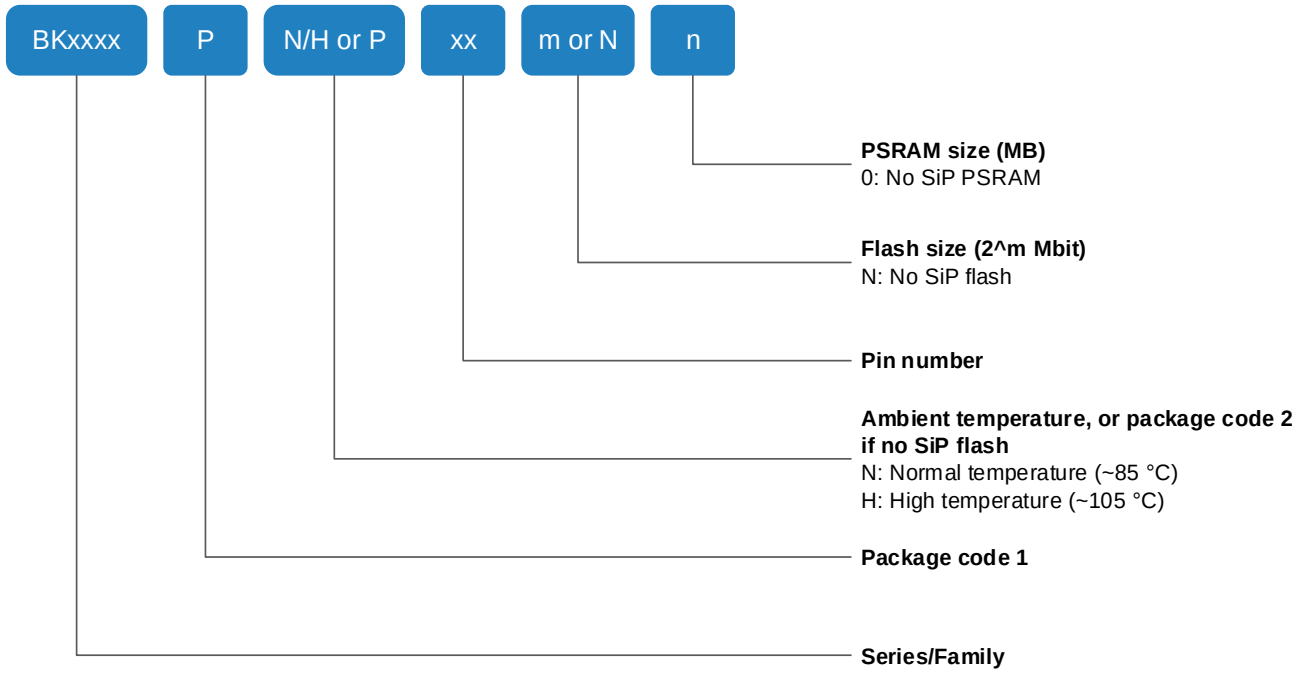


Table 8-1 Ordering Information

Ordering Code	Package	SiP Flash(1)	SiP PSRAM(1)	Packing	Minimum Ordering Qty (MOQ)
BK7258QN8868	9 mm x 9 mm QFN88	8 MB	8 MB	Tape and Reel	3000
BK7258QN88616	9 mm x 9 mm QFN88	8 MB	16 MB	Tape and Reel	3000
BK7258QN6854	8 mm x 8 mm QFN68	4 MB	4 MB	Tape and Reel	3000

(1) A system in a package (SiP) refers to flash/PSRAM enclosed in the package.

Revision History

Version	Date	Description
1.0	2023/1/17	Initial release
1.1	2023/5/6	• Removed 802.11ac support • Updated compliance with Bluetooth Specification to Bluetooth 5.4 throughout the document • Removed cache from subsection Memory of Section 1 Features • Changed USB OTG to USB throughout the document • Corrected the number of external input channels for the SAR ADC throughout the document • Updated pin assignments for QFN80 package in Section 3 Pin Descriptions • Added parameter MICBIAS to Section 5.3 Recommended Operating Conditions • Corrected V_{REF} values for AUX ADC in Section 5.18 AUX ADC Characteristics
1.2	2023/6/9	• Renamed some interfaces and peripherals • Replaced QFN80 package with QFN88 package • Updated Section 1 Features • Updated Section 2 Overview • Updated Section 3 Pin Descriptions • Updated Section 4 Functional Description • Updated and added measurement data in Section 5 Electrical Characteristics • Added Section 5.2 ESD Ratings, Section 5.4 Digital I/O Characteristics, and Section 5.17 Audio Characteristics • Updated Section 8 Ordering Information
1.3	2023/6/16	• Updated Bluetooth support • Updated core description
1.4	2023/8/30	• General wording fixes • Updated OFDMA and TWT support, added Bluetooth LE features, and updated MCU frequency in Section 1 Features • Added Flash support and updated PSRAM size • Renamed low-voltage sleep mode to sleep mode and removed normal sleep mode • Changed pin assignments for QFN88 package and updated information

Version	Date	Description
		for QFN88 package • Corrected pin assignments for UART0 CTS and RTS in Section 3 Pin Descriptions • Updated Section 4.3 Clock Management • Updated the description of Section 4.20 Display Controller (DISPLAY) • Added FIFO feature for IrDA interface in Section 4.33 IrDA Interface (IRDA) • Corrected absolute maximum ratings for VDDD and VDDDIG in Section 5.1 Absolute Maximum Ratings • Added package outline and dimensions for QFN88 package in Section 6 Package Information • Updated ordering information in Section 8 Ordering Information
1.5	2023/9/4	• Update pin assignments for QFN88 package in Section 3 Pin Descriptions • Corrected dimensions for D and E symbols of QFN88 package in Section 6 Package Information
1.6	2023/9/25	Changed pin # 73 to VDDPA_BT for QFN88 package
1.7	2024/4/22	• Updated Wi-Fi operating mode support, Wi-Fi TX power, and Wi-Fi RX sensitivity, maximum VBAT voltage, and updated and added current values in Section 1 Features • Corrected GDMA channel number and maximum number of pixels the segment LCD can drive throughout the document • Updated maximum operating temperature throughout the document • Updated the description of VDDGPIO throughout the document • Updated the description of Section 4.4 Reset • Updated the note on selecting bypass capacitors, updated Figure 4-1, Figure 4-2, and Table 4-1, and added Figure 4-3 and Table 4-2 in Section 4.5.1 Power Scheme • Updated UART baud rate in Section 4.9 UART Interfaces (UART) • Updated SDIO clock frequency in Section 4.11 SDIO Interface (SDIO) • Updated the description of Section 4.26 PWM Groups (PWMG) • Updated the introduction to IrDA interface in Section 4.33 IrDA Interface (IRDA) • Removed note “Values currently listed in this section are objective data and are subject to change.” from Section 5 Electrical Characteristics • Updated maximum voltages for power supplies in Section 5.1 Absolute Maximum Ratings • Added HBM and CDM values in Section 5.2 ESD Ratings • Added VBAT slew rate and notes in Section 5.3 Recommended Operating Conditions

Version	Date	Description
		• Updated voltage ranges for VBAT, VDDA, VDDD, VDDGPIO, and VDDRAM in Section 5.3 Recommended Operating Conditions • Added Section 5.5 IO LDO • Updated VDDA (LDO output) minimum and maximum voltages in Section 5.6 Analog LDO • Updated VDDA (buck output) minimum voltage and minimum inductor saturation current in Section 5.9 Analog Buck • Updated maximum load capacitance of the 26 MHz crystal in Section 5.11 26 MHz Crystal Characteristics • Updated and added current values in Section 5.12 Current Consumption • Updated and added RF characteristic values in Section 5.13 WLAN RF Receiver Characteristics to Section 5.16 Bluetooth LE RF Transmitter Characteristics • Updated RoHS compliance statement in Section 7 Reflow Soldering Profile
1.8	2024/7/15	• General wording fixes • Updated core name • Updated the description of flash/PSRAM size in Section 1 Features • Updated the minimum operating voltage of VBAT, VIO, VCCPA, VCCPAD, and VDDGPIO to 2.5 V • Updated the description of wake-up from deep sleep mode in Section 4.4 Reset • Updated the description of VIO in Section 4.5.1 Power Scheme • Added I2C FIFO feature in Section 4.12 I2C Interfaces (I2C) • Corrected maximum sampling rate and VBAT monitoring channel input voltage for AUX ADC in Section 4.29 Auxiliary ADC (AUX ADC) • Added minimum conversion clock frequency, and updated V_{REF} and input voltage range for AUX ADC in Section 5.18 AUX ADC Characteristics
1.9	2024/11/21	• Added flash XIP support and flash/PSRAM expansion in Section 1 Features • Added QFN68 package • Renamed pin # 24, 25, 72 of QFN88 package • Corrected the description of the ENET_REF_CLK pin in Section 3.1 QFN88 Pin Descriptions • Updated the description of Section 4.1 Wi-Fi/Bluetooth Transceiver • Updated the description of Section 4.4 Reset • Updated Figure 4-1 and power-up sequence timing parameter T_4 values in Section 4.5.1 Power Scheme • Updated the description of sleep mode in Section 4.5.2 Power Modes

Version	Date	Description
		• Updated the voltages of VCCIF, VCCRXFE, VCCPLL, VCCA, VDDA, VDDD, and VDDDIG in Section 5.3 Recommended Operating Conditions • Updated VIO typical voltage in Section 5.5 IO LDO • Updated VDDA (LDO output) voltage in Section 5.6 Analog LDO • Updated VDDD (LDO output) voltage in Section 5.7 Digital LDO • Updated VDDDIG voltage in Section 5.8 Core LDO • Updated VDDA (buck output) typical voltage in Section 5.9 Analog Buck • Updated VDDD (buck output) voltage in Section 5.10 Digital Buck

Copyright

Disclaimer

The documentation is provided on an "as-is" basis only. Beken reserves the right to make any updates, corrections and any other modifications to its documentation without further notice and limitation to product information, descriptions, and specifications herein. Beken does not give warranties as to the accuracy or completeness of the included information. Beken shall have no liability for any use of the information in this documentation. You should obtain the latest relevant information before placing orders and should verify that such information is current and complete. Information published by Beken regarding any third-party products does not constitute a license to use such products or a warranty or endorsement thereof. Use of such information may require a license from a third party under the intellectual property rights of such third party, or a license from Beken under the intellectual property rights of Beken.

Trademarks

Beken, the BEKEN logo, and combinations thereof are trademarks or registered trademarks of Beken. All other product or brand names mentioned herein are trademarks or registered trademarks of their respective holders.

Beken Corporation

Building 41, 1387 Zhangdong Rd

Shanghai 201203

China

http://www.bekencorp.com