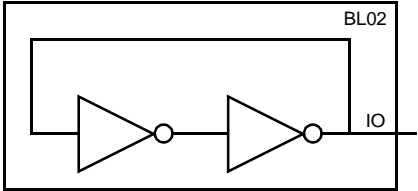


AMI5HG 0.5 micron CMOS Gate Array

Description

BL02 is a tristate bus latch that stores the final binary level on the bus when left undriven.

Core Logic

Logic Symbol	Truth Table	Pin Loading				
	N/A	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>Equivalent Load</th> </tr> </thead> <tbody> <tr> <td>IO</td> <td>1.6</td> </tr> </tbody> </table>		Equivalent Load	IO	1.6
	Equivalent Load					
IO	1.6					

Equivalent Gates 5.0

HDL Syntax

Verilog BL02 *inst_name* (IO);

VHDL *inst_name*: BL02 port map (IO);

Size And Power Characteristics

Parameter	Value	Units
Static I_{DD} ($T_J = 85^\circ\text{C}$)	TBD	nA
EQL_{pd}	16.1	Eq-load

See page 2-15 for power equation.