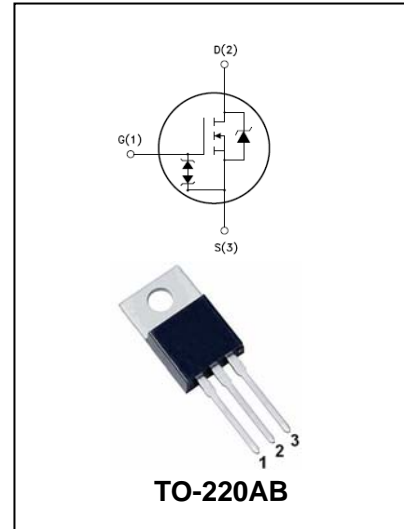


## N-Channel Enhancement Mode Field Effect Transistor

### BL10N65

#### FEATURES

- Extremely High dv/dt Capability.
- 100% Avalanche Tested.
- Gate Charge Minimized.
- Very Good Manufacturing Reliability.



#### APPLICATIONS

- N-channel Enhancement mode Effect Transistor.
- Switching Applications.

#### MAXIMUM RATING operating temperature range applies unless otherwise specified

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-Source Voltage	600	V
$V_{GS}$	Gate -Source Voltage	$\pm 30$	V
$I_D$	Maximum Drain Current(continuous) at $T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$	10 5.7	A
$I_{DM}$	Drain Current(pulsed)Note1	36	A
$P_D$	Power Dissipation at $T_C=25^\circ\text{C}$	115	W
$V_{esd}(G-S)$	G-S ESD (HBM $C=100\text{pF}$ , $R=1.5\text{k}\Omega$ )	4000	V
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j=25^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{V}$ )	300	mJ
dv/dt	Peak Diode Recovery Voltage Slope(Note2)	4.5	V/ns
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	$^\circ\text{C}/\text{W}$
$T_j$ $T_{stg}$	Operating Junction and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

Note:1.Pulse width limited by safe operating area

2.  $I_{SO} \leq 12\text{A}$ ,  $di/dt \leq 400\text{A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$

## N-Channel Enhancement Mode Field Effect Transistor

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#### ELECTRICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

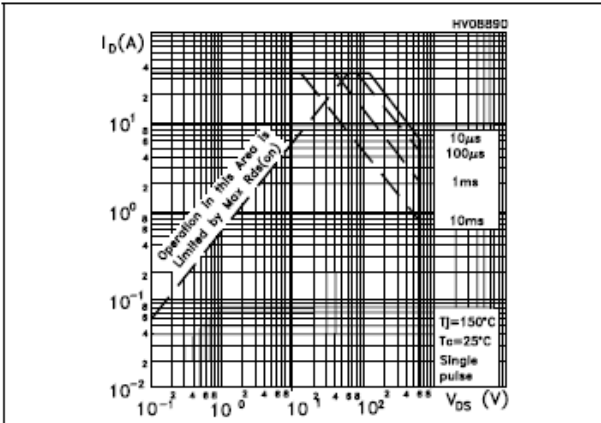
Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=650V, V_{GS}=0V$ $V_{DS}=650V, V_{GS}=0V, T_C=125^\circ C$	-	-	1 50	$\mu A$
Gate-body Leakage	$I_{GSS}$	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 10$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	3	3.75	4.5	V
Static drain-Source On-resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=4.5A$	-	0.65	0.75	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS}=15V, I_D=4.5A$	-	7.8	-	A
Forward on Voltage	$V_{SD}$	$I_{SD}=12A, V_{GS}=0$	-	-	1.5	V
Input Capacitance	$C_{ISS}$	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	-	1370	-	pF
Output Capacitance	$C_{OSS}$		-	156	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	37	-	pF
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD} = 300V, I_D=4A,$ $R_G= 4.7\Omega, V_{GS}=10V$	-	20	-	ns
Rise Time	$t_R$		-	20	-	ns
Turn-Off Delay Time	$t_{D(OFF)}$		-	55	-	ns
Fall Time	$t_F$		-	30	-	ns
Total Gate Charge	$Q_g$	$V_{DS}=480V, V_{GS}=10V$ $I_D=8A$	-	50	70	nC
Gate-source Charge	$Q_{gs}$		-	10	-	nC
Gate-drain Charge	$Q_{gd}$		-	25	-	nC
Reverse Recovery Time	$T_{rr}$	$I_{SD}=8A, V_{DD}=40V$ $dI_F/dt=100A/\mu s, T_j=150^\circ C$	-	570	-	ns
Reverse Recovery Charge	$Q_{rr}$		-	4.3	-	$\mu C$
Reverse Recovery Current	$I_{RRM}$		-	15	-	A

# N-Channel Enhancement Mode Field Effect Transistor

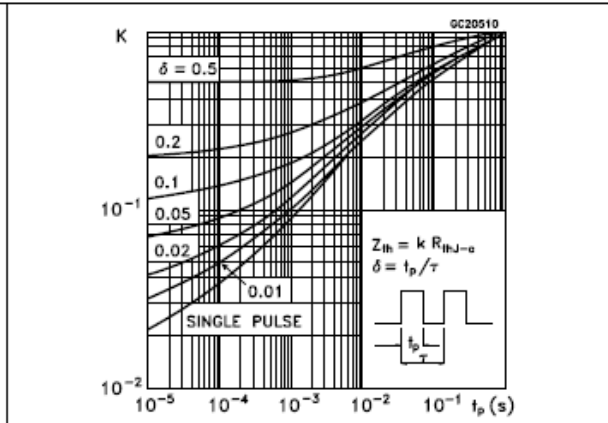
## BL10N65

TYPICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

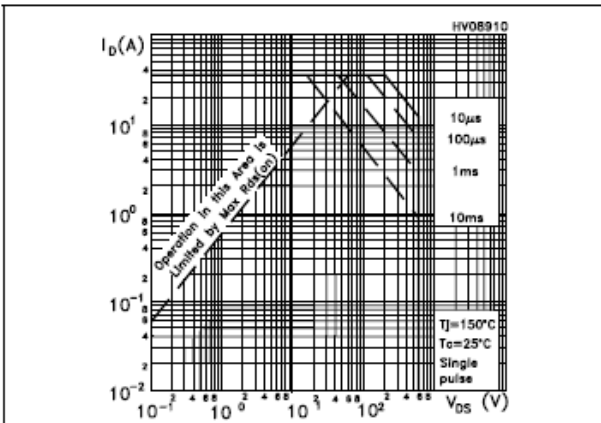
**Figure 2. Safe operating area for TO-220 / I<sup>2</sup>PAK / D<sup>2</sup>PAK**



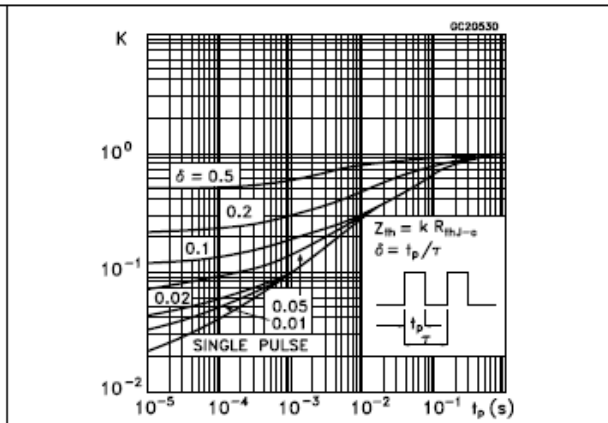
**Figure 3. Thermal impedance for TO-220 / I<sup>2</sup>PAK / D<sup>2</sup>PAK**



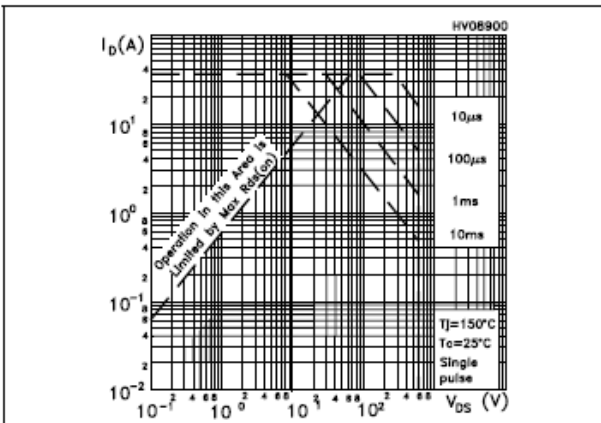
**Figure 4. Safe operating area for TO-247**



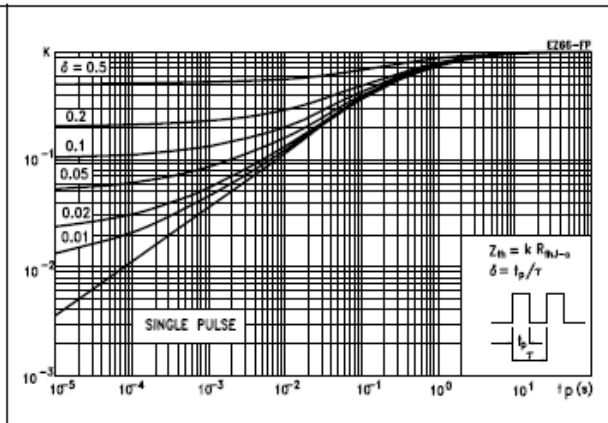
**Figure 5. Thermal impedance for TO-247**



**Figure 6. Safe operating area for TO-220FP**



**Figure 7. Thermal impedance for TO-220FP**



# N-Channel Enhancement Mode Field Effect Transistor

## BL10N65

Figure 8. Output characteristics

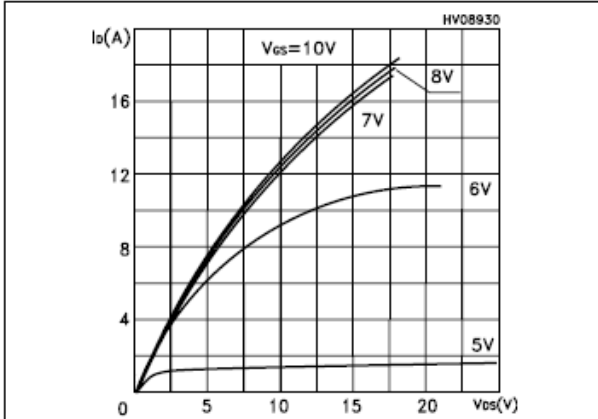


Figure 9. Transfer characteristics

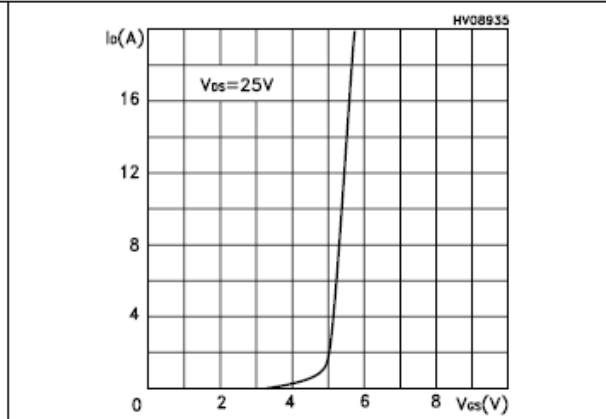


Figure 10. Transconductance

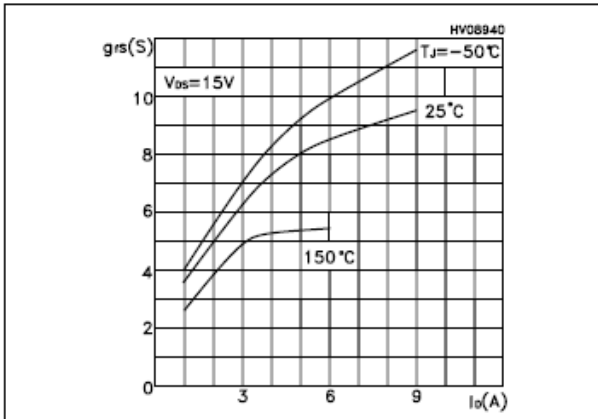


Figure 11. Static drain-source on resistance

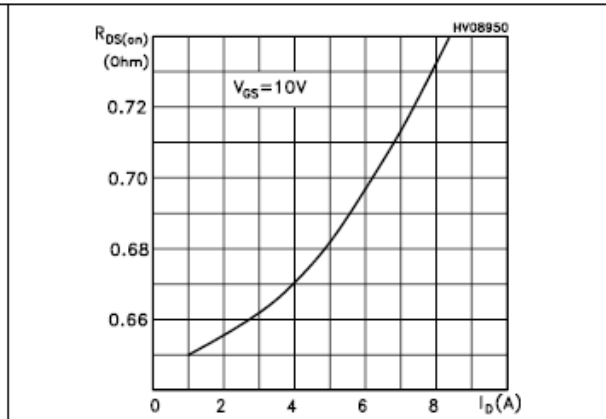


Figure 12. Gate charge vs gate-source voltage

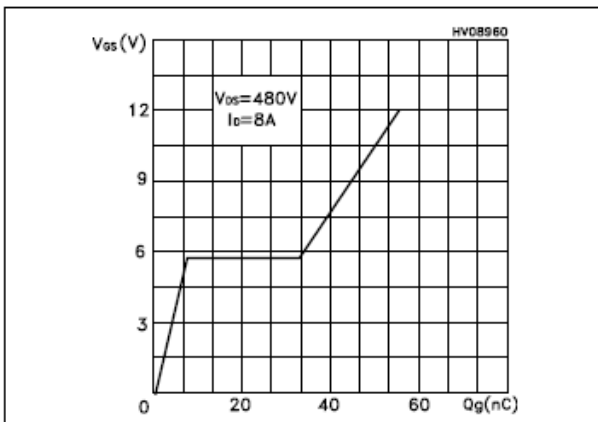
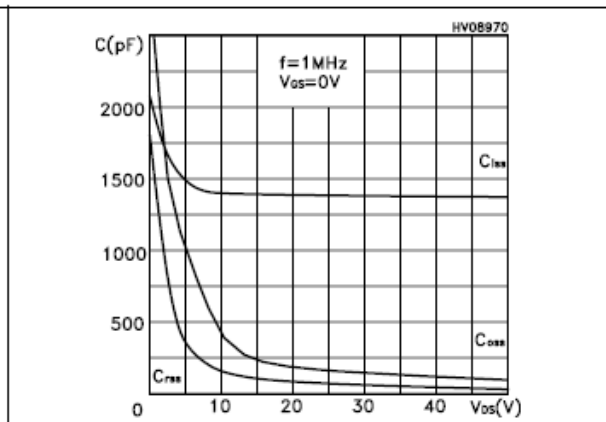


Figure 13. Capacitance variations



## N-Channel Enhancement Mode Field Effect Transistor

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Figure 14. Normalized gate threshold voltage vs temperature

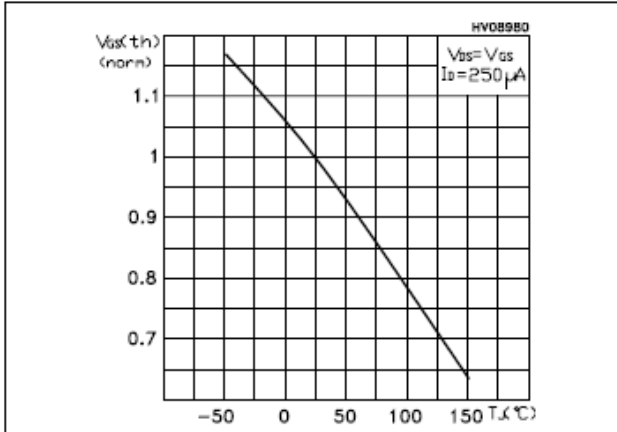


Figure 15. Normalized on resistance vs temperature

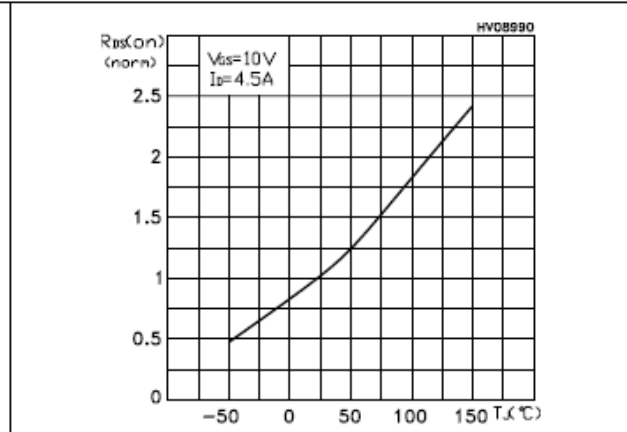


Figure 16. Source-drain diode forward characteristics

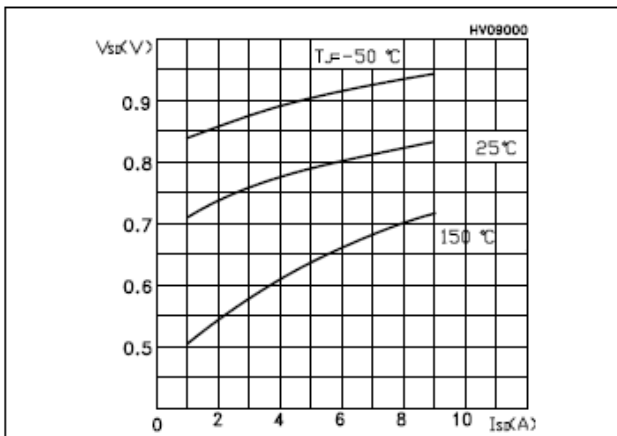


Figure 17. Maximum avalanche energy vs temperature

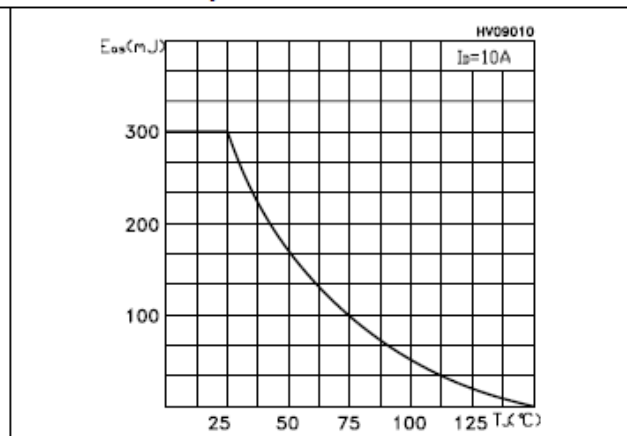
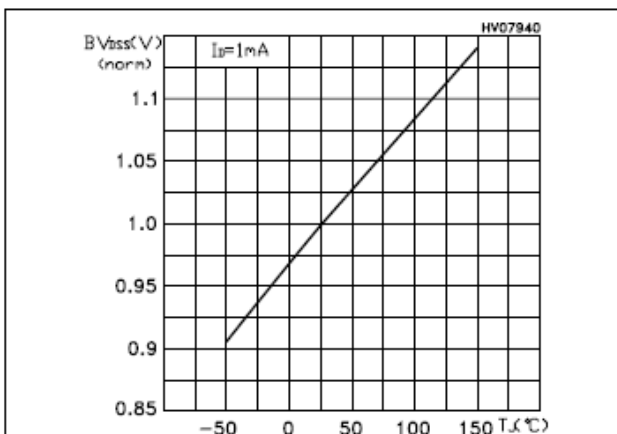


Figure 18. Normalized B<sub>VDS</sub> vs temperature



## N-Channel Enhancement Mode Field Effect Transistor

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### PACKAGE OUTLINE

Plastic surface mounted package

TO-220AB

