

General Description

The BL1302A57/S is an A-law monolithic PCM CODEC/filter which has the A/D and D/A conversion and a serial PCM interface. The device is fabricated using the advanced double-poly nwell CMOS process. It is pin compatible with TP3057.

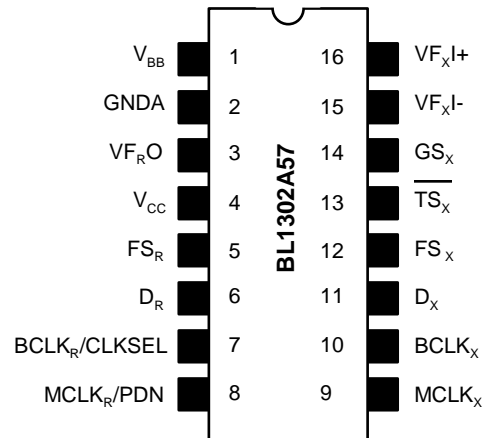
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded A-law PCM format. The decode portion consists of an expanding decoder, which reconstructs the

Analog signal from the companded A-law code, a low-pass filter which corrects for the $\sin x/x$ response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The device requires two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 KHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

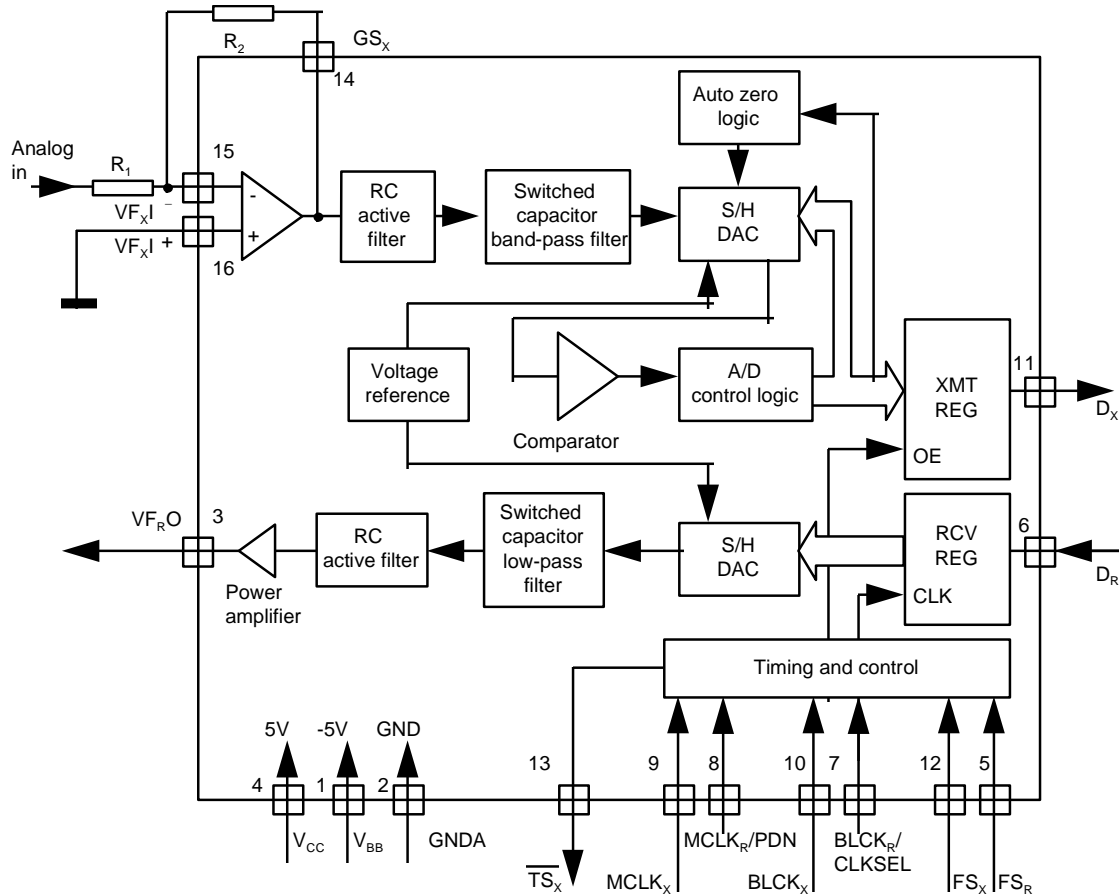
- Complete CODEC and filtering system (COMBO) including:
 - Transmit high-pass and low-pass filtering
 - Receive low-pass filter with $\sin x/x$ correction
 - Active RC noise filters
 - A-law compatible COder and DECOder
 - Internal precision voltage reference
 - Serial I/O interface
 - Internal auto-zero circuitry
- 16 pin DIP or SOP
- Designed for ITU application

Pin Assignment



- $\pm 5V$ operation
- Low power: Typical 50mW
 Stand-by 3mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces

Block Diagram



Pin Description

Symbol	Function
V _{BB}	Negative power supply pin. V _{BB} = - 5V ±5%
GNDA	Analog ground. All signals are referenced to this pin.
VF _R O	Analog output of the receive power amplifier.
V _{CC}	Positive power supply pin. V _{CC} = +5V ±5%
FS _R	Receive frame sync pulse which enables BCLK _R to shift PCM data into D _R . FS _R is an 8kHz pulse train.
D _R	Receive data input. PCM data is shifted into D _R following the FS _R leading edge.
BLCLK _R /CLKSEL	The bit clock which shifts data into D _R after the FS _R leading edge. May vary from 64kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and BCLK _x is used for both transmit and receive directions(see Table 1).
MCLK _R /PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it may be needed as a power-down control. When MCLK _R is connected continuously low, MCLK _x is selected for all internal timing. When MCLK _R is connected continuously high, the device is powered down.
MCLK _x	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. In synchronous mode, it is also used as receive master clock.
FS _x	Transmit frame sync pulse input which enables BCLK _x to shift out the PCM data on D _x . FS _x is an 8 KHz pulse train.
BCLK _x	The bit clock which shifts out the PCM data on D _x . May vary from 64 kHz to 2.048 MHz, but must be synchronous with MCLK _x .
D _x	The TRI-STATE PCM data output which is enabled by FS _x .
TS _x	Open drain output which pulses low during the encoder time slot.
GS _x	Analog output of the transmit input amplifier. Used to externally set gain.
VF _x I-	Inverting input of the transmit input amplifier.
VF _x I+	Non-inverting input of the transmit input amplifier.

Functional Description

- **Power-up**

When power is first applied, the internal power-on reset circuitry initializes the device and places it into a power-down state. Most of the analog and digital circuits are deactivated, and the D_x and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the MCLK_R/PDN pin and FS_x and/or FS_R pulses must be present.

Thus, 2 power-down control modes are available. The first is to pull the MCLK_R/PDN pin high; the alternative is to hold both FS_X and FS_R input continuously low---the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, Dx, will remain in the high impedance state until the second FS_X pulse.

- **Synchronous operation**

For synchronous operation, the same master clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to MCLK_X and the MCLK_R/PDN pin can be used as a power-down control. A low level on MCLK_R/PDN powers up the device and a high level powers down the device. In either case, MCLK_X will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to BCLK_X and the BCLK_R/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544MHz or 2.048MHz. For 1.544MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the BCLK_R/CLKSEL pin, BCLK_X will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of BCLK_R/CLKSEL. In this synchronous mode, the bit clock, BCLK_X and BCLK_R, may be from 64kHz to 2.048 MHz. The frequency of BCLK_X and BCLK_R are not necessary to be equal, but must be synchronous with MCLK_X.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled Dx output on the positive edge of BCLK_X. After 8 bit clock periods, the TRI-STATE Dx output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of BCLK_X (or BCLK_R if running). FS_X and FS_R must be synchronous with MCLK_{X/R}.

Table Selection of Master Clock Frequencies

BCLK _R /CLKSEL	Master Clock Frequency Selected
Clocked	2.048MHz
0	1.536MHz or 1.544MHz
1	2.048MHz

- **Short frame operation**

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, frame sync pulse, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 1. With FS_X high during a falling edge of BCLK_X, the next rising edge of BCLK_X enables the Dx TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK_R (BCLK_X, if BCLK_R is a fixed level), the next falling edge of BCLK_R latches in the sign bit. The following seven falling edges latch in the seven remaining bits.

- **Long frame operation**

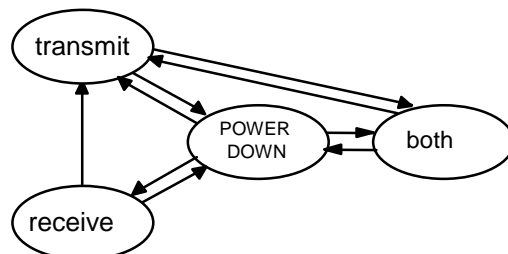
To use the long frame mode, the frame sync pulse, FS_X and FS_R , must be three or more bit clock periods long, with timing relationships specified in Figure 2. Based on the transmit frame sync, FS_X , the device will sense whether short or long frame sync pulse are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160ns. The D_X tri-state output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R , will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ if $BCLK_R$ is a fixed level).

- **Single channel operation**

Keeping FS_R input continuously low, the device enters into transmit channel operation, the data at D_R input will be ignored. Keeping FS_X input continuously low, the device enters into receive channel operation. The most part of transmit circuitry ceases to work, D_X and TS_X output will be in high impedance. If $MCLK_R$ input is a clock, it is the internal master clock. If $MCLK_R$ input is not a clock, $MCLK_X$ is the internal master clock, and $MCLK_X$ must be synchronous with FS_R . If $BCLK_R$ input is not a clock, $BCLK_X$ is the internal bit clock. In receive channel operation, the length of FS_R determines whether it is short or long frame.

- **Switch of operation**

See picture below, it is not recommended that the switching from both channels to receive only or switching from receive channel only to transmit channel only.



- **Transmit section**

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to A-law coding conventions. A built-in bandgap voltage reference is used to provide an input overload of nominally 2.492V peak. The FS_X frame pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165us (due to transmit filter) plus 125us (due to encoding delay), which totals 290us. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

- **Receive section**

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law and the 5th order low pass filter corrects for the $\sin x/x$ attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifier capable of driving a 600ohm load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R , the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLKx$) periods. At the end of the decoder time slot, the decoding cycle begins. The total decoder delay approximately 280 us.

Electrical parameters and timing

Absolute Maximum Ratings

Rating	Value	Unit
V_{CC} to GNDA	7	V
V_{BB} to GNDA	-7	V
Voltage at any Analog Input or Output	$V_{CC}+0.3$ to $V_{BB}-0.3$	V
Voltage at any Digital Input or Output	$V_{CC}+0.3$ to $GNDA-0.3$	°C
Operating Temperature Range	-25 to +125	°C
Storage Temperature Range	-65 to +150	°C
ESD (Human Body Model)	1000	V
Latch-Up Immunity at any Pins	100	mA

Electrical Characteristics: $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $T_A = 0^\circ C$ to $+70^\circ C$. All signals referenced to GNDA. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital INTERFACE						
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	$Dx, I_L=3.2mA$			0.4	V
		$TSx, I_L=3.2mA, \text{Open Drain}$			0.4	V
V_{OH}	Output High Voltage	$Dx, I_H= -3.2mA$	2.4			V
I_{IL}	Input Low Current	$GNDA \leq V_{IN} \leq V_{IL}, \text{All digital inputs}$	-10		10	μA
I_{IH}	Input High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	-10		10	μA
IOZ	Output Current in High Impedance State (TRI-STATE)	$Dx, GNDA \leq V_O \leq V_{CC}$	-10		10	μA

Analog Interface with transmit input amplifier						
I_{IXA}	Input Leakage Current	$-2.5V \leq V \leq +2.5V$, V_{FXI+} or V_{FXI-}	-200		200	nA
R_{IXA}	Input Resistance	$-2.5V \leq V \leq +2.5V$, V_{FXI+} or V_{FXI-}	10			M Ω
R_{OXA}	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_{LXA}	Load Resistance	GSx	10			k Ω
C_{LXA}	Load Capacitance	GSx			50	pF
V_{OXA}	Output Dynamic Range	GSx, $R_L \geq 10k\Omega$	-2.8		2.8	V
A_{VXA}	Voltage Gain	V_{FXI+} to GSx	5000			V/V
F_{UXA}	Unity Gain Bandwidth		1	2		MHz
V_{OSXA}	Offset Voltage		-20		20	mV
V_{CMXA}	Common-Mode Voltage	CMRRXA > 60dB	-2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	60			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER						
R_{ORF}	Output Resistance	Pin V_{FO}		1	3	Ω
R_{LRF}	Load Resistance	$V_{FO} = \pm 2.5V$	600			Ω
C_{LRF}	Load Capacitance				500	pF
V_{OSRO}	Output DC Offset Voltage		-200		200	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load (Note)		0.14	0.3	mA
I_{BB0}	Power-Down Current	No Load (Note)		0.20	1.5	mA
I_{CC1}	Power-Up Active Current	No Load		5.0	10	mA
I_{BB1}	Power-Up Active Current	No Load		5.0	10	mA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications: $V_{CC} = +5.0 \pm 5\%$, $V_{BB} = -5.0 \pm 5\%$, $T_a = 0^\circ C \sim +70^\circ C$. All signals referenced to GNDA. Typicals specified at $V_{OH} = +5.0V$, $V_{BB} = -5.0V$, $T_H = 25^\circ C$. All timing parameters are assured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	Depends on		1.536		MHz

		BCLK _R /CLKSEL Pin. MCLK _X and MCLK _R		1.544 2.048		MHz MHz
t _{RM}	Rise Time of Master Clock	MCLK _X and MCLK _R			50	ns
t _{FM}	Fall Time of Master Clock	MCLK _X and MCLK _R			50	ns
t _{PB}	Period of Bit Clock		485	488	15725	ns
t _{RB}	Rise Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t _{FB}	Fall Time of Bit Clock	BCLK _X and BCLK _R			50	ns
t _{WMH}	Width of Master Clock High	MCLK _X and MCLK _R	160			ns
t _{WML}	Width of Master Clock Low	MCLK _X and MCLK _R	160			ns
t _{SBFM}	Set-Up Time from BCLK _X High to MCLK _X Falling Edge	First Bit Clock after the Leading Edge of FS _X	100			ns
t _{SFFM}	Set-up Time from FS _X High to MCLK _X Falling Edge	Long Frame Only	100			ns
t _{WBH}	Width of Bit Clock High	VIH=2.2V	160			ns
t _{WBL}	Width of Bit Clock Low	VIL=0.6V	160			ns
t _{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t _{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	0			ns
t _{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t _{DBD}	Delay Time from BCLK _X High to Data Valid	Load=150 pF plus 2 LSTTL	0		140	ns
t _{DBTS}	Delay Time to TS _X Low	Load=150 pF plus 2 LSTTL Loads	0		140	ns
t _{DZC}	Delay Time from BCLK _X Low to Data Output Disabled	CL=0 pF to 150 pF	50		165	ns
t _{DZF}	Delay Time to Valid Data from FS _X or BCLK _X , Whichever Comes Later	CL=0 pF to 150 pF	20		165	ns
t _{SDB}	Set-Up time from D _R Valid to BCLK _{R/X} Low		50			ns
t _{HBD}	Hold Time from BCLK _{R/X} Low to D _R Invalid		50			ns
t _{SF}	Set-Up Time from FS _{X/R} to	Short Frame Sync Pulse	50			ns

	BCLK _{X/R} Low	(1 Bit Clock Period Long)			
t_{HF}	Hold Time from BCLK _{X/R} Low to FS _{X/R} Low	Short Frame Sync Pulse (1 bit Clock Period Long)	100		ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS _X or FS _R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	100		ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64K Bit/s Operating Mode	160		ns

Timing diagrams

Figure 1. Short Frame Sync Timing

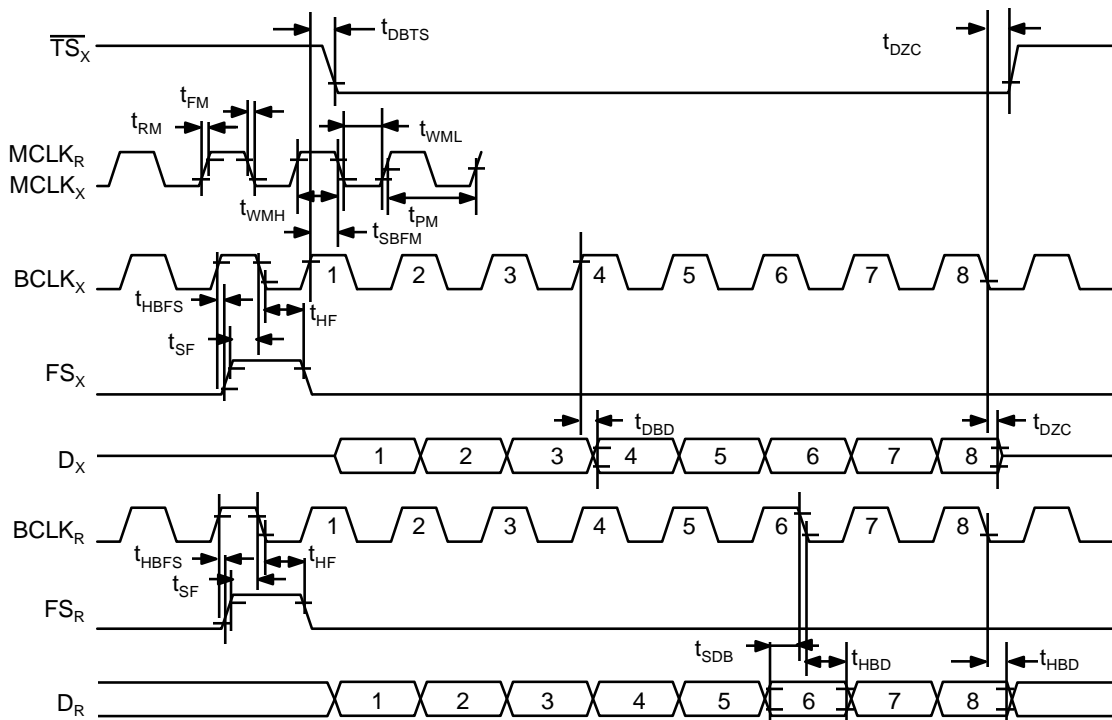
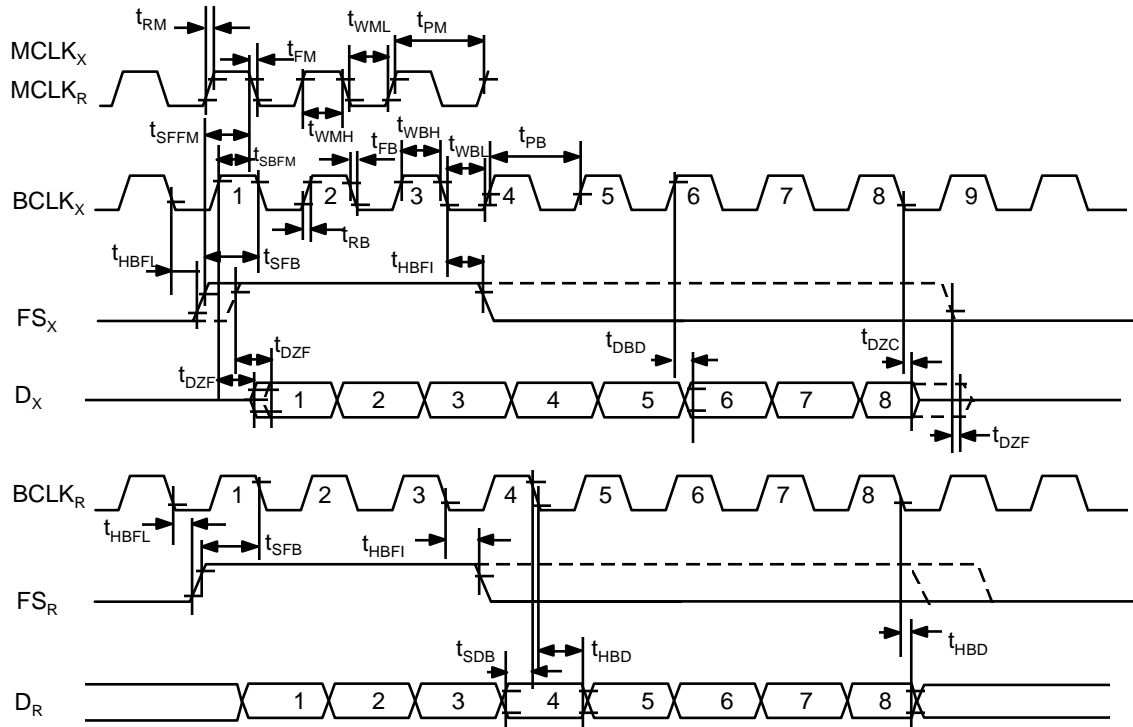


Figure 2. Long Frame Sync Timing


Transmission Characteristics: $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, $GNDA=0V$, $T_A = 0^\circ C$ to $+70^\circ C$, $f=1.02kHz$, $V_{in}=0dBm0$, transmit input amplifier connected for unity gain inverting.
 Typicals are specified at $V_{CC} = +5V$, $V_{BB} = -5.0V$, $T_A = 25^\circ C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Amplitude response						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm(600Ω) 0 dBm0		1.2276		V _{rms}
t_{MAX}	Virtual Decision Valve Defined Per CCITT Rec. G711	Max Overload Level (3.14 dBm0)		2.492		V _{PK}
G_{XA}	Transmit Gain, Absolute	$T_A=25^\circ C$, $V_{CC}=5V$, $V_{BB}=-5V$ Input at $G_{SX}=0$ dBm0 at 1020 Hz	-0.25		0.25	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	$f=16Hz$ $f=50Hz$ $f=60Hz$ $f=200Hz$	-1.8		-40 -30 -26 -0.1	dB

		f=300Hz-3000Hz	-0.15		0.15	dB
		f=3300Hz	-0.35		0.05	dB
		f=3400Hz	-0.7		0	dB
		f=4000Hz			-14	dB
		f=4600Hz and Up, Measure Response from 0 Hz to 4000 Hz			-32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	-0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	-0.05		0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=-10dBm0 VFxI+/-40dBm0 to +3dBm0 VFxI+/-50dBm0 to -40dBm0 VFxI+/-55dBm0 to -50dBm0	-0.2 -0.4 -1.2		0.2 0.4 1.2	dB dB dB
G_{RA}	Receive Gain, Absolute	$T_A=25^{\circ}C, V_{CC}=5V, V_{BB}=-5V$ Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	-0.25		0.25	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0Hz to 3000 Hz f=3300Hz f=3400Hz f=4000Hz	-0.15 -0.35 -0.7		0.15 0.05 0 -14	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	-0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	-0.05		0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level				

		=-40 dBm0 to +3 dBm0	-0.2		0.2	dB
		=-50 dBm0 to -40 dBm0	-0.4		0.4	dB
		=-55 dBm0 to -50 dBm0	-1.2		1.2	dB
V _{RO}	Receive Output Drive Level	R _L =600Ω	-2.5		2.5	V
Envelope delay distortion with frequency						
D _{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	us
D _{XR}	Transmit Delay, Relative to D _{XA}	f=500 Hz - 600 Hz		195	220	us
		f=600 Hz - 800 Hz		120	145	us
		f=800 Hz - 1000 Hz		50	75	us
		f=1000 Hz - 1600 Hz		20	40	us
		f=1600 Hz - 2600 Hz		55	75	us
		f=2600 Hz - 2800 Hz		80	105	us
		f=2800 Hz - 3000 Hz		130	155	us
D _{RA}	Receive Delay, Absolute	f=1600 Hz		270	290	us
D _{RR}	Receive Delay, Relative to D _{RA}	f=500 Hz - 1000 Hz	-40	-25		us
		f=1000 Hz - 1600 Hz	-30	-20		us
		f=1600 Hz - 2600 Hz		70	90	us
		f=2600 Hz - 2800 Hz		100	125	us
		f=2800 Hz - 3000 Hz		145	175	us
Noise						
N _{XP}	Transmit Noise, P Message Weighted			-74	-67	dBm0p
N _{RP}	Receive Noise, P Message Weighted	PCM Code Equals Positive Zero		-82	-79	dBm0p
N _{RS}	Noise, Single Frequency	f=0kHz to 100 kHz, Loop Around Measurement, VFxI±=0 Vrms			-53	dBm0
PPSR _x	Positive Power Supply Rejection, Transmit	VFxI±= -50 dBm0 V _{cc} =5.0 V _{DC} +100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dB
NPSR _x	Negative Power Supply Rejection, Transmit	VFxI±= -50 dBm0 V _{cc} =-5.0 V _{DC} +100 mVrms f=0 kHz - 50 kHz (Note 2)	40			dB
PPSR _R	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero, V _{cc} =5.0V _{DC} +100mVrms Measure VF _{RO}				

		f=0 Hz - 4000 Hz	40			dBC
		f=4 kHz - 25 kHz	40			dB
		f=25 kHz - 50 kHz	36			dB
NPSR _R	Negative Power Supply Rejection, Receive	PCM code Equals Positive Zero, $V_{BB} = -5.0V_{DC} + 100mV_{rms}$ Measure V_{FRO}				
		f=0 Hz - 4000 Hz	40			dBC
		f=4 kHz - 25 kHz	40			dB
		f=25 kHz - 50 kHz	36			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D _R .				
		4600 Hz - 7600 Hz			-30	dB
		7600 Hz - 8400 Hz			-40	dB
		8400 Hz - 100,000 Hz			-30	dB
Distortion						
STD _x	Signal to Total Distortion	Sinusoidal Test Method				
STD _R	Transmit or Receive Half-Channel	(Note 3)				
		Level=3.0 dBm0	33			dBC
		=0 dBm0 to -30 dBm0	36			dBC
		=-40 dBm0 XMT	30			dBC
		RCV	14			dBC
		=-55 dBm0 XMT	15			dBC
		RCV				
SFD _x	Single Frequency Distortion, Transmit				-46	dB
SFD _R	Single frequency Distortion, Receive				-46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, $V_{Fx} = -4dBm0$ to $-21 dBm0$, Two Frequencies in the			-41	dB

		Range 300 Hz-3400Hz				
Crosstalk						
CT _{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f=300Hz-3400Hz D _R =Quiet PCM Code (Note 2)		-90	-75	dB
CT _{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f=300Hz-3400Hz, VF _{XI} =Multitone (Note1)		-90	-70	dB

Note 1: Measured by extrapolation from the distortion test result at -50 dBm0.

Note 2: PPSRx, NPSRx, and CTR-X are measured with a -50 dBm0 activation signal applied to VF_{XI}+.

Note 3: Device is measured using psophometric-weighted filter.

Encoding Format at Dx Output

V _{in} (at GS _x) = +Full-Scale	1 0 1 0 1 0 1 0
V _{in} (at GS _x) = 0V	1 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1
V _{in} (at GS _x) = -Full-Scale	0 0 1 0 1 0 1 0

Applications Information

Power supplies

While the pins of the device are well protected against electrical misuse, it is recommended that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a “hot” socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

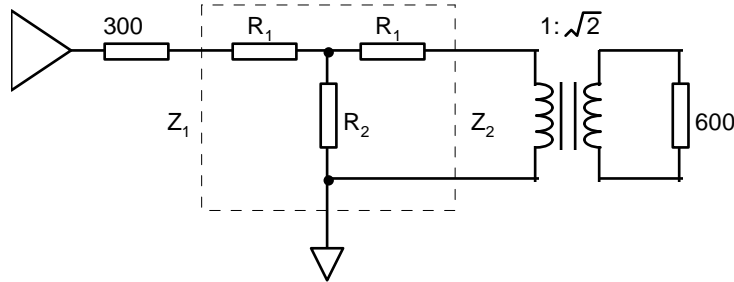
This common ground point should be decoupled to V_{CC} and V_{BB} with $10\mu F$ capacitors.

Receive gain adjustment

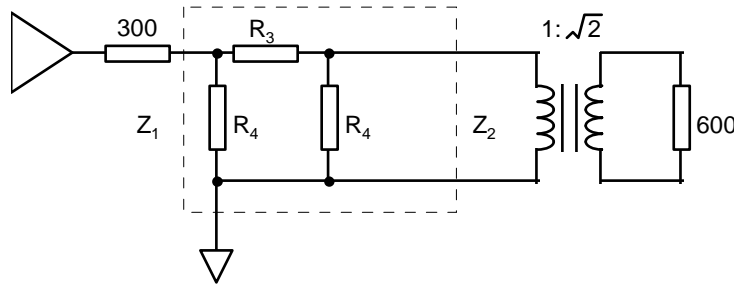
For applications where a device CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than $\pm 2.5V$ is required, the receive gain can be easily adjusted by inserting a matched T-pad or π -pad at the output. The followed table lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R_1 or R_4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss.

Attenuator diagram and table

T-Pad attenuator



π - Pad attenuator



Where

$$R_1 = Z_1 \frac{N^2 + 1}{N^2 - 1} - 2\sqrt{Z_1 Z_2} \cdot \frac{N}{N^2 - 1}$$

$$N = \sqrt{\frac{\text{Power in}}{\text{Power out}}}$$

$$R_2 = 2\sqrt{Z_1 Z_2} \cdot \frac{N}{N^2 - 1}$$

$$S = \sqrt{\frac{Z_1}{Z_2}}$$

$$R_3 = \sqrt{\frac{Z_1 Z_2}{2}} \cdot \left(\frac{N^2 - 1}{N} \right)$$

$$Z = \sqrt{Z_{sc} \cdot Z_{oc}}$$

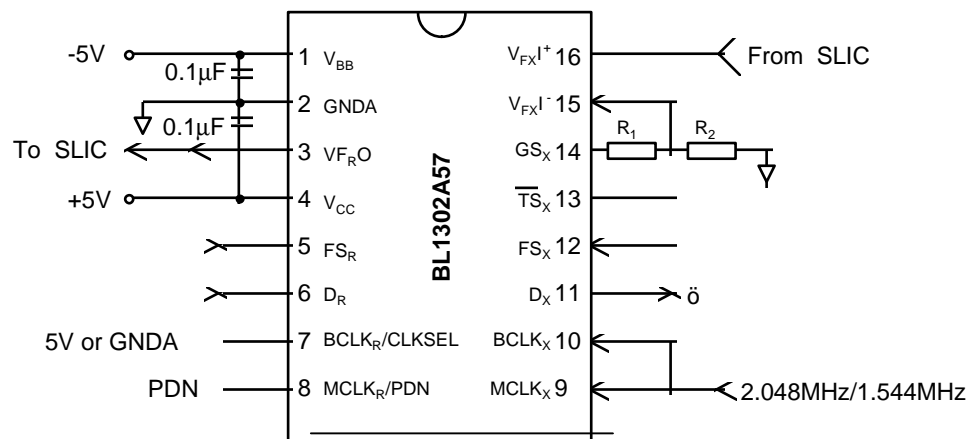
$$R_4 = Z_1 \left(\frac{N^2 - 1}{N^2 - 2NS + 1} \right)$$

Z_{sc} = impedance with short circuit termination

Z_{oc} = impedance with open circuit termination

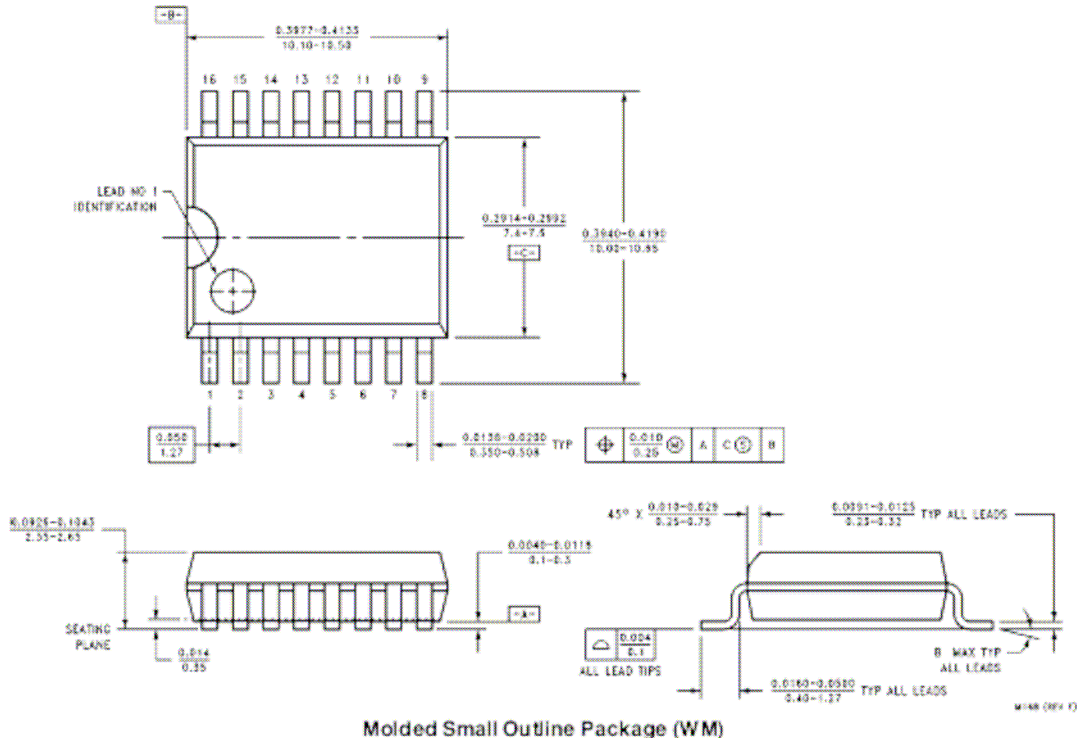
Attenuator Table for $Z_1=Z_2=300\Omega$, all values in Ω

dB	R_1	R_2	R_3	R_4	dB	R_1	R_2	R_3	R_4
0.1	1.7	26k	3.5	52k	6	100	402	224	900
0.2	3.5	13k	6.9	26k	7	115	380	269	785
0.3	5.2	8.7k	10.4	17.4k	8	379	284	317	698
0.4	6.9	6.5k	13.8	13k	9	143	244	370	630
0.5	8.5	5.2k	17.3	10.5k	10	156	211	427	527
0.6	10.4	4.4k	21.3	8.7k	11	168	184	490	535
0.7	12.1	3.7k	24.2	7.5k	12	180	161	550	500
0.8	13.8	3.3k	27.7	6.5k	13	190	142	635	473
0.9	15.5	2.9k	31.1	5.8k	14	200	125	720	450
1.0	17.3	2.6k	34.6	5.2k	15	210	110	816	430
2	34.4	1.3k	70	2.6k	16	218	98	924	413
3	51.3	850	107	1.8k	18	233	77	1.17k	386
4	68	650	144	1.3k	20	246	61	1.5k	366
5	84	494	183	1.1k					

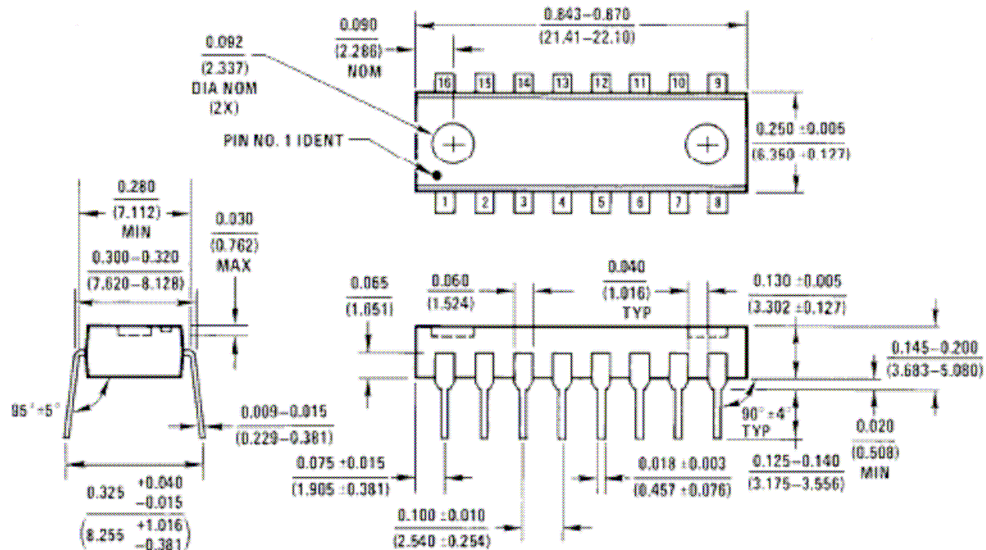
Typical synchronous application


Print Information

Physical Dimensions inches (millimeters)



Molded Small Outline Package (WM)



Molded Dual-In-Line Package (N)