

N-Channel Enhancement Mode Field Effect Transistor

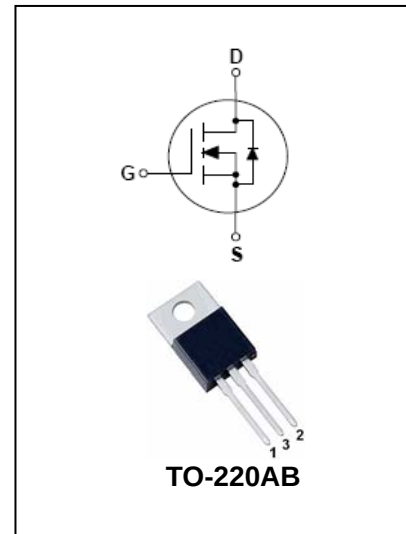
BL1N60

FEATURES

- $R_{DS(ON)} = 9.3\Omega @ V_{GS} = 10V$.
- Ultra Low gate charge (typical 5.0nC)
- Low reverse transfer capacitance ($CR_{SS} = \text{typical } 3.0 \text{ pF}$)
- Fast switching capability
- Avalanche energy specified
- Improved dv/dt capability, high ruggedness



Lead-free



MAXIMUM RATING operating temperature range applies unless otherwise specified

Symbol	Parameter	Value	Units
V_{DS}	Drain-Source voltage	600	V
V_{GS}	Gate -Source voltage	± 30	V
I_D	Continuous Drain current $T_C = 25^\circ\text{C}$	1.2	A
	Continuous Drain current $T_C = 100^\circ\text{C}$	0.76	A
E_{AS}	Single Pulse Avalanche Energy(Note3)	50	mJ
E_{AR}	Avalanche Energy, Repetitive(Note2)	4.0	mJ
I_{AR}	Avalanche Current(Note2)	1.2	A
ISD	Continuous Drain-Source Current	1.2	A
ISM	Pulsed Drain-Source Current	4.8	A
dv/dt	Peak Diode Recovery dv/dt(Note4)	4.5	V/ns
P_D	Power Dissipation	40	W
	Derating Fcator above 25°C	0.32	W/ $^\circ\text{C}$
$R_{\theta JC}$	Junction-to-Case	4	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction-to-Ambient	54	$^\circ\text{C/W}$
T_J, T_{stg}	Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$
T_L	Maximum Temperature for Soldering	+150	$^\circ\text{C}$

Note: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

3. $L=64\text{mH}$, $I_{AS}=1.2\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$

4. $ISD \leq 1.2\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$

N-Channel Enhancement Mode Field Effect Transistor

BL1N60

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
Bvdss Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	$I_D=250mA$	-	0.4	-	V/°C
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V
Drain to Source Leakage Current	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$	-	-	10	mA
		$V_{DS}=480V, T_a=125^\circ C$			100	
Static drain-Source on-resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=0.6A$	-	9.3	11.5	Ω
Gate-body Leakage Forward Reverse	I_{GSS}	$V_{GS}=\pm 30V$			± 100	nA
Forward Transconductance	g_{fs}	$V_{DS}=50V, I_D=0.6A$	-	0.9	-	S
Input Capacitance	C_{iss}	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$	-	120	150-	pF
Output Capacitance	C_{oss}		-	20	25	
Reverse Transfer Capacitance	C_{rss}		-	3.0	4.0	
Turn-on Delay Time	$t_{d(ON)}$	$I_D=1.2A, V_{DD}=300V$ $V_{GS}=10V$	-	5	20	ns
Rise Time	t_r		-	25	60	
Turn-Off Delay Time	$t_{d(OFF)}$		-	7	25	
Fall Time	t_f		-	25	60	
Total Gate Charge	Q_g	$I_D=1.2A, V_{DD}=480V$ $V_{GS}=10V$	-	5.0	6.0	nC
Gate to Source Charge	Q_{gs}		-	1.0		
Gate to Drain ("Miller") Charge	Q_{gd}		-	2.6		
Reverse Recovery Time	t_{rr}	$I_S=1.2A, T_J=25^\circ C$ $dI_F/dt=100A/\mu s$	-	160	-	ns
Reverse Recovery Charge	Q_{rr}	$V_{GS}=0V$	-	0.3	-	nC

Note: 1. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$
2. Essentially Independent of Operating Temperature

N-Channel Enhancement Mode Field Effect Transistor

BL1N60

PACKAGE OUTLINE

Plastic surface mounted package

TO-220AB

