Low Voltage I/O TOUCH SCREEN CONTROLLER

Features

- 2.2V to 5.25V operation
- 1.5V to 5.25V digital I/O
- Internal 2.5V reference
- 4-wire I/F
- Programmable 8 or 12 bit Resolution
- Direct battery measurement(0V to 6V)
- Temperature measurement
- Touch-pressure measurement
- Available in QFN-16 and TSSOP-16 package

General Description

The BL2046 is a 4-wire touch screen controller which supports a low-voltage I/O interface from 1.5V to 5.25V. The BL2046 has an on-chip 2.5V reference that can be used for the auxiliary input, battery monitor, and temperature measurement modes. The reference can also be powered down when not used to conserve power. The internal reference operates down to 2.7V supply voltage, while monitoring the battery voltage from 0V to 6V.

The BL2046 is a highly integrated controller for portable applications with 4-wire resistive touch panel such as, PDA, portable instruments, cellular phone, etc.

Applications

- Cellular phones
- Personal digital assistants
- Touch screen monitors
- Portable instruments

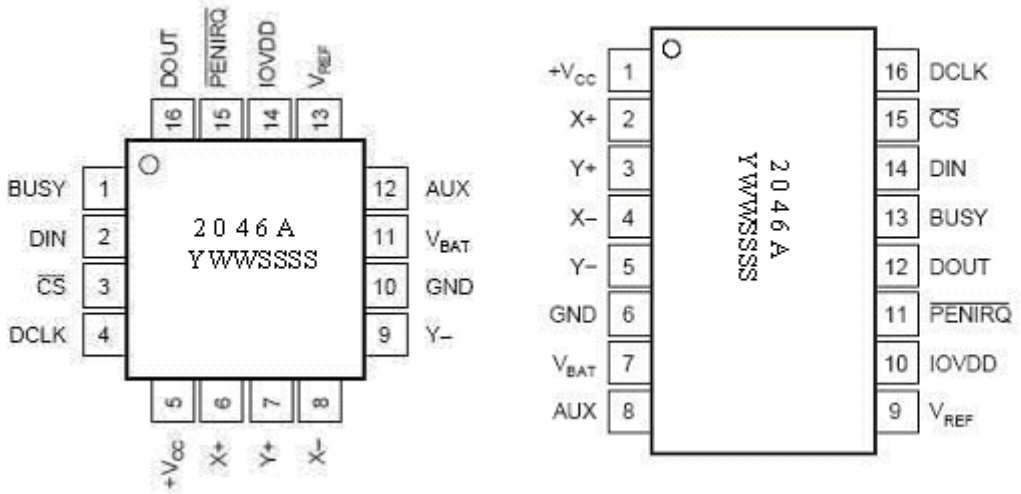
Order Information

Part Number	Package	Shipping
BL2046QN	QFN-16	3000pcs / Tape & Reel
BL2046TS	TSSOP-16	2500pcs / Tape & Reel

Absolute Maximum Ratings

$+V_{CC}$ and IOVDD to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to IOVDD + 0.3V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Pin Diagrams



2046A - product code
Y - assembly year
WW - assembly week
SSSS - digits from lot number

Pin Description

No.	Pin Name	Description
1	BUSY	Busy Output. This output is high impedance when $\overline{CS}$ is high.
2	DIN	Serial Data Input. If $\overline{CS}$ is low, data is latched on rising edge of DCLK.
3	$\overline{CS}$	Chip Select Input. Controls conversion timing and enables the serial input/output register. $\overline{CS}$ high = power-down mode (ADC only).

4	DCLK	External Clock Input. This clock runs the SAR conversion process and synchronizes serial data I/O.
5	+Vcc	Power Supply
6	X+	X+ Position Input
7	Y+	Y+ Position Input
8	X-	X– Position Input
9	Y-	Y– Position Input
10	GND	Ground
11	V_{BAT}	Battery Monitor Input
12	AUX	Auxiliary Input to ADC
13	V_{REF}	Voltage Reference Input/Output
14	IOVDD	Digital I/O Power Supply
15	$\overline{PENIRQ}$	Pen Interrupt
16	DOUT	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is high.

Typical Application Circuit

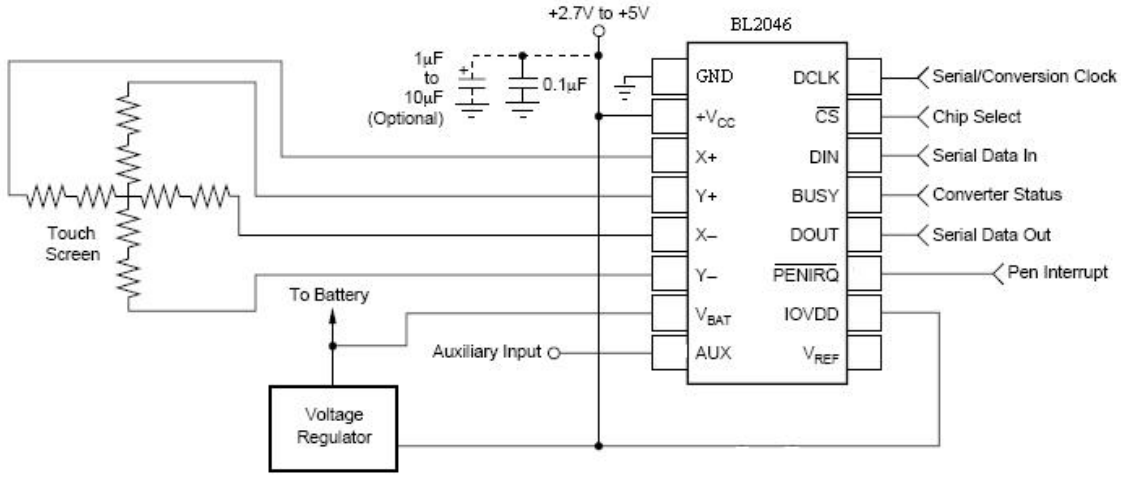


Figure 1 Typical Application Circuit of the BL2046

Electrical Characteristics

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = 2.5V internal voltage, f_{SAMPLE} = 125kHz, f_{CLK} = 16 • f_{SAMPLE} = 2MHz, 12-bit mode, digital inputs = GND or IOVDD, and $+V_{CC}$ must be •IOVDD, unless otherwise noted

PARAMETER	CONDITIONS	BL2046			UNITS
		MIN	TYP	MAX	
REFERENCE OUTPUT Internal Reference Voltage		2.46	250	2.54	V

Internal Reference Drift			15		ppm/℃
Quiescent Current			500		uA
ANALOG INPUT					
Full-Scale Input Span	Positive Input-Negative Input	0		VREF	V
Absolute Input Range	Positive Input	-0.2		+VCC+0.2	V
	Negative Input	-0.2		+0.2	V
Capacitance			25		PF
Leakage Current			0.1		uA
TEMPERATURE MEASUREMENT					
Temperature Range		-40℃		+85	℃
Resolution	Differential Method[3]		1.6		℃
Accuracy	TEMPO:[4]		0.3		℃
	Differential Method[3]		±2		℃
	TEMPO[4]		±3		℃
SYSTEM PERFORMANCE					
Resolution			12		Bits
No Missing Codes		11			Bits
Integral Linearity Error				±2	LSB[1]
Offset Error				±6	LSB
Gain Error	External V_{REF}			±4	LSB
Noise	Including Internal V_{REF}		70		uVrms
Power-Supply Rejection			70		dB
SAMPLING DYNAMICS					
Conversion Time				12	CLKCycles
Acquisition Time		3			CLKCycles
Throughput Rate				125	khz
Multiplexer Settling Time			500		ns
Aperture Delay			30		ns
Aperture Jitter			100		ps
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 50kHz		100		dB
BATTERY MONITOR					
Input Voltage Range		0.5		6.0	V
Input Impedance					
Sampling Battery			10		kΩ
Battery Monitor Off			1		GΩ
Accuracy	V_{BAT} = 0.5V to 5.5V, External				
	VREF =2.5V	-2		+2	%
	V_{BAT} = 0.5V to 5.5V,				
	Internal Reference	-3		+3	%
REFERENCE INPUT		1.0		+VCC	
Range					V
Input Impedance	SER/DFR = D, PD1 = 0, Internal Reference Off		1		GΩ

	Internal Reference On		250		Ω
DIGITAL INPUTfOUTPUT					
Logic Family			CMOS		
V_{IH}	$I\ I_{IH}\ I \leqslant +5uA$	IOVDD • 0.7		IOVDD+0.3	V
V_{IL}	$I\ I_{IL}\ I \leqslant +5uA$	-0.3		0.3 • IOVDD	V
V_{OH}	L_{OH} = -250 uA	IOVDD • 0.8			V
V_{OL}	L_{OL} = 250uA			0.4	V
Data Format			Straight Binary		
POWER-SUPPLY REQUIREMENTS					
$+V_{CC}$[5]	Specified Performance	2.7		3.6	V
	Operating Range	2.2		5.25	V
IOVDO[6]		1.5		$+V_{CC}$	V
Quiescent Current[7]	Internal Reference Off		280	650	uA
	Internal Reference On		780		uA
	fSAMPLE= 12.5kHz		220		uA
	Power-Down Mode with $\overline{CS}$=DCLK=DIN=IOVDD			3	uA
Power Dissipation	+VCC=+2.7V			1.8	mW
TEMPERATURE RANGE					
Specified Performance		-40		+85	℃
SWITCH DRIVERS					
Qn-Resistance					
Y+, X+			5		**Ω**
Y-.X-			6		**Ω**
Drive Current[2]	Duration 100ms			50	mA

NOTES: (1) LSB means least significant bit. With V_{REF} = +2.5V, one LSB is 610μV. (2) Assured by design, but not tested. Exceeding 50mA source current may result in device degradation. (3) Difference between TEMP0 and TEMP1 measurement, no calibration necessary. (4) Temperature drift is –2.1mV/°C. (5) BL2046 operates down to 2.2V. (6) IOVDD must be - $+V_{CC}$. (7) Combined supply current from $+V_{CC}$ and IOVDD. Typical values obtained from conversions on AUX input with PD0 = 0.

Analog Input

Table 1 and Table 2 show the relationship between the A2, A1, A0, and SER/$\overline{DFR}$ control bits and the configuration of the BL2046. The control bits are provided serially via the DIN pin (see the Digital Interface section of this data sheet for more details).

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The input current into the analog inputs depends on the

conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor . After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	V_{BAT}	AUX_{IN}	TEMP	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	X-DRIVERS	Y-DRIVERS
0	0	0			+IN (TEMP0)								Off	Off
0	0	1					+IN		Measure				Off	On
0	1	0	+IN										Off	Off
0	1	1					+IN				Measure		X–, On	Y+, On
1	0	0				+IN						Measure	X–, On	Y+, On
1	0	1						+IN		Measure			On	Off
1	1	0		+IN									Off	Off
1	1	1			+IN (TEMP1)								Off	Off

TABLE 1. Input Configuration (DIN), Single-Ended Reference Mode (SER/$\overline{DFR}$ high).

A2	A1	A0	+REF	–REF	Y–	X+	Y+	Y-POSITION	X-POSITION	Z_1-POSITION	Z_2-POSITION	DRIVERS ON
0	0	1	Y+	Y–		+IN		Measure				Y+, Y–
0	1	1	Y+	X–		+IN				Measure		Y+, X–
1	0	0	Y+	X–	+IN						Measure	Y+, X–
1	0	1	X+	X–			+IN		Measure			X+, X–

TABLE 2. Input Configuration (DIN), Differential Reference Mode (SER/$\overline{DFR}$ low).

Internal Reference

The BL2046 has an internal 2.5V voltage reference that can be turned on or off with the control bit, PD1 (see Table 5). Typically, the internal reference voltage is only used in the single-ended mode for battery monitoring, temperature measurement, and for using the auxiliary input. Optimal touch screen performance is achieved when using the differential mode.

Reference Input

The voltage difference between +REF and –REF sets the analog input range. The BL2046 operates with a reference in the range of 1V to $+V_{CC}$. There are several critical items concerning the reference input and its wide voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB size and is equal to the reference voltage divided by 4096 in 12-bit mode. Any offset or gain error inherent in the ADC appears to increase, in terms of LSB size, as the reference voltage is reduced. With a lower reference voltage, more care must be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal.

The voltage into the V_{REF} input directly drives the capacitor digital-to-analog converter (CDAC) portion of the BL2046. Therefore, the input current is very low.

There is also a critical item regarding the reference when making measurements while the switch drivers are ON. For this discussion, it is useful to consider the typical application of the BL2046.

This particular application shows the device being used to digitize a resistive touch screen. A measurement of the current Y-Position of the pointing device is made by connecting the X+ input to the ADC, turning on the Y+ and Y– drivers, and digitizing the voltage on X+. For this measurement, the resistance in the X+ lead does not affect the conversion. However, since the resistance between Y+ and Y– is fairly low, the on-resistance of the Y drivers does make a small difference. Under the situation outlined so far, it is not possible to achieve a 0V input or a full-scale input regardless of where the pointing device is on the touch screen because some voltage is lost across the internal switches. In addition, the internal switch resistance is unlikely to track the resistance of the touch screen, providing an additional source of error.

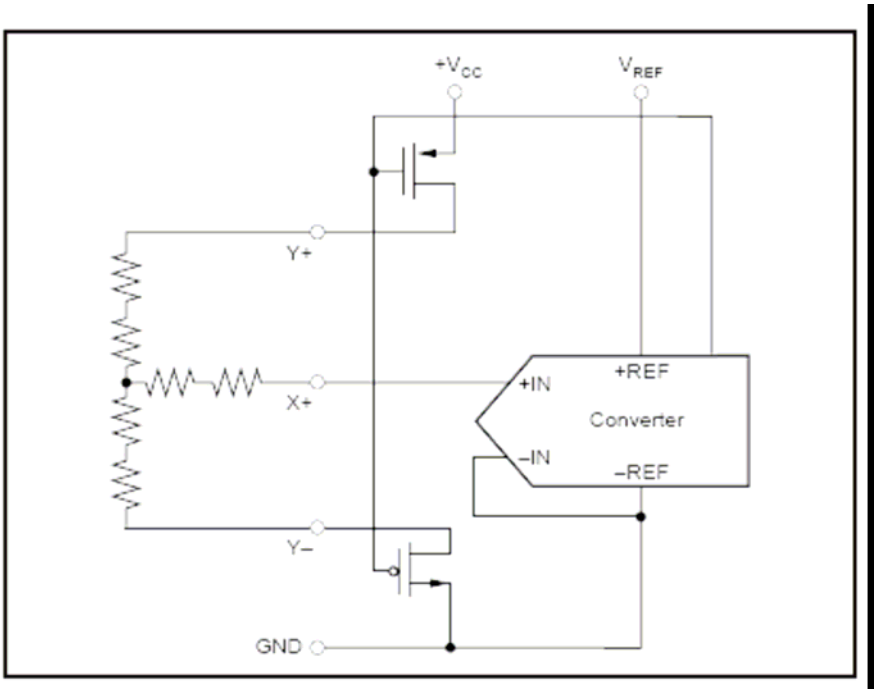


Figure 2. Diagram of Single-Ended Reference (SER/$\overline{DFR}$ high, Y switches enabled, X+ is analog input).

This situation can be remedied (see Figure 3) . By setting the SER/ $\overline{DFR}$ bit low, the +REF and –REF inputs are connected directly to Y+ and Y–, respectively, which makes the analog-to-digital conversion ratiometric. The result of the conversion is always a percentage of the external resistance, regardless of how it changes in relation to the on-resistance of the internal switches. Note that there is an important consideration regarding power dissipation when using the ratiometric mode of operation.

As a final note about the differential reference mode, it must be used with $+V_{CC}$ as the source of the +REF voltage and cannot be used with V_{REF}. It is possible to use a high-precision reference on V_{REF} and single-ended reference mode for measurements which do not need to be ratiometric. In some cases, it is possible to power the converter directly from a precision reference. Most references can provide enough power for the BL2046, but might not be able to supply enough current for the external load (such as a resistive touch screen).

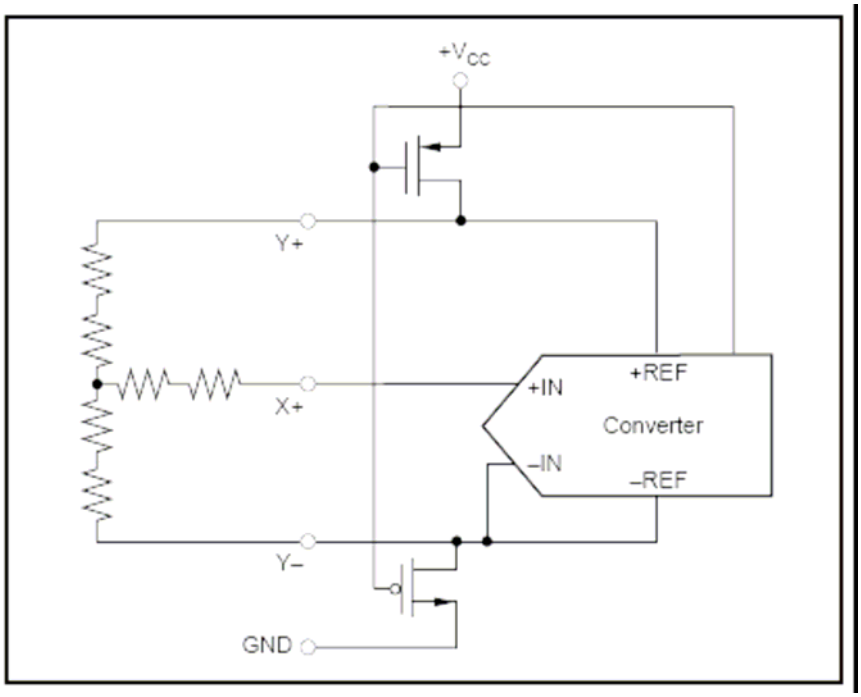


Figure 3. Diagram of Differential Reference (SER/$\overline{DFR}$ low, Y switches enabled, X+ is analog input).

Touch Screen Setting

In some applications, external capacitors may be required across the touch screen for filtering noise picked up by the touch screen. These capacitors provide a low-pass filter to reduce the noise, but cause a settling time requirement when the panel is touched that typically shows up as a gain error. There are several methods for minimizing or eliminating this issue. The problem is the input and/or reference has not settled to the final steady-state value prior to the ADC sampling the input(s) and providing the digital output. Additionally, the reference voltage may still be changing during the measurement cycle. Option 1 is to stop or slow down the BL2046 DCLK for the required touch screen settling time. This allows the input and reference to have stable values for the Acquire period (3 clock cycles of the BL2046; see Figure 7). This works for both the single-ended and the differential modes. Option 2 is to operate the BL2046 in the differential mode only for the touch screen measurements and command the BL2046 to remain on (touch screen drivers ON) and not go into power-down (PD0 = 1). Several conversions are made depending on the settling time required and the BL2046 data rate. Once the required number of conversions have been made, the processor commands the BL2046 to go into its power-down state on the last measurement. This process is required for X-Position, Y-Position, and Z-Position measurements. Option 3 is to operate in the 15 Clock-per-Conversion mode, which overlaps the analog-to-digital conversions and maintains the touch screen drivers on until commanded to stop by the processor (see Figure 11).

Tempeature Mesurement

In some applications, such as battery recharging, a measurement of ambient temperature is required. The temperature measurement technique used in the BL2046 relies on the characteristics of a semiconductor junction operating at a fixed current level. The forward diode voltage (V_{BE}) has a well-defined characteristic versus temperature. The ambient temperature can be predicted in applications by knowing the +25°C value of the V_{BE} voltage and then monitoring the delta of that voltage as the temperature changes. The BL2046 offers two modes of operation. The first mode requires calibration at a known temperature, but only requires a single reading to predict the ambient temperature. A diode is used (turned on) during this measurement cycle. The voltage across the diode is connected through the MUX for digitizing the forward bias voltage by the ADC with an address of A2 = 0, A1 = 0, and A0 = 0 (see Table 1 and Figure 4 for details). This voltage is typically 600mV at +25°C with a 20μA current through the diode. The absolute value of this diode voltage can vary a few millivolts. However, the TC of this voltage is very consistent at –2.1mV/°C. During the final test of the end product, the diode voltage would be stored at a known room temperature, in memory, for calibration purposes by the user. The result is an equivalent temperature measurement resolution of 0.3°C/LSB (in 12-bit mode).

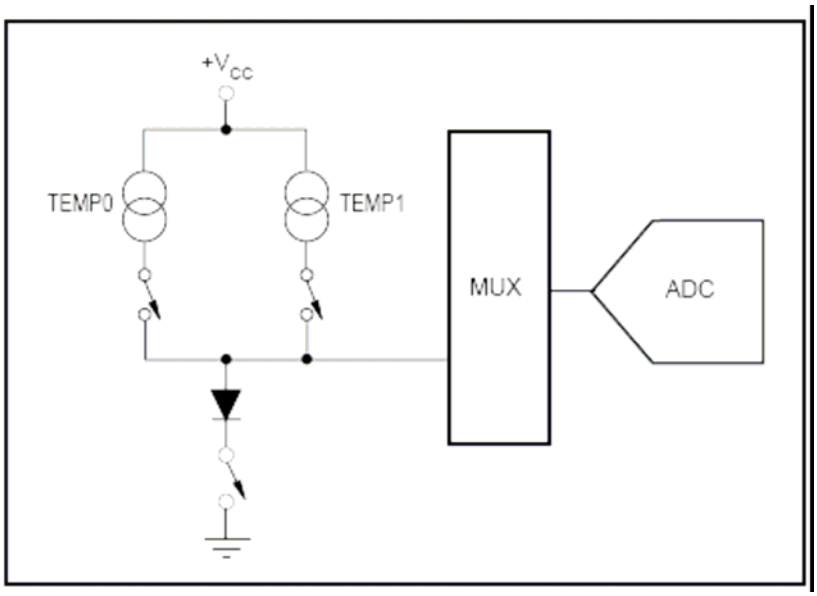


Figure 4. Functional Block Diagram of Temperature Measurement Mode.

The second mode does not require a test temperature calibration, but uses a two-measurement method to eliminate the need for absolute temperature calibration and for achieving 2°C accuracy. This mode requires a second conversion with an address of A2 = 1, A1 = 1, and A0 = 1, with a 91 times larger current. The voltage difference between the first and second conversion using 91 times the bias current is represented by kT/q • ln (N), where N is the current ratio = 91, k = Boltzmann's constant ($1.38054 \cdot 10^{-23}$ electron volts/ degrees Kelvin), q = the electron charge ($1.602189 \cdot 10^{-19}$ C), and T = the temperature in degrees Kelvin. This method can provide improved absolute temperature measurement over the first mode at the cost of less resolution (1.6°C/LSB). The equation for solving for °K is:

$$°K = q \cdot \triangle V/(k \cdot \ln (N)) \qquad (1)$$

where, $V = V(I_{91}) - V(I_1)$ (in mV)

$\therefore$ °K = 2.573 °K/mV • △V

°C = 2.573 •△V(mV) – 273°K

NOTE: The bias current for each diode temperature measurement is only on for 3 clock cycles (during the acquisition mode) and, therefore, does not add any noticeable increase in power, especially if the temperature measurement only occurs occasionally.

Battery Mesruement

An added feature of the BL2046 is the ability to monitor the battery voltage on the other side of the voltage regulator (DC/DC converter), as shown in Figure 5. The battery voltage can vary from 0V to 6V, while maintaining the voltage to the BL2046 at 2.7V, 3.3V, etc. The input voltage (V_{BAT}) is divided down by 4 so that a 5.5V battery voltage is represented as 1.375V to the ADC. This simplifies the multiplexer and control logic. In order to minimize the power consumption, the divider is only on during the sampling period when A2 = 0, A1 = 1, and A0 = 0 (see Table 1 for the relationship between the control bits and configuration of the BL2046).

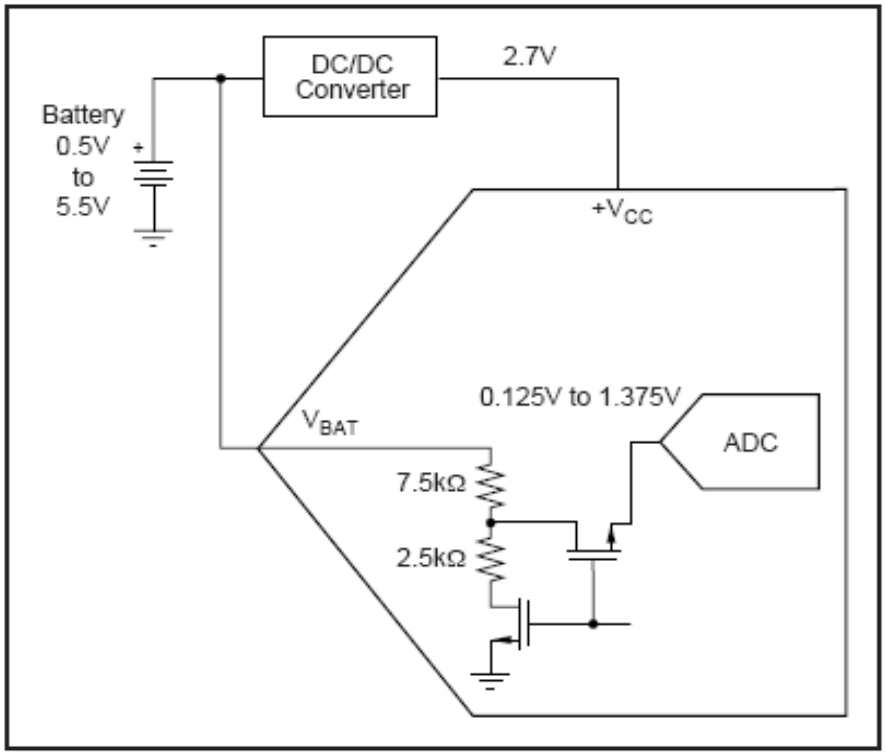


Figure 5. Battery Measurement Functional Block Diagram.

Pressure Mesurement

Measuring touch pressure can also be done with the BL2046. To determine pen or finger touch, the pressure of the touch needs to be determined. Generally, it is not necessary to have very high performance for this test, therefore, the 8-bit resolution mode is recommended (however, calculations will be shown here in the 12-bit resolution mode). There are several different ways of

performing this measurement. The BL2046 supports two methods. The first method requires knowing the X-plate resistance, measurement of the X-Position, and two additional cross panel measurements (Z_1 and Z_2) of the touch screen, as shown in Figure 6. Using Equation 2 calculates the touch resistance:

$$R_{TOUCH} = R_{X-plate} \bullet \frac{X-Position}{4096} \left(\frac{Z_2}{Z_1} - 1 \right) \qquad (2)$$

The second method requires knowing both the X-plate and Y-plate resistance, measurement of X-Position and Y-Position, and Z_1. Using Equation 3 also calculates the touch resistance:

$$R_{TOUCH} = \frac{R_{X-plate} \bullet X-Position}{4096} \left(\frac{4096}{Z_1} - 1 \right) - R_{Y-plate} \left(1 - \frac{Y-Position}{4096} \right) \qquad (3)$$

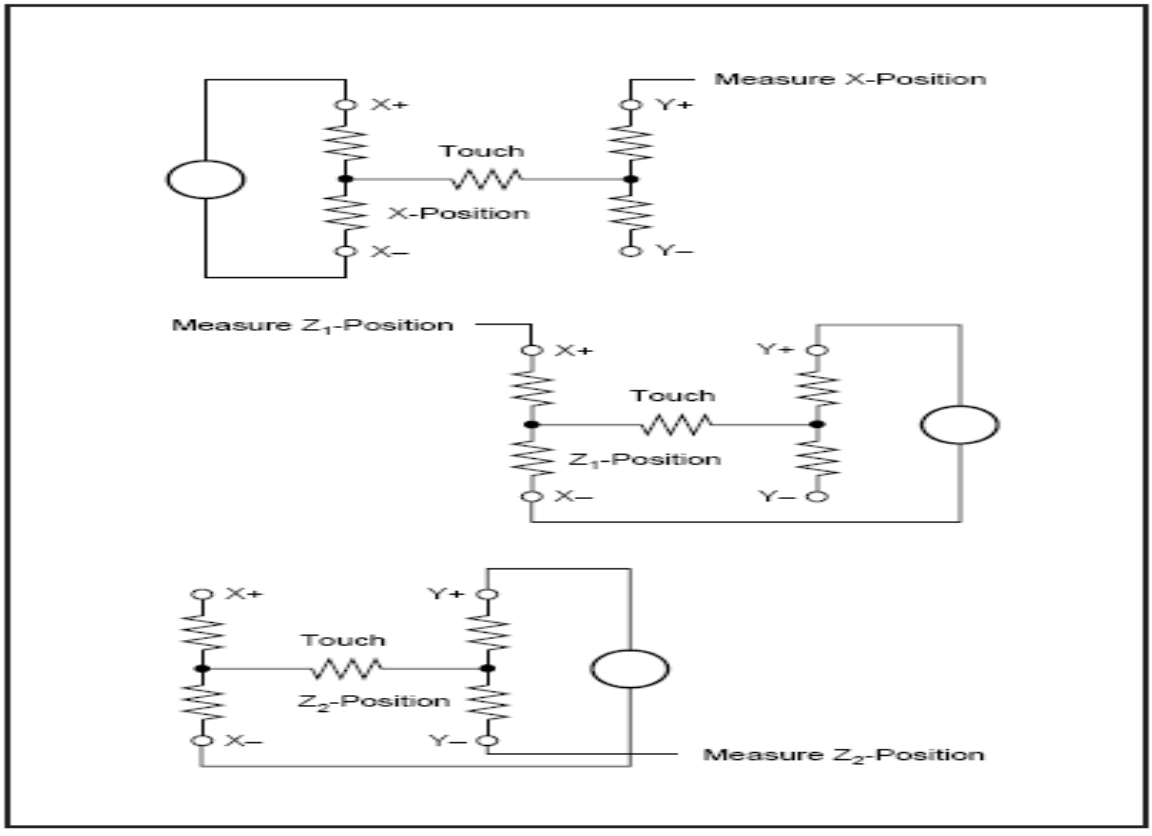


Figure 6. Pressure Measurement Block Diagrams.

Digital Interface

Figure 7 shows the typical operation of the BL2046 digital interface. This diagram assumes that the source of the digital signals is a microcontroller or digital signal processor with a basic serial interface. Each communication between the processor and the converter, such as SPI or SSI synchronous serial interface, consists of eight clock cycles. One complete conversion can be

accomplished with three serial communications for a total of 24 clock cycles on the DCLK input.

The first eight clock cycles are used to provide the control byte via the DIN pin. When the converter has enough information about the following conversion to set the input multiplexer and reference inputs appropriately, the converter enters the acquisition (sample) mode and, if needed, the touch panel drivers are turned on. After three more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the hold mode and the touch panel drivers turn off (in single-ended mode). The next 12 clock cycles accomplish the actual analog-to-digital conversion. If the conversion is ratiometric (SER/$\overline{DFR}$ = 0), the drivers are on during the conversion and a 13th clock cycle is needed for the last bit of the conversion result. Three more clock cycles are needed to complete the last byte (DOUT will be low), which are ignored by the converter.

Control Byte

The control byte (on DIN), as shown in Table 3, provides the start conversion, addressing, ADC resolution, configuration, and power-down of the BL2046. Tables 3 and 4 give detailed information regarding the order and description of these control bits within the control byte.

Bit7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
S	A2	A1	A0	MODE	SER/$\overline{DFR}$	PD1	PD0

TABLE 3. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start bit. Control byte starts with first high bit on DIN.A new control byte can start every 15th clock cycle in 12-bit conversion mode or every 11th clock cycle in 8-bit conversion mode (see Figure 11).
6-4	A2-A0	Channel Select bits. Along with the SER/$\overline{DFR}$ bit, these bits control the setting of the multiplexer input, touch driver switches, and reference inputs (see Tables 1 and 2).
3	MODE	12-Bit/8-Bit Conversion Select bit. This bit controls the number of bits for the next conversion: 12-bits (low) or 8-bits (high).
2	SER/$\overline{DFR}$	Single-Ended/Differential Reference Select bit. Along with bits A2-A0, this bit controls the setting of the multiplexer input, touch driver switches, and reference
1-0	PD1-PD0	inputs (see Tables 1 and 2). Power-Down Mode Select bits. Refer to Table V for details.

TABLE 4. Descriptions of the Control Bits within the Control Byte.

Initiate START—The first bit, the S bit, must always be high and initiates the start of the control byte. The BL2046 ignores inputs on the DIN pin until the start bit is detected.

Addressing—The next three bits (A2, A1, and A0) select the active input channel(s) of the input multiplexer (see Tables 1, 2), touch screen drivers, and the reference inputs.

MODE—The mode bit sets the resolution of the ADC. With this bit low, the next conversion has 12 bits of resolution, whereas with this bit high, the next conversion has 8 bits of resolution.

SER/$\overline{\text{DFR}}$—The SER/$\overline{\text{DFR}}$ bit controls the reference mode, either single-ended (high) or differential (low). The differential mode is also referred to as the ratiometric conversion mode and is preferred for X-Position, Y-Position, and Pressure- Touch measurements for optimum performance. The reference is derived from the voltage at the switch drivers, which is almost the same as the voltage to the touch screen. In this case, a reference voltage is not needed as the reference voltage to the ADC is the voltage across the touch screen. In the single-ended mode, the converter reference voltage is always the difference between the V_{REF} and GND pins.

If X-Position, Y-Position, and Pressure-Touch are measured in the single-ended mode, an external reference voltage is needed. The BL2046 must also be powered from the external reference. Caution should be observed when using the single-ended mode such that the input voltage to the ADC does not exceed the internal reference voltage, especially if the supply voltage is greater than 2.7V.

NOTE: The differential mode can only be used for X-Position, Y-Position, and Pressure-Touch measurements. All other measurements require the single-ended mode.

PD0 and PD1—Table 5 describes the power-down and the internal reference voltage configurations. The internal reference voltage can be turned on or off independently of the ADC. This can allow extra time for the internal reference voltage to settle to the final value prior to making a conversion. Make sure to also allow this extra wake-up time if the internal reference is powered down. The ADC requires no wake-up time and can be instantaneously used. Also note that the status of the internal reference power-down is latched into the part (internally) with BUSY going high. In order to turn the reference off, an additional write to the BL2046 is required after the channel has been converted.

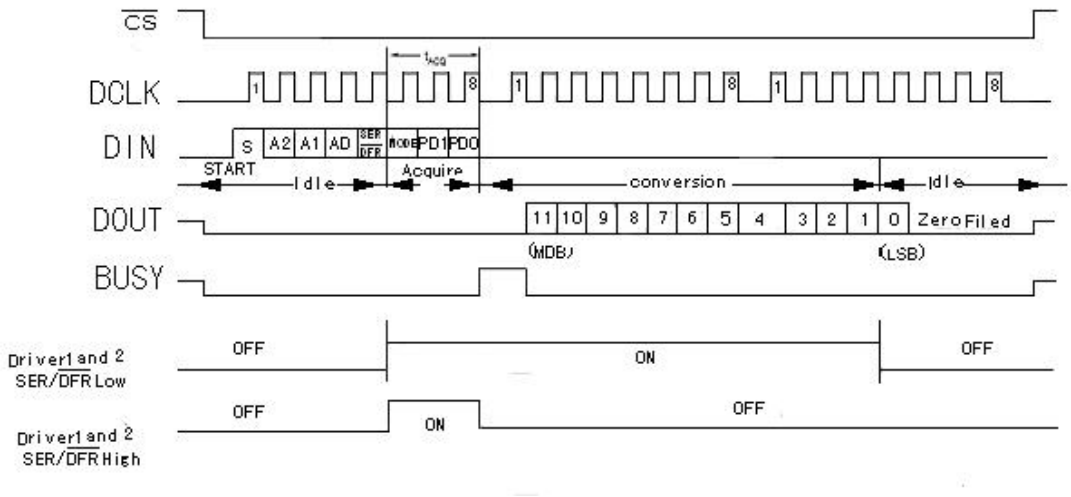


Figure 7. Conversion Timing, 24 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

PD1	PD0	$\overline{\text{PENIRQ}}$	DESCRIPTION
0	0	Enabled	Power-Down Between Conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to ensure full operation, and the very first conversion is valid. The Y– switch is on when in power-down.
0	1	Disabled	Reference is off and ADC is on.
1	0	Enabled	Reference is on and ADC is off.
1	1	Disabled	Device is always powered. Reference is on andADC is ON.

TABLE 5. Power-Down and Internal Reference Selection.

$\overline{\text{PENIRQ}}$ OUTPUT

The pen-interrupt output function is shown in Figure 8. While in power-down mode with PD0 = 0, the Y– driver is on and connects the Y-plane of the touch screen to GND. The $\overline{\text{PENIRQ}}$ output is connected to the X+ input through two transmission gates. When the screen is touched, the X+ input is pulled to ground through the touch screen.

In most of the BL2046 models, the internal pullup resistor value is nominally 50kΩ, but this may vary between 36K and 67kΩ given process and temperature variations. In order to assure a logic low of 0.35VDD is presented to the $\overline{\text{PENIRQ}}$ circuitry, the total resistance between the X+ and Y- terminals must be less than 21kΩ.

The -90 version of the BL2046 uses a nominal 90kΩ pullup resistor, which allows the total resistance between the X+ and Y- terminals to be as high as 30kΩ. Note that the higher pullup resistance will cause a slower response time of the $\overline{\text{PENIRQ}}$ to a screen touch, so user software should take this into account.

The $\overline{\text{PENIRQ}}$ output goes low due to the current path through the touch screen to ground, which initiates an interrupt to the processor. During the measurement cycle for X-, Y-, and Z-Position, the X+ input is disconnected from the $\overline{\text{PENIRQ}}$ internal pull-up resistor. This is done to eliminate any leakage current from the internal pull-up resistor through the touch screen, thus causing no errors.

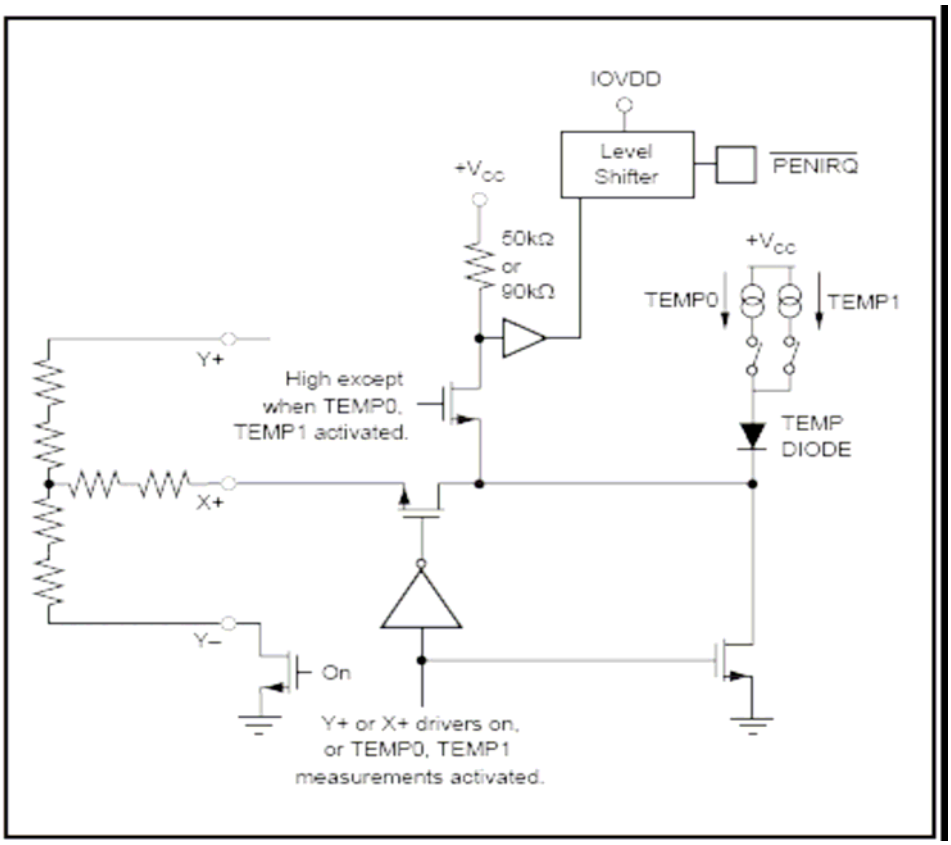


Figure 8. $\overline{\text{PENIRQ}}$ Functional Block Diagram.

Furthermore, the $\overline{\text{PENIRQ}}$ output is disabled and low during the measurement cycle for X-, Y-, and Z-Position. The $\overline{\text{PENIRQ}}$ output is disabled and high during the measurement cycle for battery monitor, auxiliary input, and chip temperature. If the last control byte written to the BL2046 contains PD0 = 1, the pen-interrupt output function is disabled and is not able to detect when the screen is touched. In order to re-enable the pen-interrupt output function under these circumstances, a control byte needs to be written to the BL2046 with PD0 = 0. If the last control byte written to the BL2046 contains PD0 = 0, the pen-interrupt output function is enabled at the end of the conversion. The end of the conversion occurs on the falling edge of DCLK after bit 1 of the converted data is clocked out of the BL2046.

It is recommended that the processor mask the interrupt $\overline{PENIRQ}$ is associated with whenever the processor sends a control byte to the BL2046. This prevents false triggering of interrupts when the $\overline{PENIRQ}$ output is disabled in the cases discussed in this section.

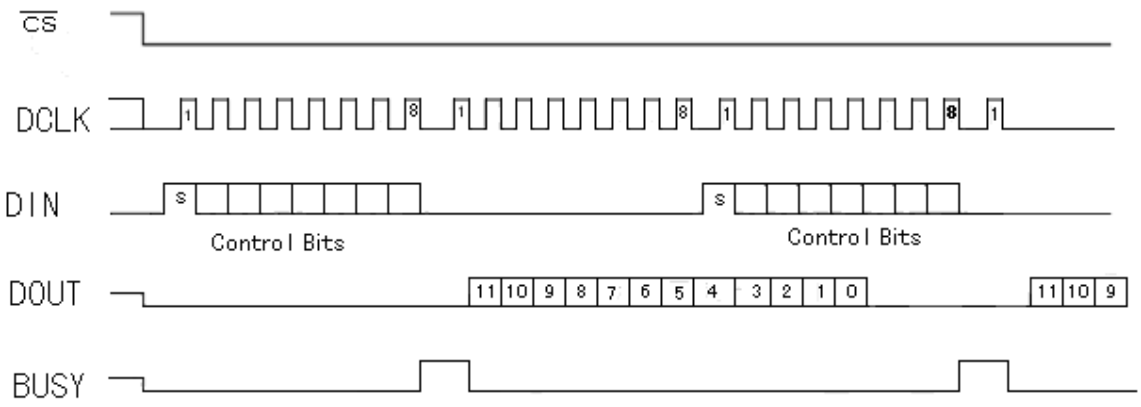


Figure 9. Conversion Timing, 16 Clocks-per-Conversion, 8-Bit Bus Interface. No DCLK delay required with dedicated serial port.

16 Clocks-per-Conversion

The control bits for conversion n + 1 can be overlapped with conversion n to allow for a conversion every 16 clock cycles, as shown in Figure 9. This figure also shows possible serial communication occurring with other serial peripherals between each byte transfer from the processor to the converter. This is possible, provided that each conversion completes within 1.6ms of starting. Otherwise, the signal that is captured on the input sample-and-hold may droop enough to affect the conversion result. Note that the BL2046 is fully powered while other serial communications are taking place during a conversion.

SYMBOL	DESCRIPTION	+V_{CC} • 2.7V, +V_{CC} • IOVDD • 1.5V, C_{LOAD} = 50pF			UNITS
		MIN	TYP	MAX	
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	DIN Valid Prior to DCLK Rising	100			ns
t_{DH}	DIN Hold After DCLK High	50			ns
t_{DO}	DCLK Falling to DOUT Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to DOUT Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to DOUT Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	10			ns
t_{CH}	DCLK High	200			ns
t_{CL}	DCLK Low	200			ns
t_{BD}	DCLK Falling to BUSY Rising/Falling			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE 6. Timing Specifications, T_A = –40°C to +85°C.

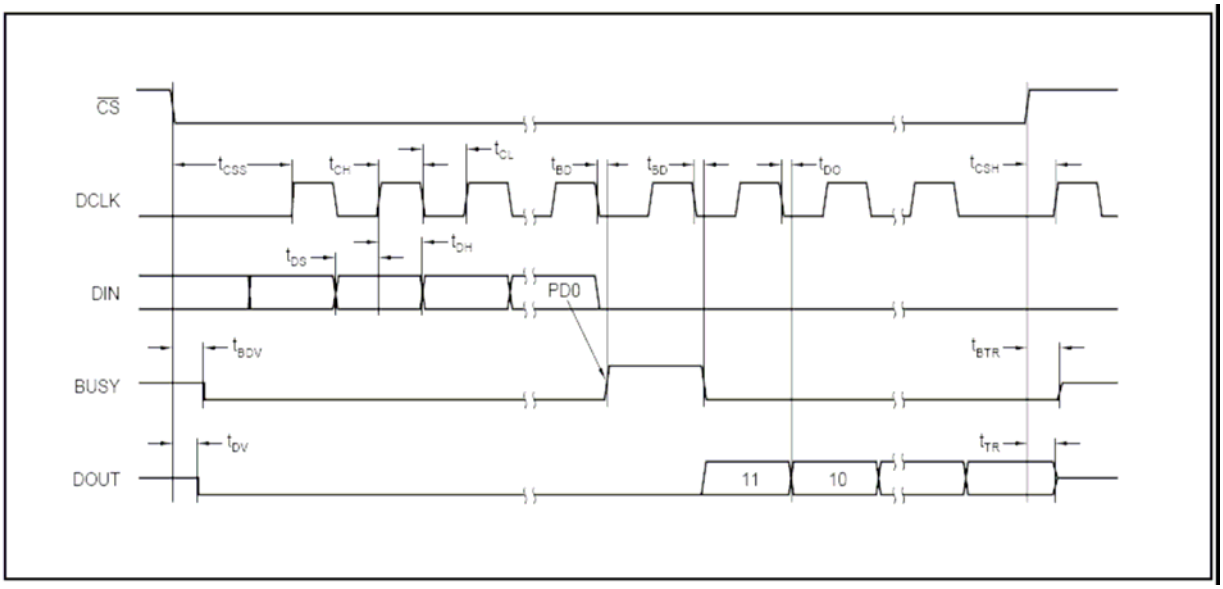


Figure 10. Detailed Timing Diagram.

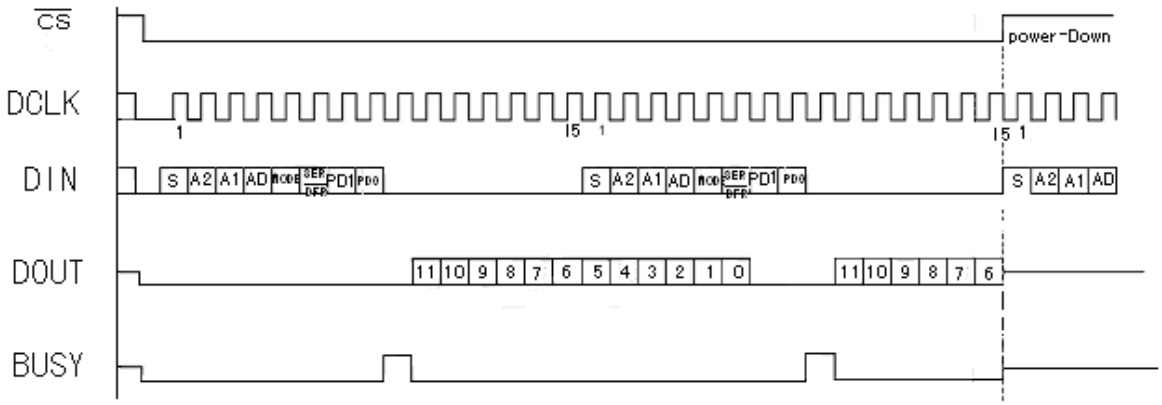


Figure 11. Maximum Conversion Rate, 15 Clocks-per-Conversion.

Digital Timing

Figures 7 and 10 and Table 6 provide detailed timing for the digital interface of the BL2046.

15 Clocks-per-Conversion

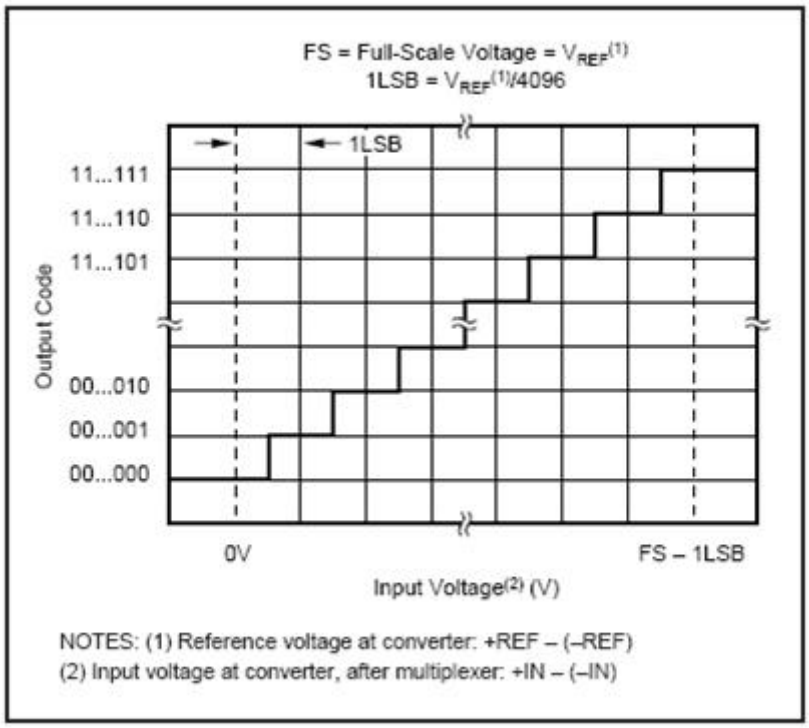


Figure 12. Ideal Input Voltages and Output Codes.

Figure 11 provides the fastest way to clock the BL2046. This method does not work with the serial interface of most microcontrollers and digital signal processors, as they are generally not capable of providing 15 clock cycles per serial transfer. However, this method can be used with field programmable gate arrays (FPGAs) or application specific integrated circuits (ASICs). Note that this effectively increases the maximum conversion rate of the converter beyond the values given in the specification tables, which assume 16 clock cycles per conversion.

Data Format

The BL2046 output data is in Straight Binary format, as shown in Figure 12. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

8-Bit Conversion

The BL2046 provides an 8-bit conversion mode that can be used when faster throughput is needed and the digital result is not as critical. By switching to the 8-bit mode, a conversion is complete four clock cycles earlier. Not only does this shorten each conversion by four bits (25% faster throughput), but each conversion can actually occur at a faster clock rate. This is because the internal settling time of the BL2046 is not as critical—settling to better than 8 bits is all that is needed. The clock rate can be as much as 50% faster. The faster clock rate and fewer clock cycles combine to provide a 2x increase in conversion rate.

Power Dissipation

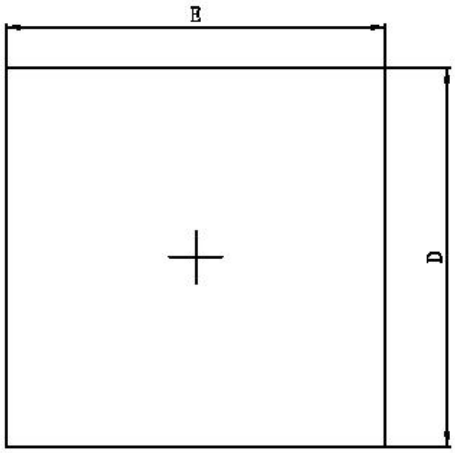
There are two major power modes for the BL2046: full-power (PD0 = 1) and auto power-down (PD0 = 0). When operating at full speed and 16 clocks-per-conversion (see Figure 9), the BL2046 spends most of the time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Therefore, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion but conversions are done less often, the difference between the two modes is dramatic.

$\overline{CS}$ also puts the BL2046 into power-down mode. When $\overline{CS}$ goes high, the BL2046 immediately goes into power-down mode and does not complete the current conversion. The internal reference, however, does not turn off with $\overline{CS}$ going high. To turn the reference off, an additional write is required before $\overline{CS}$ goes high (PD1 = 0).

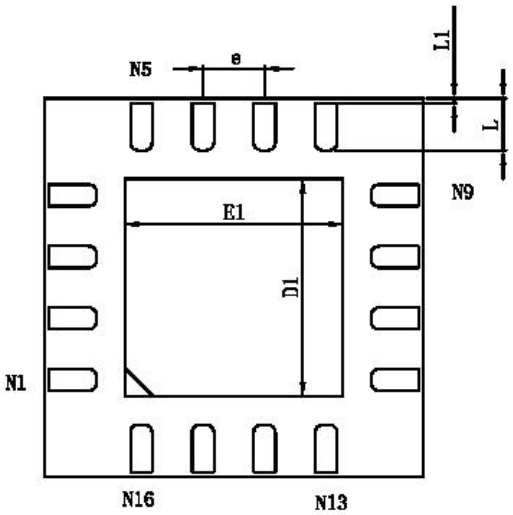
When the BL2046 first powers up, the device draws about 20μA of current until a control byte is written to it with PD0 = 0 to put it into power-down mode. This can be avoided if the BL2046 is powered up with $\overline{CS}$ = 0 and DCLK = IOVDD.

Package Dimensions

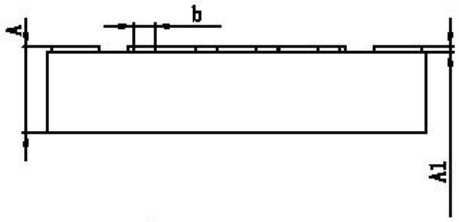
QFN-16



Top View



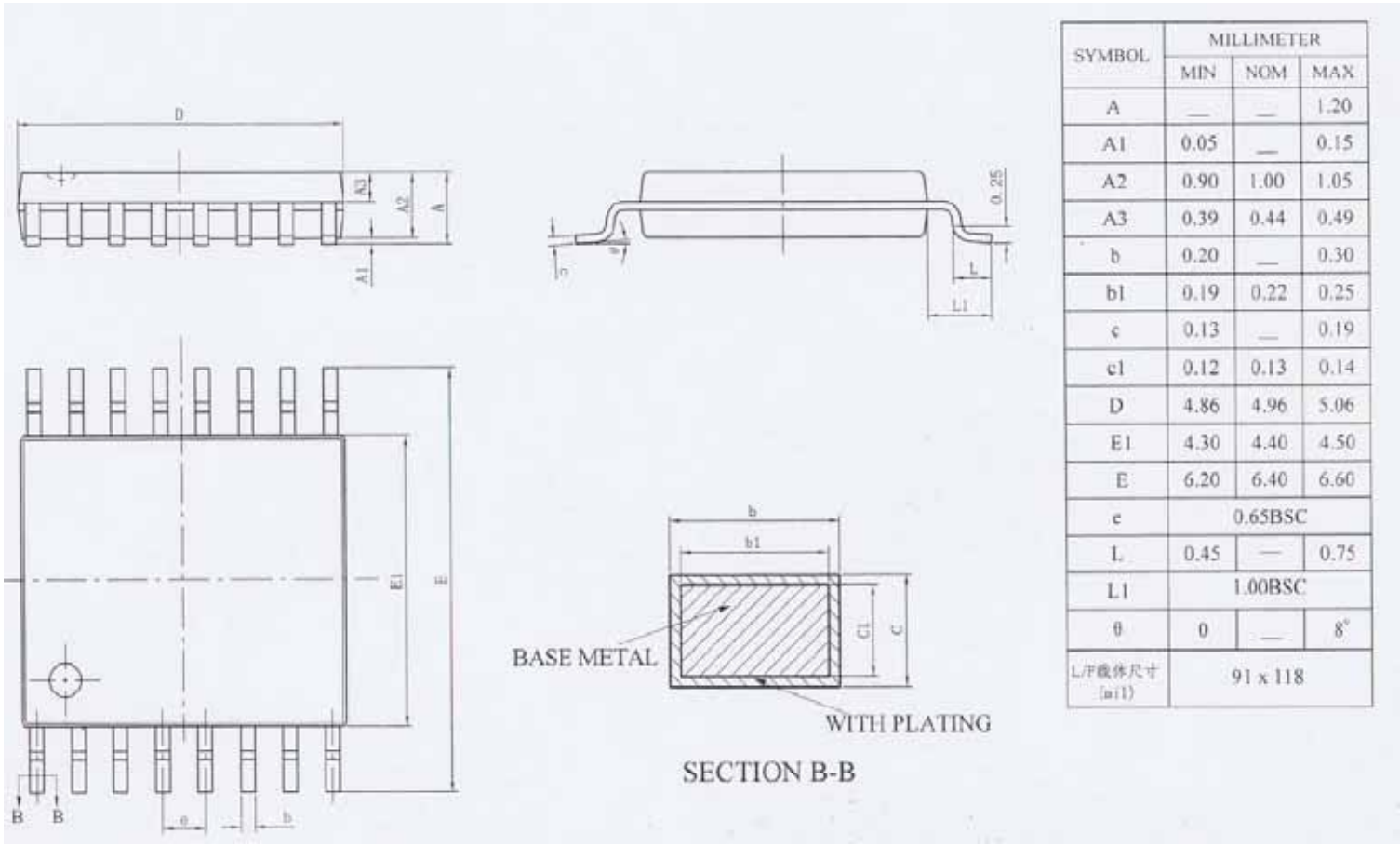
Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	0.900	0.031	0.035
A1	0.010	0.090	0.000	0.004
D	3.900	4.100	0.154	0.161
E	3.900	4.100	0.154	0.161
D1	2.300 REF.		0.091 REF.	
E1	2.300 REF.		0.091 REF.	
b	0.180	0.280	0.007	0.011
e	0.650 BSC.		0.026 BSC.	
L	0.500	0.600	0.020	0.024
L1	0.000	0.050	0.000	0.002

TSSOP-16



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.20	—	0.30
b1	0.19	0.22	0.25
c	0.13	—	0.19
c1	0.12	0.13	0.14
D	4.86	4.96	5.06
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0.45	—	0.75
L1	1.00BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	91 x 118		