General Description

TheBL3085E is a +/- 15kV electrostatic discharge (ESD) protected, high-speed transceiver for RS-485 communication that contain one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic-high even if all transmitters on a terminated bus are disabled. The BL3085E features reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps. All transmitter outputs and receiver inputs are protected to +/- 15kV using the Human Body Model. The transceiver typically draws 500 micron ampere of supply current when unloaded, or when fully loaded with the driver disabled. All devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. The BL3085E is intended for half-duplex communications.

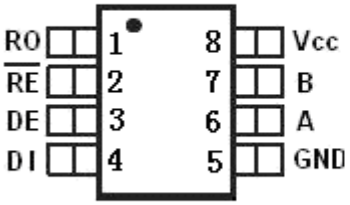
Applications

- RS-485 Communications
- Level Translators
- Transceivers for EMI-Sensitive Applications
- Industrial Control Local Area Networks
- Energy Meter Networks
- Power Inverters
- Building Automation Networks
- Telecommunications Equipment

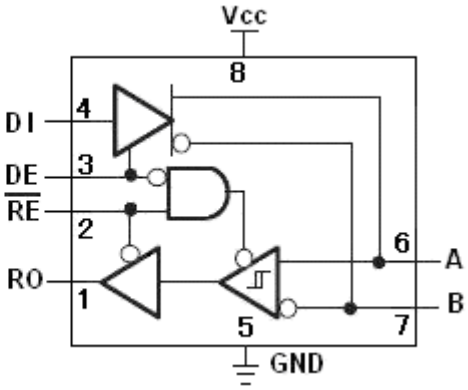
I/O ESD protection

Human Body Model: ±15kV
IEC 61000-4-2：
Contact discharge: ±15kV
Air discharge: ±20kV

PIN Configuration



BL3085E Pin figure



BL3085E logic figure

Ordering Information

PART	TEMP RANGE	PIN PACKAGE
BL3085E	-40℃～+85℃	SOP8

Pin Description

BL3085E PIN	NAME	FUNCTION
1	RO	Receiver Output. When RE is low and if A - B ≧ -50mV, RO will be high; if A - B ≦ -200mV, RO will be low.
2	RE	Receiver Output Enable. Drive RE low to enable RO; RO is high impedance when RE is high. Drive RE high and DE low to enter low-power shutdown mode.
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. These outputs are high impedance when DE is low. Drive RE high and DE low to enter low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces non-inverting output low and inverting output high. Similarly, a high on DI forces non-inverting output high and inverting output low.
5	GND	Ground
6	A	Non-inverting Receiver Input and Non-inverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	VCC	Positive Supply 4.75V ≦ VCC ≦ 5.25V

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	NUM	UNITS
Supply Voltage (VCC)	V_{CC}	+7	V
Control Input Voltage (RE, DE)	/RE, DE	-0.3~V_{CC}+0.3	V
Driver Input Voltage (DI)	DI	-0.3~V_{CC}+0.3	V
Driver Output Voltage (A, B)	A, B	±13	V
Receiver Input Voltage (A, B)	A, B	±13	V
Receiver Output Voltage (RO)	RO	-0.3~V_{CC}+0.3	V
Continuous Power Dissipation	Pd	471	mW
Operating Temperature Ranges	BL3085E	-40～+85	℃
Storage Temperature Range		-65～+150	℃
Lead Temperature (soldering, 10s)		300	℃

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(VCC = +5V ± 5%, TA = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output (No Load)	VOD1	Figure 1				5	V
Differential Driver Output	VOD2	Figure 1, R = 27Ω		1.5			V
Change-in-Magnitude of Differential Output Voltage (Note 2)	ΔVOD	Figure 1, R = 27Ω				0.2	V
Driver Common Mode Output Voltage	VOC	Figure 1, R = 27Ω				3	V
Change-in-Magnitude of Common-Mode Voltage (Note 2)	ΔVOC	Figure 1, R = 27Ω				0.2	V
Input High Voltage	VIH1	DE, DI, RE		2.0			V
Input Low Voltage	VIL1	DE, DI, RE				0.8	V
DI Input Hysteresis	VHYS	BL3085E			100		mV
Input Current (A and B)	IIN1	DE = GND, VCC = GND Or 5.25V	VIN = 12V			125	μA
			VIN = -7V			-75	
Driver Short-Circuit Output Current (Note 3)	I_{OSD}	-7V ≦VOUT ≦VCC		-250			mA
		0V ≦VOUT ≦12V				250	
		0V ≦VOUT≦VCC		±25			
RECEIVER							
Receiver Differential Threshold Voltage	VTH	-7V ≦VCM ≦12V		-200	-120	-50	mV
Receiver Input Hysteresis	ΔVTH				30		mV
Receiver Output High Voltage	VOH	IO = -4mA, VID = -50mV		VCC-1.5			V
Receiver Output Low Voltage	VOL	IO = 4mA, VID = -200mV				0.4	V
Three-State Output Current at Receiver	IOZR	0.4V ≦VO≦2.4V				±1	μA

Receiver Input Resistance	RIN	-7V≦VCM ≦12V		96			kΩ
Receiver Output Short Circuit Current	IOSR	0V ≦VRO ≦VCC		±7		±95	m A
SUPPLY CURRENT							
Supply Current	ICC	No load, RE = DI= GND or VCC	DE = VCC		110	900	μA
			DE = GND		180	600	μA
Supply Current in Shutdown Mode	ISHDN	DE = GND, VRE = VCC			0.001	10	μA
ESD Protection for A, B		Human Body Model			±15		kV

SWITCHING CHARACTERISTICS—BL3085E

(VCC = +5V ± 5%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V and TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t DPLH	Figure 3, RDIFF =54Ω, CL1 = CL2 =100pF	250	720	900	ns
	t DPHL		250	720	900	
Driver Output Skew | t DPLH – t DPHL |	t DSKEW	Figure 3, RDIFF =54Ω CL1 = CL2 =100pF		-3	±100	ns
Driver Rise or Fall Time	t DR, t DF	Figure 3, RDIFF =54Ω ,CL1 = CL2 =100pF	200	530	750	ns
Maximum Data Rate	f MAX				500	Kbps
Driver Enable to Output High	t DZH	Figure 4, CL =100pF, S2 closed			2500	ns
Driver Enable to Output Low	t DZL	Figure 4, CL =100pF, S1 closed			2500	ns
Driver Disable Time from Low	t DLZ	Figure 4, CL = 15pF, S1 closed			100	ns
Driver Disable Time from High	t DHZ	Figure 4, CL = 15pF, S2 closed			100	ns
Receiver Input to Output	t RPLH, t RPHL	Figure 5, | VID |≧2.0V rise and fall time of VID≦15ns		127	200	ns
| t RPLH – t RPHL| Differential Receiver Skew	t RSKD	Figure 5, | VID |≧2.0V rise and fall time of VID≦15ns		3	±30	ns
Receiver Enable to Output Low	t RZL	Figure 2, CL =100pF, S1 closed		20	50	ns
Receiver Enable to Output High	t RHZ	Figure 2, CL =100pF, S2 closed		20	50	ns
Receiver Disable Time from Low	t RLZ	Figure 2, CL =100pF, S1 closed		20	50	ns
Receiver Disable Time from High	t RHZ	Figure 2, CL =100pF, S2 closed		20	50	ns
Time to Shutdown	t SHDN	(Note 4)	50	200	600	ns
Driver Enable from Shutdown-to-Output High	t DZH(SHDN)	Figure 4, CL = 15pF, S2 closed			4500	ns
Driver Enable from Shutdown-to-Output Low	t DZL(SHDN)	Figure 4, CL = 15pF, S1 closed			4500	ns
Receiver Enable	t RZH(SHDN)	Figure 2, CL =100pF,			3500	ns

from Shutdown-to-Output High		S2 closed				
Receiver Enable from Shutdown-to-Output Low	t RZL(SHDN)	Figure 2, CL =100pF, S1 closed			3500	ns

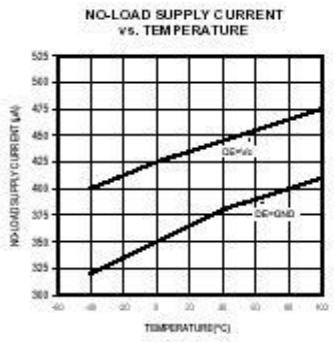
Note 1: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

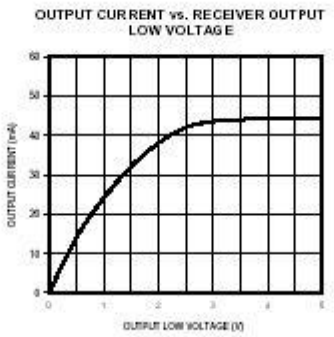
Note 2: ΔVOD and ΔVOC are the changes in VOD and VOC, respectively, when the DI input changes state.

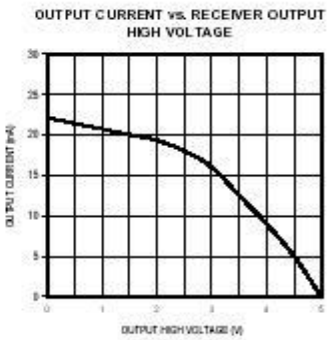
Note 3: Maximum current level applies to peak current just prior to fold-back current limiting; minimum current level applies during current limiting.

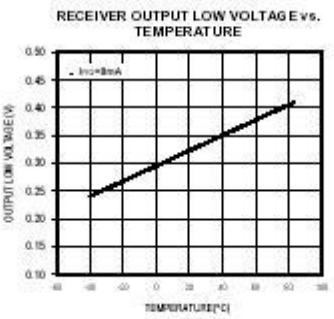
Note 4: The device is put into shutdown by bringing RE high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

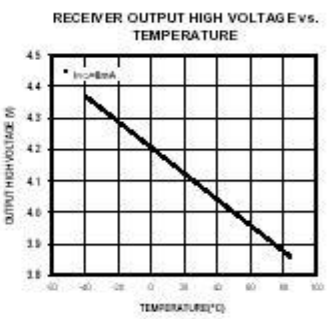
Typical Operating Characteristics

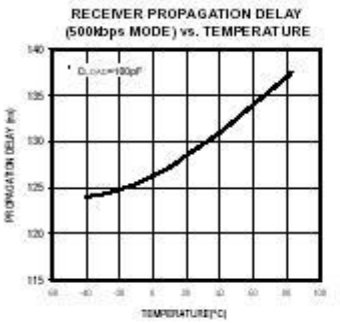


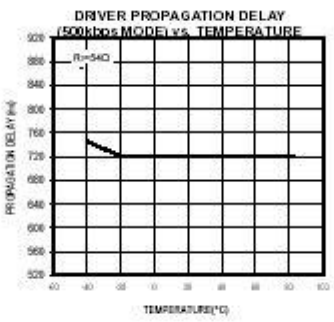


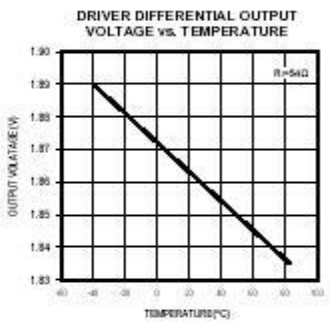












Function Tables

TRANSMITTING				
INPUTS			OUTPUTS	
RE	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

RECEIVING			
INPUTS			OUTPUTS
RE	DE	A - B	RO
0	X	≧-0.05V	1
0	X	≦-0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

X = Don't care
Shutdown mode, driver and receiver outputs high impedance

Test Circuits

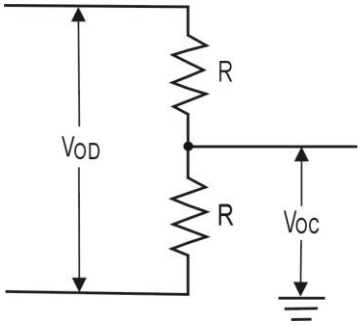


Figure1. Driver DC Test Load

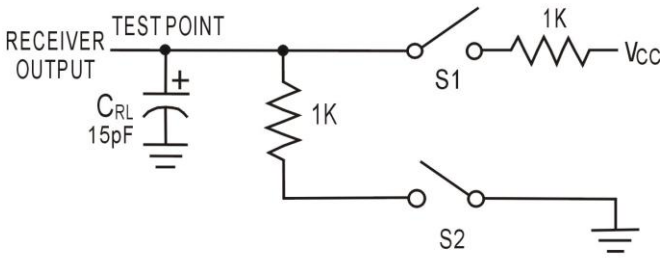


Figure 2. Receiver Enable/Disable Timing Test Load

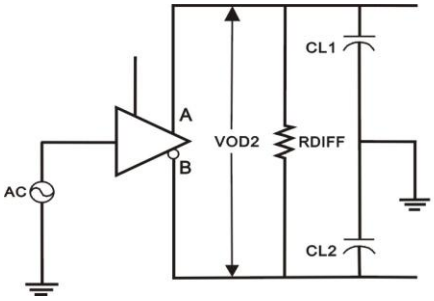


Figure3. Driver Timing Test Load

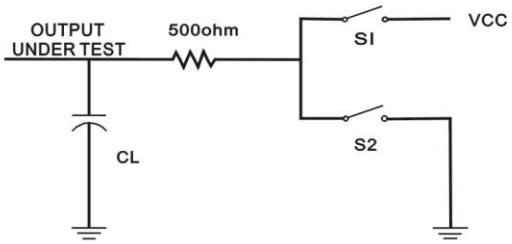


Figure 4. Driver Enable/Disable Timing Test Load

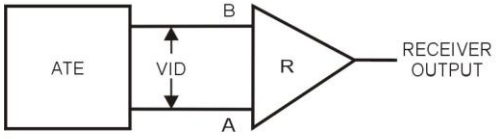


Figure5. Receiver Propagation Delay Test Load

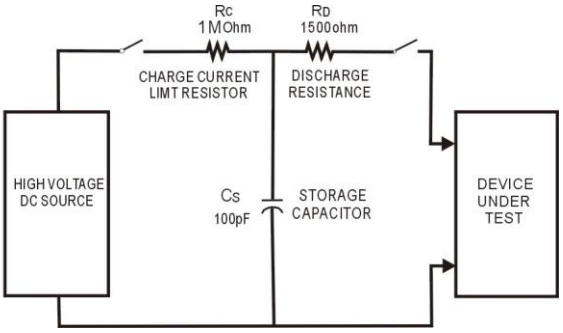


Figure 6. Human Body ESD Test Model

Detailed Description

The BL3085E high - speed transceiver for RS-485 communication contains one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the Fail-Safe section). The BL3085E feature reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 500kbps (see the Reduced EMI and Reflections section). The BL3085E is a half-duplex transceiver. The voltage operates from a single +5V supply. Drivers are output short-circuit current limited. Thermal shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal shutdown circuitry places the driver outputs into a high impedance state.

Receiver Input Filtering

The receiver of the BL3085E, when operating in 500kbps, incorporates input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 25% due to this filtering.

Fail-Safe

The BL3085E guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the input voltage of differential receiver (A-B) is greater than or equal to -50mV, RO is logic high. If A-B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0V by the termination. With the receiver threshold of the BL3085E, this results in a logic high with a 50mV minimum noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the +/−200mV EIA/TIA-485 standard.

ESD Protection

As with BL3085E, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. The driver output and receiver input of theBL3085Ehave extra protection against static electricity. The ESD-protected pins are tested with reference to the ground pin in a powered-down condition. They are tested to +/− 15kV using the Human Body Model.

Power Usage In An RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load as well as to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes, plus the termination resistors at each end of the bus. The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The BL3085E is rated as a 1/8 unit load device. the bus input current is less than 1/8 mA, allowing up to 256 nodes on a single bus. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line. The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 145 ohm resistor at each end, this sums to 25 mA differential output current whenever the bus is active. Typically the BL3085E can drive more than 25 mA to a 60 ohm load, resulting in a differential output voltage higher than the minimum required by the standard. Overall, the total load current can be 60 mA to a loaded RS-485 bus. There is additional current required by the transceiver itself; the BL3085E circuitry requires only about 0.3 mA with both driver and receiver enabled, and below 0.3 mA with either the driver enabled or with the receiver enabled. In low-power shutdown mode, neither the driver nor receiver is active. And the supply current is very low. Supply current increases with signaling rate primarily due to the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting and this creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

Low-Power Shutdown Mode

When both the driver and receiver are disabled (DE low and RE high) the device is in shutdown mode. If the enable inputs are in this state for less than 60 ns, the device does not enter shutdown mode. This guards against inadvertently entering shutdown mode during driver/receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in shutdown mode. In this low-power shutdown mode, most internal circuitry is powered down except over temperature protection circuit, and the supply current is typically 40 micron ampere. When either the driver or the receiver is re-enabled, the internal circuitry becomes active. If only the driver is re-enabled (DE changed to high) the driver outputs are driven according to the DI input after the enable times given by t_{PZH}(SHDN) and t_{PZL} (SHDN) in the driver switching

characteristics. If the DI input is open when the driver is enabled, the driver outputs defaults to A high and B low, in accordance with the driver failsafe feature. If only the receiver is re-enabled (RE changed to low) the receiver output is driven according to the state of the bus inputs (A and B) after the enable time given by t_{PZH}(SHDN) and t_{PZL}(SHDN) in the receiver switching characteristics. If there is no valid state on the bus the receiver responds as described in the failsafe operation section. If both the receiver and driver are re-enabled simultaneously, the receiver output is driven according to the state of the bus inputs (A and B) and the driver output is driven according to the DI input. Note that the state of the active driver affects the inputs to the receiver. Therefore, the receiver outputs are valid as soon as the driver outputs are valid.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a fold back current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range. The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

Layout Consideration

A ground plane is recommended when using a high frequency device like the BL3085E. A 0.1uF ceramic bypass capacitor less than 1/4 inch away from the VDD pin is recommended. Good bypassing is especially needed when operating at maximum frequency or when package to package matching is very important. The PC board traces connected to the A and B outputs must be kept as symmetrical and short as possible to obtain the same parasitic board capacitance. This maintains the good matching characteristics of the low-to-high and high to low transitions of the BL3085E. Note that output A to output B capacitance should also be minimized. If routed adjacent to each other on the same layer, they should be separated by an amount at least as wide as the trace widths. If output A and output B are routed on different signal planes, they should not be routed directly on top of each other. A trace width lateral separation is also recommended. As mentioned before, care should also be taken when routing the DI input. To achieve consistent board-to board propagation delay, the ringing on this signal should be kept below a few hundred millivolts.