LCD Driver for 144 Display Units BL55072A

General Description

The BL55072A is a general LCD driver IC for 144 units LCD panel. It features a wide operating supply voltage range, incorporates simple communication interface with microcomputer and is suitable for multiple application.

Features

- Single-chip LCD controller/driver
- 144(36 SEG x 4 COM) Display Units
- Serial data interface(I2C): SDA, SCL
- Integrated Oscillator circuit
- Integrated LCD Driver Power Supply Circuit
  1/3 or 1/2 Bias, 1/4 Duty
  On Chip Buffer AMP
- Operation voltage: 2.5~5.5V
- No External Componet
- Low Power Consumption Design
- Versatile blinking modes
- Excellent EMC immunity
- Compatible with general microcomputer
- TSSOP48 package

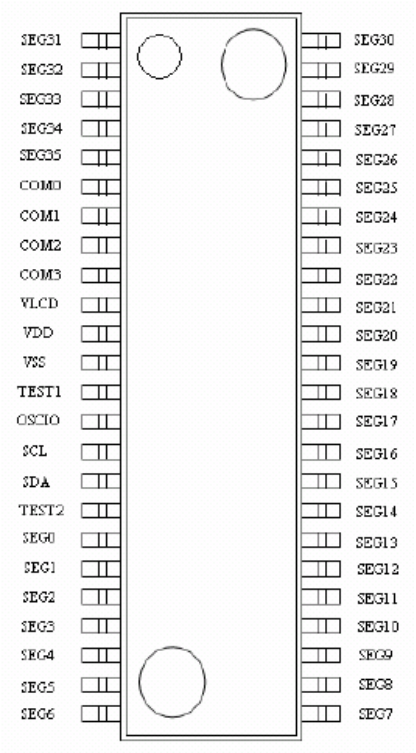
Application

Power Meter, Gas Meter…
Toy, Clock
Industrial instrument

Pin Description

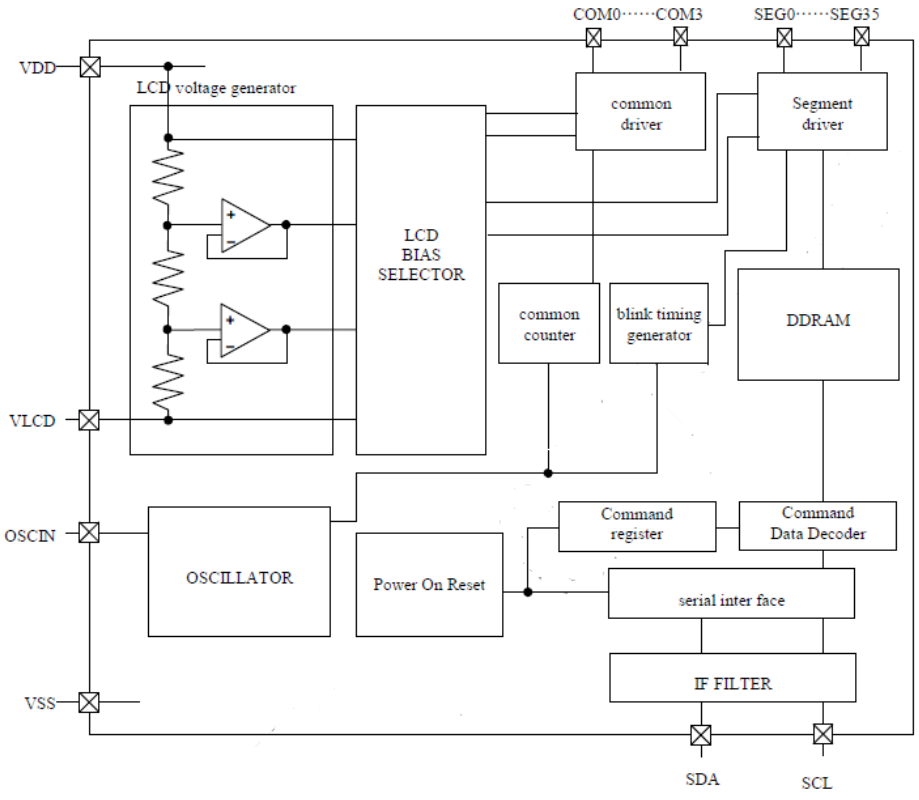
Pin No.	SYMBOL	DESCRIPTION
16	SDA	Serial data input/output
15	SCL	Serial clock input
11	VDD	Supply voltage
10	VLCD	Power supply for LCD driving circuit
12	VSS	GND
1-5，18-48	SEG0-35	Segment output
6-9	COM0-3	Common output
13	TEST1	Input Pin for internal test, connect to VSS
14	OSCIO	External clock input, Must be connected to VSS when use internal oscillation circuit
17	NC	Connect to VDD/GND or Open

Pin Assignment



TSSOP48

Block Diagram



Function Description

Function Circuit

The BL55072A has all function circuits that can directly drive LCD containing up to four commons and up to 36 segments. The function circuits include: Power-on reset, LCD bias generator, Oscillator, display RAM, Common/segment outputs, Blinker, etc.

Display Function Decription

The display RAM is a static 36x 4-bit RAM which stores LCD data. A logic 1 in the RAM bit-map indicates the on state of the corresponding LCD segment; similarly, a logic 0 indicates the off state. There is a one-to-one correspondence between the RAM addresses and the segment outputs, and between the individual bits of a RAM byte and the common outputs.

		Com0	Com1	Com2	Com3
00h	Seg0	a	b	c	d
01h	Seg1	e	f	g	h
02h	Seg2	i	j	k	l
03h	Seg3	m	n	o	p
…	…	…			
22h	Seg35				
23h	Seg36				

When display data is transmitted to the BL55072A, the display bytes received are stored in the display RAM in accordance with the selected LCD drive mode.

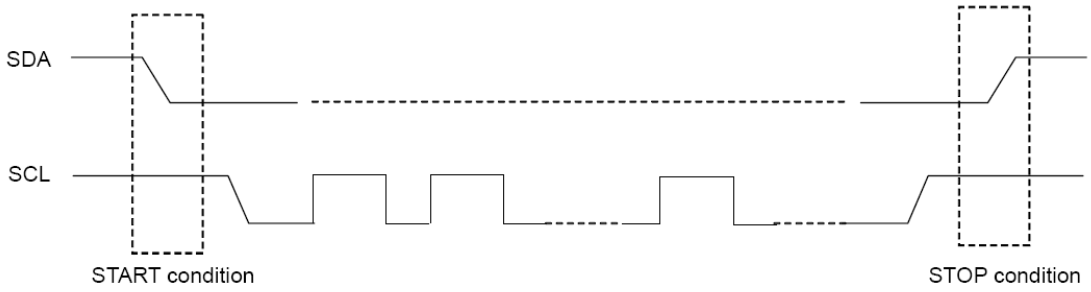
I^2C-bus protocol

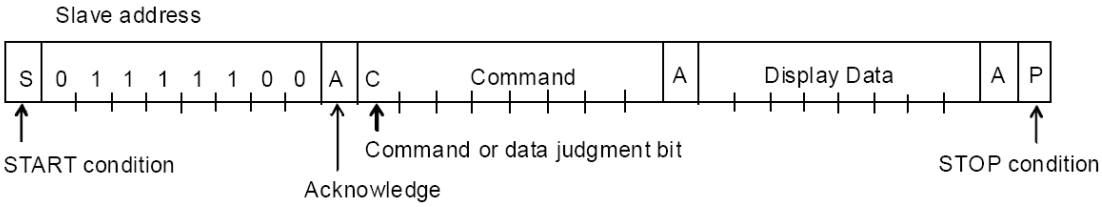
Two I2C-bus slave addresses (01111100) are reserved for the BL55072A. . The sequence is initiated with a START condition (S) from the I2C-bus master which is followed by BL55072A slave address. After acknowledgement, one or more command bytes (m) follow. The MSB (Command or Data judgment bit) define if the succeeding byte is a command or data.

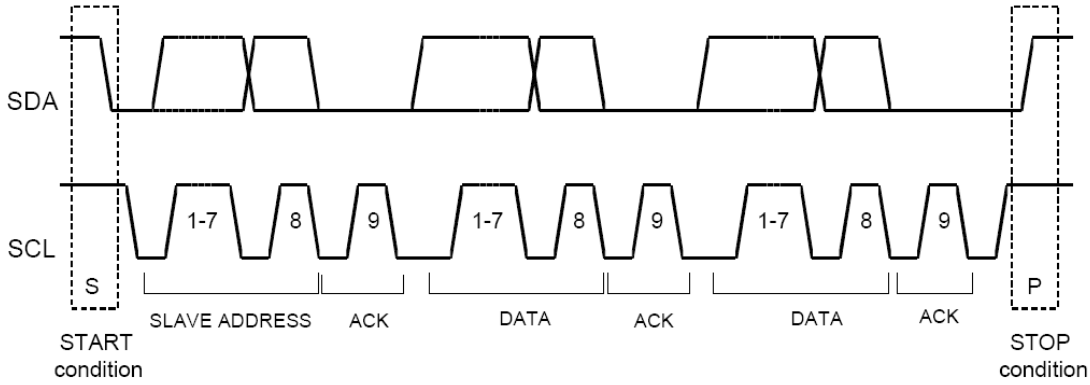
When C (Command or Data judgment bit) =1, the next byte is a command.

When C (Command or Data judgment bit) =0, the next byte is display data.

After the last command byte, a series of display data bytes (n) may follow. These display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended BL55072A device. After the last display byte, the I2C-bus master issues a STOP condition (P).







Command Decoder

The command decoder identifies command bytes that arrive on the I²C-bus. All available commands carry a continuation bit C in their most significant bit position. The six commands available to the BL55072A are defined.

	Command	Function
1	**MODESET**	Display ON/OFF, 1/2 or 1/3 bias
2	**ADSET**	Address[4:0] set DRAM address （00h to 23h） REG address （24h to 25h）
3	**DISCTL**	Frame frequency, Drive Mode control, power save mode
4	**ICSET**	Address[5] set software reset, internal/external clock
5	**BLKCTL**	Blink OFF/0.5s/1s/2s/3s/5s blink
6	**APCTL**	All pixels ON/OFF during Display ON

MODESET——mode set

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	0	*	display	bias	*	*

default	C	1	0	*	0	0	*	*

[3]：Display on and off
0 – Display off （default）
1 – Display on

[2]：Bias control
0 – 1/3 bias （default）
1 – 1/2 bias

ADSET——address set

	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Value	C	0	0	addr[4：0]				
default	C	0	0	0	0	0	0	0

bit[4：0] set address[4：0]；and ICSET bit2 set address[5]
In write mode, the range of address is 0_00000 ~ 1_00011，otherwise address will be set 0_00000；
In read mode, the range of address is 0_00000 ~ 1_00101，otherwise address will be set 0_00000；

ICSET[2]_ADSET[4:0]	Write	Read
0_00000 ~ 1_00011	New address	
1_00100 ~ 1_00101	Last address	New address
1_00110 ~ 1_11111	0_00000	

DISCTL——display control

	Bit7	**Bit6**	**Bit5**	**Bit4**	**Bit3**	**Bit2**	**Bit1**	**Bit0**
Value	C	0	1	FR[1：0]		DM	SR[1：0]	
default	C	1	1	0	0	0	1	0

[4：3]：frame frequency control （FR）
00 - 80Hz （default）
01 - 71Hz
10 - 64Hz
11 - 53Hz

[2]：LCD Drive Mode control（DM）
0 – Line inversion mode （default）
1 – Frame inversion mode

[1：0]：power save mode control （SR）
00 – power save mode 1
01 – power save mode 2
10 – normal mode （default）
11 – high power mode

ICSET——set IC operation

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	0	1	addr[5]	softrst	oscmode
Default	C	1	1	0	1	0	0	0

[2]：Addr[5]

See **ADSET command**

[1]：software reset

0 – no operation （default）

1 – software reset

[0]：oscillator mode control

0 – inner oscillator （default） ： OSCIN pin connected to VSS pin.

1 – outside oscillator ： OSCIN pin connected to outside clock signal.

BLKCTL——blink control

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	1	0	blk[2：0]		
Default	C	1	1	1	0	0	0	0

[2：0]： blinking control

000 – blinking off

001 – 0.5 Hz

010 – 1 Hz

011 – 2 Hz

100 – 0.3 Hz

101 – 0.2 Hz

APCTL——all pixel control

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Value	C	1	1	1	1	1	Apon	Apoff
Default	C	1	1	1	1	1	0	0

[1]：all pixel ON control

0 – normal （default）

1 – all pixel on

[0]：all pixel OFF control

0 – normal （default）

1 – all pixel off

Note that all pixel ON/OFF is effective only at “Display ON” state.

“all pixel OFF” is prior to “all pixel ON”. When both of Apon and Apoff are set to 1, “all pixel OFF” is available.

5. Write data command

ID	ICSET ad[5]	ADSET ad[4:0]	Data	Data	…
01111100	11101000	00000000	xxxxxxxx	xxxxxxxx	…

6. Read data command

ID	ICSET ad[5]	ADSET ad[4:0]	ID	Data	Data
01111100	11101000	10000000	01111101		

7. Read command register

ID	ICSET ad[5]	ADSET ad[4:0]	ID	Data	description
01111100	1110110	10000100	01111101		Read 24h
01111100	1110110	10000101	01111101		Read 25h

24h：
[7：6]：**
[5]：Bias control setting
[4]：oscillator mode control setting
[3]：software reset setting
[2：0]： blinking control setting

25h：
[7：6]：frame frequency control （FR）setting
[5：4]：power save mode control （SR）setting
[3]：LCD Drive Mode control（DM）setting
[2]：Display on and off setting
[1]：all pixel ON control setting
[0]：all pixel OFF control setting

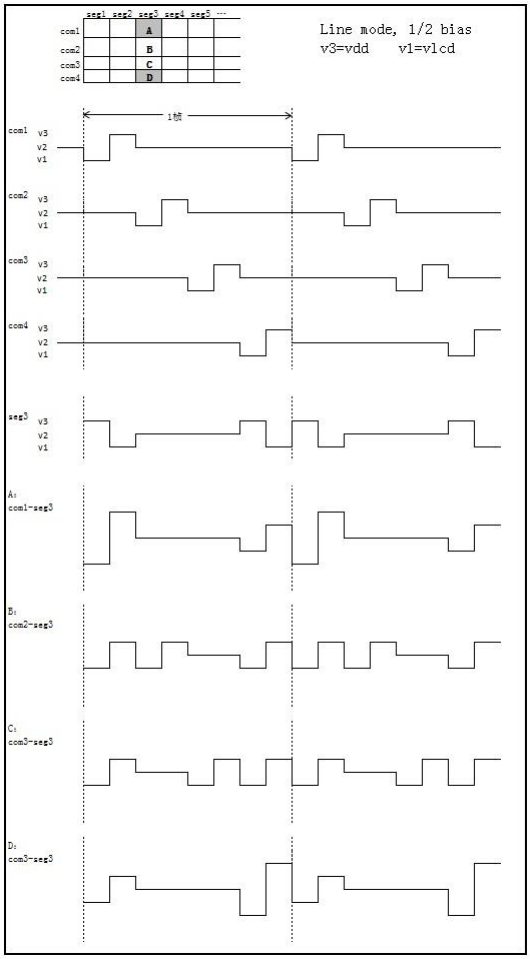
Example of BL55072A Start Sequence

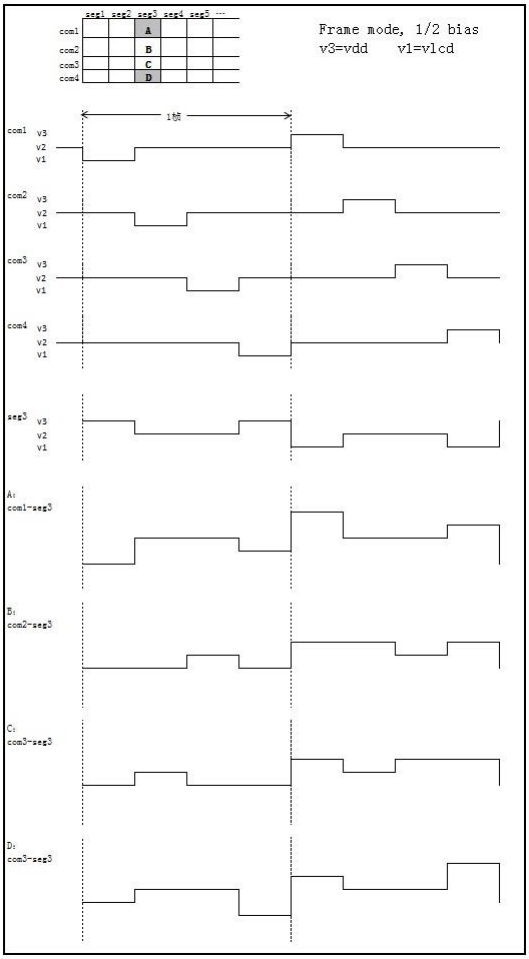
No.	Input	D7	D6	D5	D4	D3	D2	D1	D0	Descriptions
1	Power on									VDD=0→5 V (Tr=100us)
	↓									
2	Wait 100us									IC initialization
	↓									
3	Stop									Stop condition
	↓									
4	Start									Start condition
	↓									
5	Slave address	0	1	1	1	1	1	0	0	Issule slave address
	↓									
6	ICSET	1	1	1	0	1	*	1	0	Software reset
	↓									
7	BLKCTL	1	1	1	1	0	*	0	0	Unnecessary when initial setup
	↓									(if you need to change the condition)
8	DISCTL	1	0	1	0	0	0	1	0	Unnecessary when initial setup
	↓									(if you need to change the condition)
9	ICSET	1	1	1	0	1	*	0	1	RAM address MSB set
	↓									
10	ADSET	0	0	0	0	0	0	0	0	RAM address set
	↓									
11	Display data	*	*	*	*	*	*	*	*	Address 00h - 01h
	Display data	*	*	*	*	*	*	*	*	Address 02h - 03h
	. . .									
	Display data	*	*	*	*	*	*	*	*	Address 22h - 23h
	↓									
12	Stop									Stop condition
	↓									
13	Start									Start condition
	↓									
14	Slave address	0	1	1	1	1	1	0	0	Issule slave address
	↓									
15	MODESET	1	1	0	*	1	0	*	*	Display on
	↓									
16	Stop									Stop condition

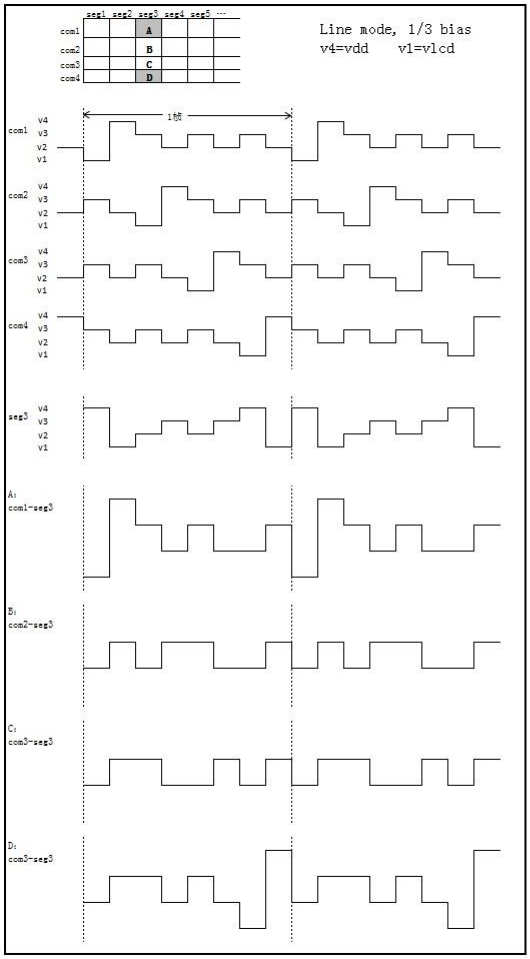
	data	description
initial		
Power On		
Wait 100us		
STOP		
START		
Slave address	0 1 1 1 1 1 0 0	7C
APCTL	1 1 1 1 1 1 1 1	Set all pixels off
MODESET	1 1 0 0 1 0 0 0	Set display on
ICSET	1 1 1 0 1 0 1 0	Software reset
DISCT	1 0 1 1 0 1 1 0	Set power save mode
ICSET	1 1 1 0 1 0 0 0	Set msb of ram address
ADSET	0 0 0 0 0 0 0 0	Set ram address
Display Data	* * * * * * * *	
…		
STOP		
Display ON		
START		
Slave address	0 1 1 1 1 1 0 0	7C
DISCT	1 0 1 1 0 1 1 0	Set power save mode
BLKCTL	1 1 1 1 0 0 0 0	Set blink
APCTL	1 1 1 1 1 1 0 0	Close all pixels on/off function
MODESET	1 1 0 0 1 0 0 0	Set display on
STOP		
Write data		
START		
Slave address	0 1 1 1 1 1 0 0	7C
DISCT	1 0 1 1 0 1 1 0	Set power save mode
BLKCTL	1 1 1 1 0 0 0 0	Set blink
APCTL	1 1 1 1 1 1 0 0	Close all pixels on/off function
MODESET	1 1 0 0 1 0 0 0	Set display on
ICSET	1 1 1 0 1 0 0 0	Set msb of ram address
ADSET	0 0 0 0 0 0 0 0	Set ram address
Display Data	* * * * * * * *	
…		
STOP		
Display OFF		

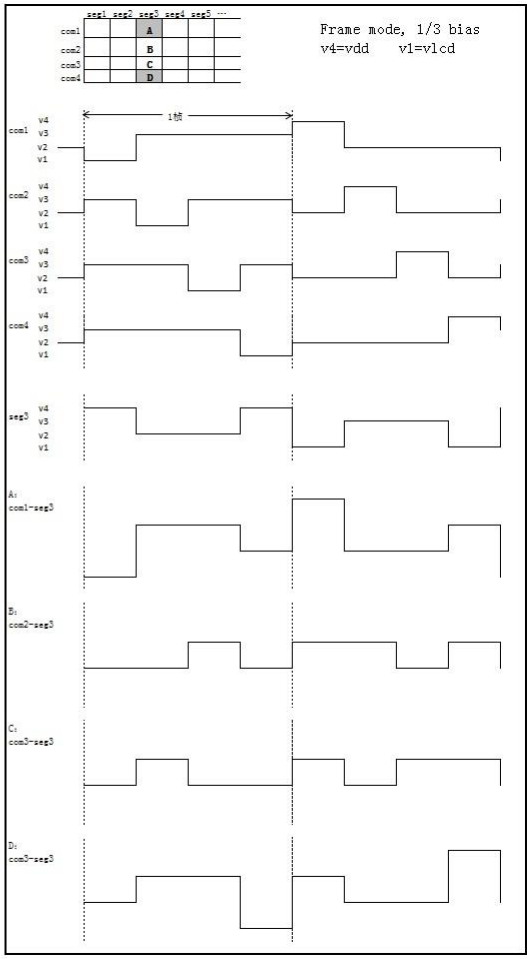
START		
Slave address	0 1 1 1 1 1 0 0	7C
MODESET	1 1 0 0 0 0 0 0	Set display off
STOP		

LCD驱动波形图







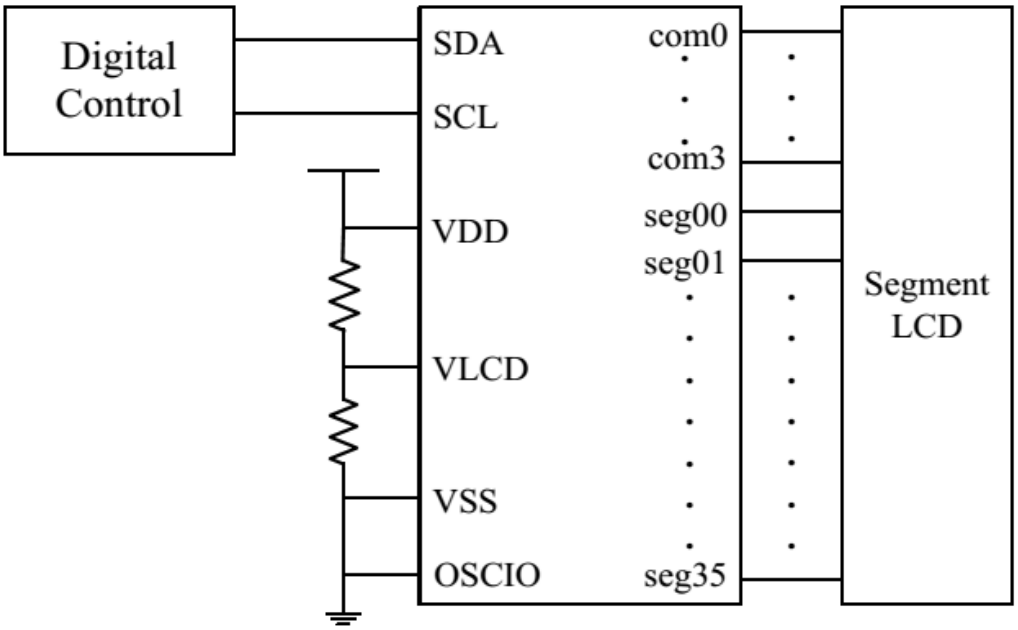


Electrical Characteristic(VDD=2.5V~5.5V，VSS=0，Ta=-40~85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
VDD	IC Operating voltage		2.5	-	5.5	V
Vlcd	LCD operating voltage		0	-	VDD-2.4	V
I_{sl}	Sleep current	Vdd=5V,VLCD=0V, display off, oscillation off	-	0.5	5	uA
IDD	Operating current	VDD=3.3V,T=25℃,Power save mode1，1/3bias，Frame inverse		7.5	20	uA
FCLK	Frame frequency	VDD=3.3V, FR=80Hz	56	80	104	Hz
V_C	DC voltage component	C_{COM}=32nF, COM0~COM3	-20		20	mV
V_S	DC voltage component	C_S=4.7nF, SEG0~SEG35	-20		20	mV

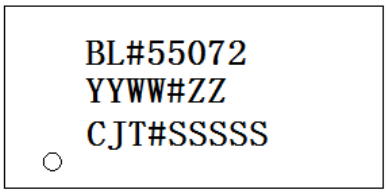
NOTE: the voltage of DC voltage component test: VDD=3.3 V, VLCD=0V

Typical Application



Package Outlines

Marking Number

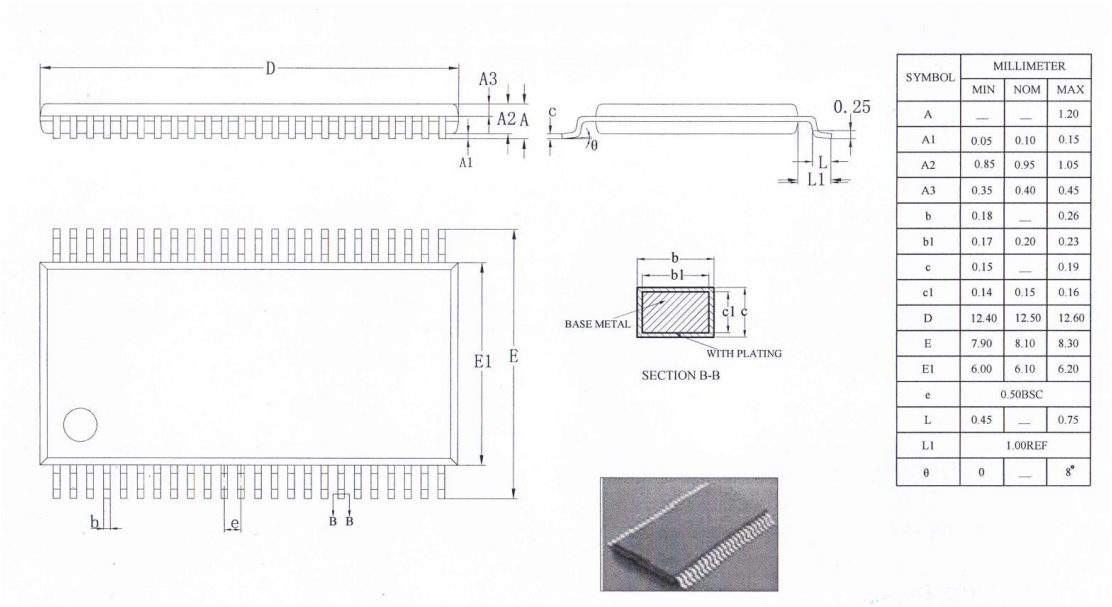


"#" Space
"YY" production year code
"WW" production week code
"ZZ" production factory code
"SSSSS" LOT Number

Order Information

BL55072-*X* ***X=R:reel***
X=T:tube

TSSOP48



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	0.10	0.15
A2	0.85	0.95	1.05
A3	0.35	0.40	0.45
b	0.18	—	0.26
b1	0.17	0.20	0.23
c	0.15	—	0.19
c1	0.14	0.15	0.16
D	12.40	12.50	12.60
E	7.90	8.10	8.30
E1	6.00	6.10	6.20
e	0.50BSC		
L	0.45	—	0.75
L1	1.00REF		
θ	0	—	8°

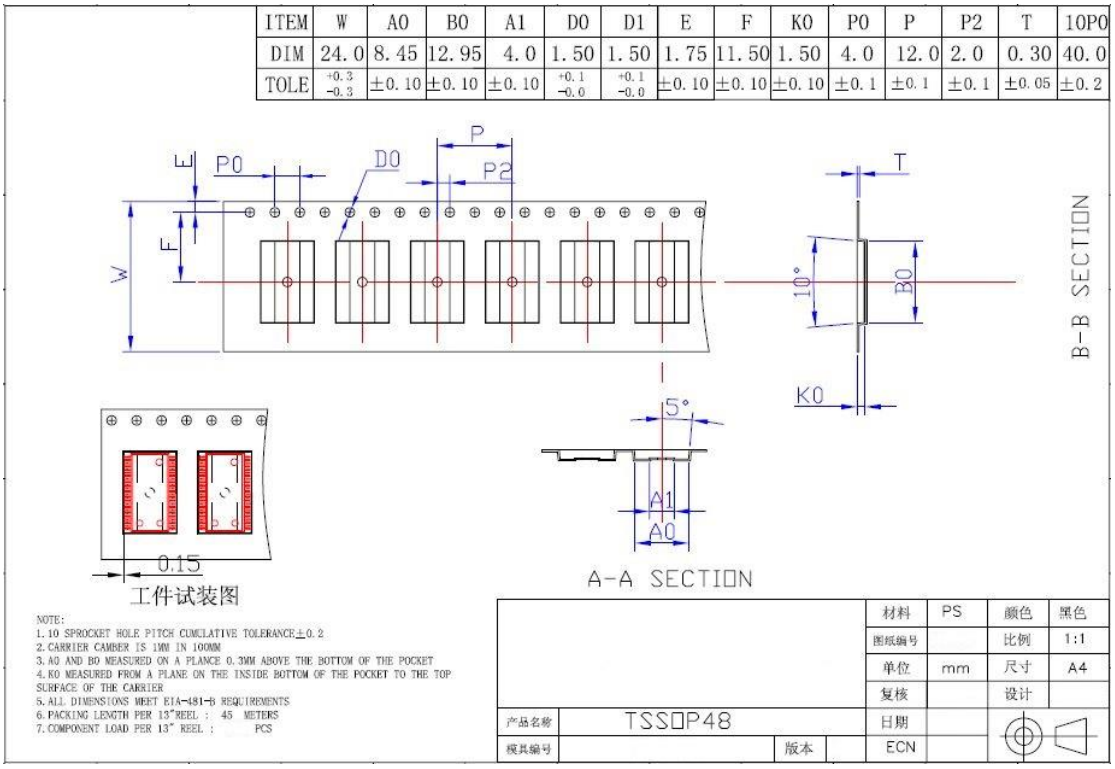
Storage conditions and Packing style

Moisture Sensitivity Level: MSL 3

Storage Period: 2 years

Packing style: Tape Reel

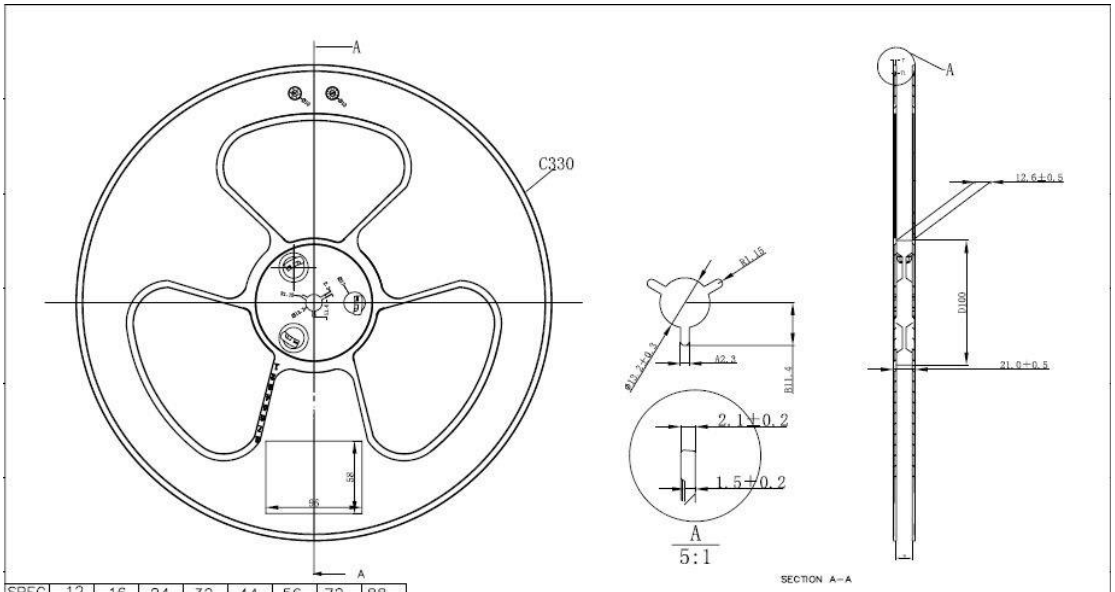
Quantity: 2000pcs



ITEM	W	A0	B0	A1	D0	D1	E	F	K0	P0	P	P2	T	10P0
DIM	24.0	8.45	12.95	4.0	1.50	1.50	1.75	11.50	1.50	4.0	12.0	2.0	0.30	40.0
TOLE	+0.3 −0.3	±0.10	±0.10	±0.10	+0.1 −0.0	+0.1 −0.0	±0.10	±0.10	±0.10	±0.1	±0.1	±0.1	±0.05	±0.2

NOTE:
1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE±0.2
2. CARRIER CAMBER IS 1MM IN 100MM
3. A0 AND B0 MEASURED ON A PLANCE 0.3MM ABOVE THE BOTTOM OF THE POCKET
4. K0 MEASURED FROM A PLANE ON THE INSIDE BOTTOM OF THE POCKET TO THE TOP SURFACE OF THE CARRIER
5. ALL DIMENSIONS MEET EIA-481-B REQUIREMENTS
6. PACKING LENGTH PER 13"REEL : 45 METERS
7. COMPONENT LOAD PER 13" REEL : PCS

		材料	PS	颜色	黑色
		图纸编号		比例	1:1
		单位	mm	尺寸	A4
		复核		设计	
产品名称	TSSOP48	日期			
模具编号	版本	ECN			



SPEC	12	16	24	32	44	56	72	88
C±0.2	330	330	330	330	330	330	330	330
T±0.2	2.1	2.1	2.1	2.1	2.1	2.1	2.1	2.1
T1±0.2	1.5	1.5	1.5	1.5	1.5	1.5	1.5	1.5
A±0.2	2.3	2.3	2.3	2.3	2.3	2.3	2.3	2.3
B±0.2	11.4	11.4	11.4	11.4	11.4	11.4	11.4	11.4
D±0.2	100	100	100	100	100	100	100	100

		材料	PS	颜色	蓝色
		图纸编号		比例	1:1
		单位	mm	尺寸	A4
		复核		设计	
产品名称	13"胶盘	日期			
模具编号	版本	ECN			