

## 2.6 Watt Mono Filter-Free Class-D Audio Power Amplifier

### Features

- Efficiency With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- 2.1mA Quiescent Current
- 0.4μA Shutdown Current
- Optimized PWM Output Stage Eliminates LC Output Filter
- Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor
- Improved PSRR (−75 dB) and Wide Supply Voltage (2.5 V to 5.5 V) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- MSOP8, SOP8, DFN8 package

### General Description

The BL6305 is a 2.6W high efficiency filter-free class-D audio power amplifier that requires only three external components.

Features like 88% efficiency, −75dB PSRR, and improved RF-rectification immunity make the BL6305 ideal for cellular handsets. In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the BL6305.

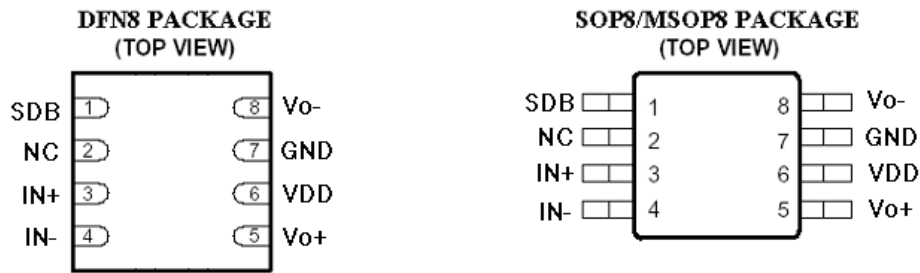
### Applications

- Mobile phone、PDA
- MP3/4、PMP
- Portable electronic devices

### Order Information

| Part Number | Package | Shipping               |
|-------------|---------|------------------------|
| BL6305MM    | MSOP8   | 3000 pcs / Tape & Reel |
| BL6305DN    | DFN8    | 3000 pcs / Tape & Reel |
| BL6305SO    | SOP8    | 2500 pcs / Tape & Reel |

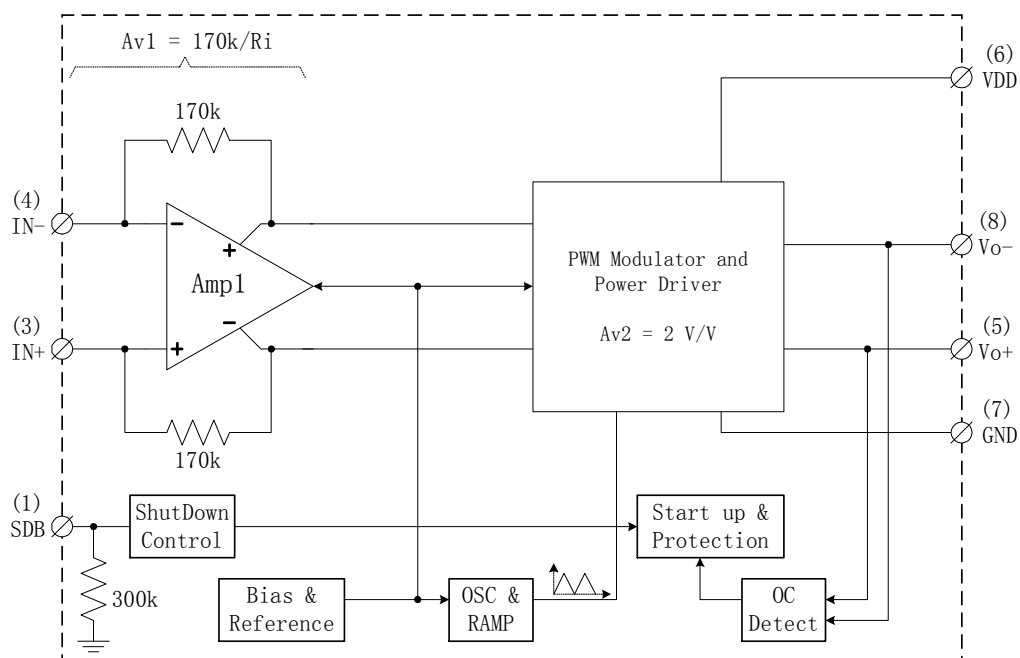
### Pin Diagrams



### Pin Description

| Pin # | Name | Description                    |
|-------|------|--------------------------------|
| 1     | SDB  | Shutdown terminal (low active) |
| 2     |      | NC (No internal connection)    |
| 3     | IN+  | Positive differential input    |
| 4     | IN-  | Negative differential input    |
| 5     | VO+  | Positive BTL output            |
| 6     | VDD  | Power Supply                   |
| 7     | PGND | Power Ground                   |
| 8     | VO-  | Negative BTL output            |

### Function Block Diagram



**Note**

$$s: \text{Total Voltage Gain} = Av1 \times Av2 = 2 \times \frac{170k}{R_i}$$

Figure 1. Function Block Diagram

**Application Circuit**

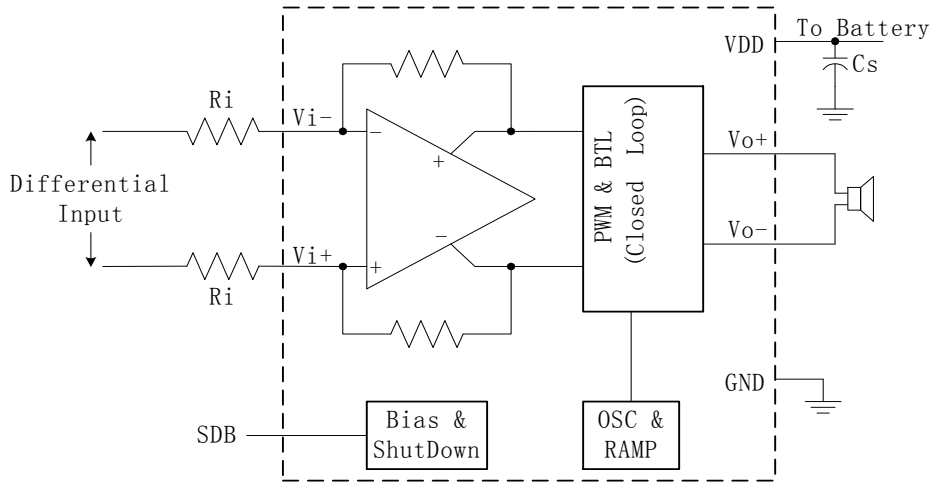


Figure 2. BL6305 Application Schematic With Differential Input

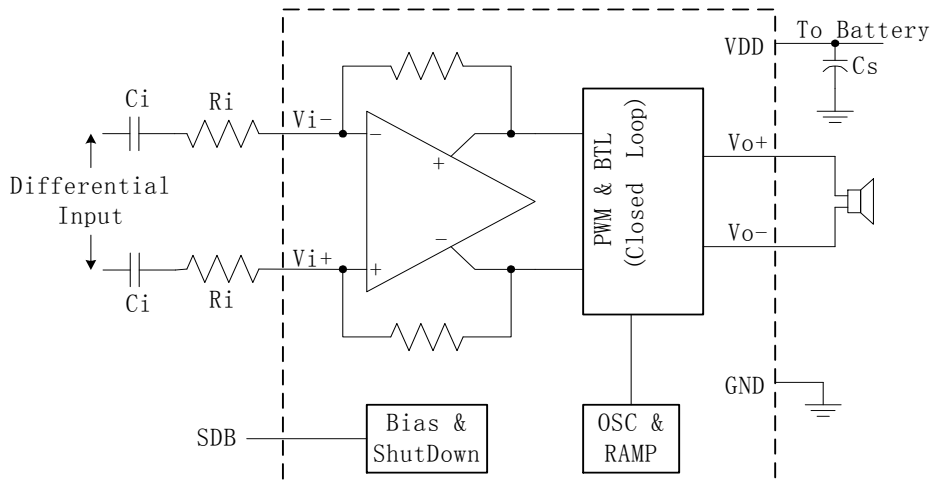


Figure 3. BL6305 Application Schematic With Differential Input and Input Capacitors

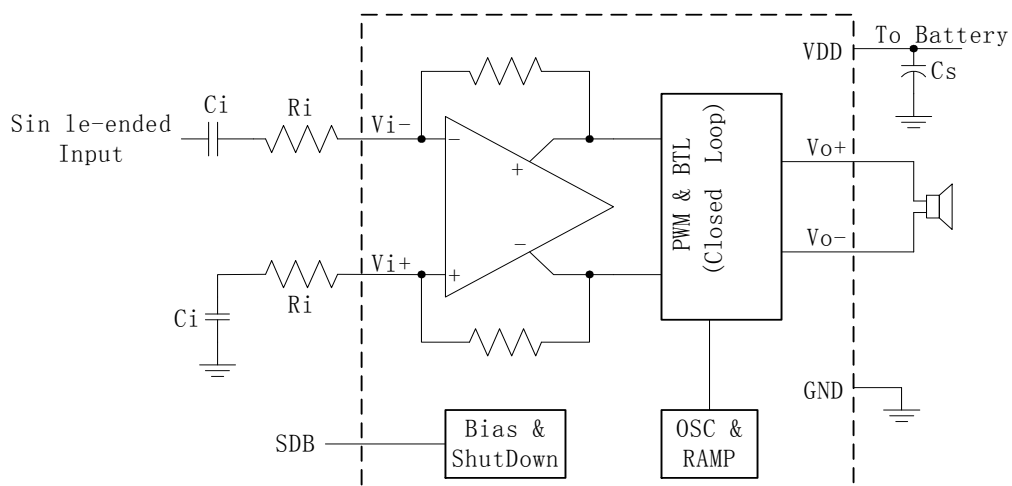


Figure 4. BL6305 Application Schematic With Single-Ended Input

### Electrical Characteristics

The following specifications apply for the circuit shown in Figure 5.

$T_A = 25$  , unless otherwise specified.

| Symbol       | Parameter                          | Conditions  | Spec               |                    |                    | Units      |
|--------------|------------------------------------|---|--------------------|--------------------|--------------------|------------|
|              |                                    |   | Min.               | Typ.               | Max.               |            |
| $I_{SD}$     | Shutdown Current                   | $V_{IN}=0V, V_{SDB}=0V, \text{No Load}$   |                    | 0.4                | 2                  | $\mu A$    |
| $I_Q$        | Quiescent Current                  | $V_{DD} = 2.5V, V_{IN} = 0V, \text{No Load}$  |                    | 1.8                | 3.2                | mA         |
|              |                                    | $V_{DD} = 3.6V, V_{IN} = 0V, \text{No Load}$  |                    | 2.1                |                    |            |
|              |                                    | $V_{DD} = 5.5V, V_{IN} = 0V, \text{No Load}$  |                    | 2.5                | 4.5                |            |
| $ V_{OS} $   | Output Offset Voltage              | $V_{IN} = 0V, A_V = 2V/V,$<br>$V_{DD} = 2.5V \text{ to } 5.5V$  |                    | 2                  | 25                 | mV         |
| PSRR         | Power Supply Rejection Ratio       | $V_{DD} = 2.5V \text{ to } 5.5V$  |                    | -75                |                    | dB         |
| CMRR         | Common Mode Rejection Ratio        | $V_{DD} = 2.5V \text{ to } 5.5V,$<br>$V_{IC} = V_{DD}/2 \text{ to } 0.5V,$<br>$V_{IC} = V_{DD}/2 \text{ to } V_{DD} - 0.8V$ |                    | -68                |                    | dB         |
| $F_{SW}$     | Modulation frequency               | $V_{DD} = 2.5V \text{ to } 5.5V$  | 200                | 250                | 300                | kHz        |
| $A_V$        | Voltage gain                       | $V_{DD} = 2.5V \text{ to } 5.5V$  | $\frac{320k}{R_1}$ | $\frac{340k}{R_1}$ | $\frac{360k}{R_1}$ | V/V        |
| $R_{SDB}$    | Resistance from SDB to GND         |   |                    | 300                |                    | k $\Omega$ |
| $Z_I$        | Input impedance                    |   | 160                | 170                | 180                | k $\Omega$ |
| $T_{WU}$     | Wake-up time from shutdown         | $V_{DD} = 3.6V$   |                    | 1                  |                    | mS         |
| $r_{DS(on)}$ | Drain-Source resistance (on-state) | $V_{DD} = 2.5V$   |                    | 700                |                    | m $\Omega$ |
|              |                                    | $V_{DD} = 3.6V$   |                    | 500                |                    |            |
|              |                                    | $V_{DD} = 5.5V$   |                    | 400                |                    |            |

### Operating Characteristics

□  $V_{DD} = 5V, R_1 = 150k\Omega, T_A = 25$  , unless otherwise specified.

| Symbol | Parameter                         | Conditions                                 | Spec |      |      | Units |
|--------|-----------------------------------|--|------|------|------|-------|
|        |                                   |  | Min. | Typ. | Max. |       |
| $P_O$  | Output Power                      | THD+N=10%, f=1KHz, $R_L = 4\Omega$         |      | 2.65 |      | W     |
|        |                                   | THD+N=1%, f=1KHz, $R_L = 4\Omega$          |      | 2.15 |      |       |
|        |                                   | THD+N=10%, f=1KHz, $R_L = 8\Omega$         |      | 1.65 |      |       |
|        |                                   | THD+N=1%, f=1KHz, $R_L = 8\Omega$          |      | 1.33 |      |       |
| THD+N  | Total Harmonic Distortion + Noise | $P_o=1.0W_{rms}, f=1kHz, R_L = 8\Omega$    |      | 0.21 |      | %     |
| SNR    | Signal-to-Noise ratio             | $V_{DD}=5V, P_o=1.0W_{rms}, R_L = 8\Omega$ |      | 95   |      | dB    |

□  $V_{DD} = 3.6V, R_1 = 150k\Omega, T_A = 25$  , unless otherwise specified.

| Symbol | Parameter    | Conditions                         | Spec |      |      | Units |
|--------|--------------|------------------------------------|------|------|------|-------|
|        |              |                                    | Min. | Typ. | Max. |       |
| $P_O$  | Output Power | THD+N=10%, f=1KHz, $R_L = 4\Omega$ |      | 1.35 |      | W     |
|        |              | THD+N=1%, f=1KHz, $R_L = 4\Omega$  |      | 1.08 |      |       |
|        |              | THD+N=10%, f=1KHz, $R_L = 8\Omega$ |      | 0.85 |      |       |
|        |              | THD+N=1%, f=1KHz, $R_L = 8\Omega$  |      | 0.69 |      |       |

|           |                                   |   |              |      |  |               |
|-----------|-----------------------------------|---|--------------|------|--|---------------|
| THD+N     | Total Harmonic Distortion + Noise | $P_o=0.5W_{rms}$ , $f=1kHz$ , $R_L = 8\Omega$   |              | 0.21 |  | %             |
| $K_{SVR}$ | Supply ripple rejection ratio     | $V_{DD} = 3.6V$ , input ac-grounded with $C_1 = 2\mu F$<br>$f=217Hz$ , $V(Ripple)=200mV_{PP}$ |              | -67  |  | dB            |
| $V_n$     | Output voltage noise              | $V_{DD} = 3.6V$ , input ac-grounded with $C_1 = 2\mu F$ , $f=20\sim 20kHz$                    | No weighting | 87   |  | $\mu V_{RMS}$ |
|           |                                   |   | A weighting  | 65   |  |               |
| CMRR      | Common Mode Rejection Ratio       | $V_{DD} = 3.6V$ , $V_{IC} = 1 V_{PP}$ , $f=217Hz$   |              | -70  |  | dB            |

□  $V_{DD} = 2.5V$ ,  $R_1 = 150k\Omega$ ,  $T_A = 25$  , unless otherwise specified.

| Symbol | Parameter                         | Conditions                                    | Spec |      |      | Units |
|--------|-----------------------------------|---|------|------|------|-------|
|        |                                   |   | Min. | Typ. | Max. |       |
| $P_o$  | Output Power                      | THD+N=10%, $f=1kHz$ , $R_L = 4\Omega$         |      | 0.63 |      | W     |
|        |                                   | THD+N=1%, $f=1kHz$ , $R_L = 4\Omega$          |      | 0.51 |      |       |
|        |                                   | THD+N=10%, $f=1kHz$ , $R_L = 8\Omega$         |      | 0.40 |      |       |
|        |                                   | THD+N=1%, $f=1kHz$ , $R_L = 8\Omega$          |      | 0.33 |      |       |
| THD+N  | Total Harmonic Distortion + Noise | $P_o=0.2W_{rms}$ , $f=1kHz$ , $R_L = 8\Omega$ |      | 0.21 |      | %     |

### Test Circuit

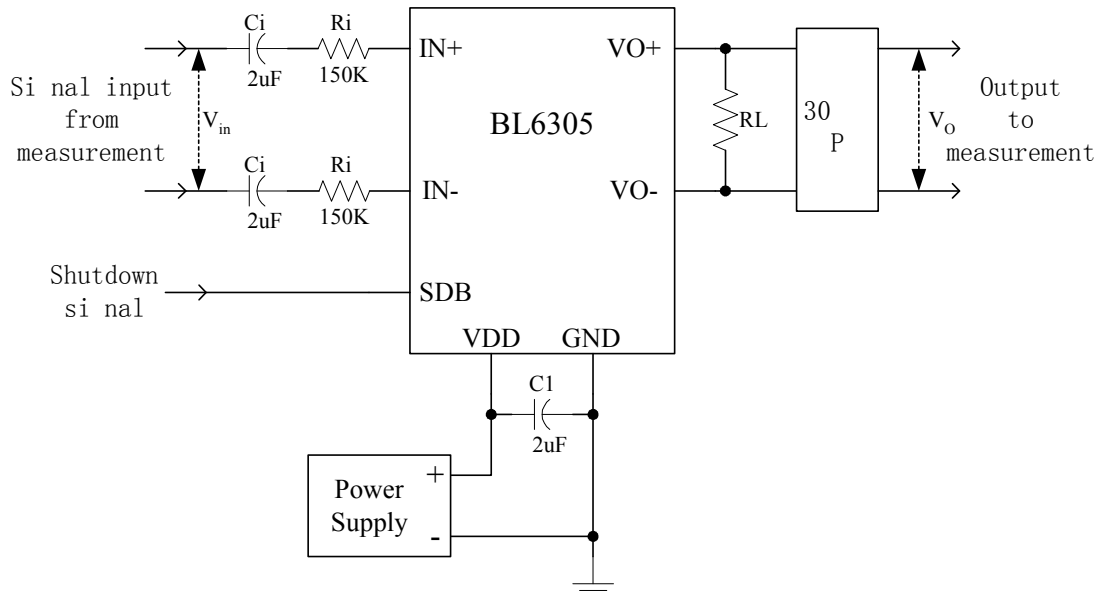


Figure 5. BL6305 test set up circuit

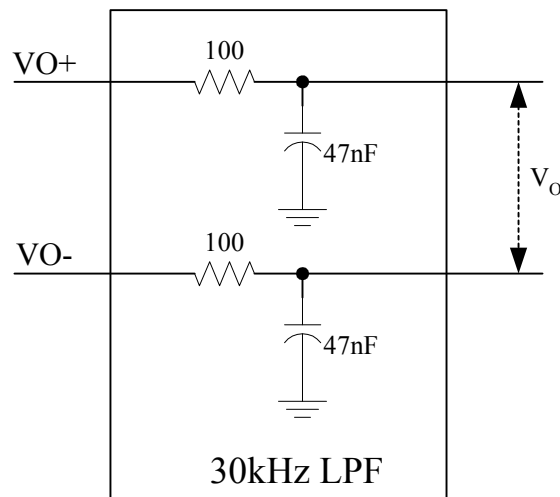


Figure 6. 30-kHz LPF for BL6305 test

- Notes: 1>  $C_S$  should be placed as close as possible to VDD/GND pad of the device  
 2>  $C_I$  should be shorted for any Common-Mode input voltage measurement  
 3> A 33uH inductor should be used in series with  $R_L$  for efficiency measurement  
 4> The 30 kHz LPF (shown in figure 5) is required even if the analyzer has an internal LPF

### **Component Recommended**

Due to the weak noise immunity of the single-ended input application, the differential input application should be used whenever possible. The typical component values are listed in the table:

| $R_I$ | $C_I$  | $C_S$ |
|-------|--------|-------|
| 150 k | 3.3 nF | 2 uF  |

- (1)  $C_I$  should have a tolerance of  $\pm 10\%$  or better to reduce impedance mismatch.  
 (2) Use 1% tolerance resistors or better to keep the performance optimized, and place the  $R_I$  close to the device to limit noise injection on the high-impedance nodes.

### **Input Resistors ( $R_I$ ) & Capacitors ( $C_I$ )**

The input resistors ( $R_I$ ) set the total voltage gain of the amplifier according to Eq1

$$Gain = \frac{2 \times 170k\Omega}{R_I} \left( \frac{V}{V} \right) \quad Eq1$$

The input resistor matching directly affects the CMRR, PSRR, and the second harmonic distortion cancellation.

If a differential signal source is used, and the signal is biased from  $0.5V \sim V_{DD}-0.8V$  (shown in Figure2), the input capacitor ( $C_I$ ) is not required.

If the input signal is not biased within the recommended common-mode input range in differential input application (shown in Figure3), or in a single-ended input application (shown in Figure4), the input coupling capacitors are required.

If the input coupling capacitors are used, the  $R_I$  and  $C_I$  form a high-pass filter (HPF). The corner frequency ( $f_c$ ) of the HPF can be calculated by Eq2

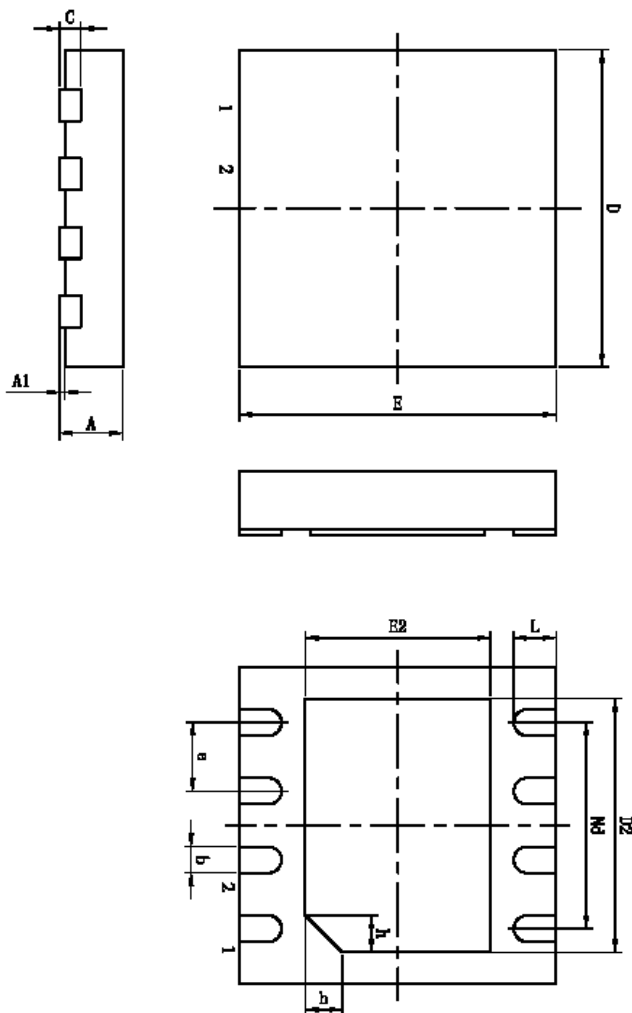
$$f_c = \frac{1}{2\pi \cdot R_I \cdot C_I} \quad (\text{Hz}) \quad \text{Eq2}$$

### Decoupling Capacitor (C<sub>S</sub>)

A good low equivalent-series-resistance (ESR) ceramic capacitor (C<sub>S</sub>), used as power supply decoupling capacitor (C<sub>S</sub>), is required for high power supply rejection (PSRR), high efficiency and low total harmonic distortion (THD). Typically C<sub>S</sub> is 2μF, placed as close as possible to the device VDD pin.

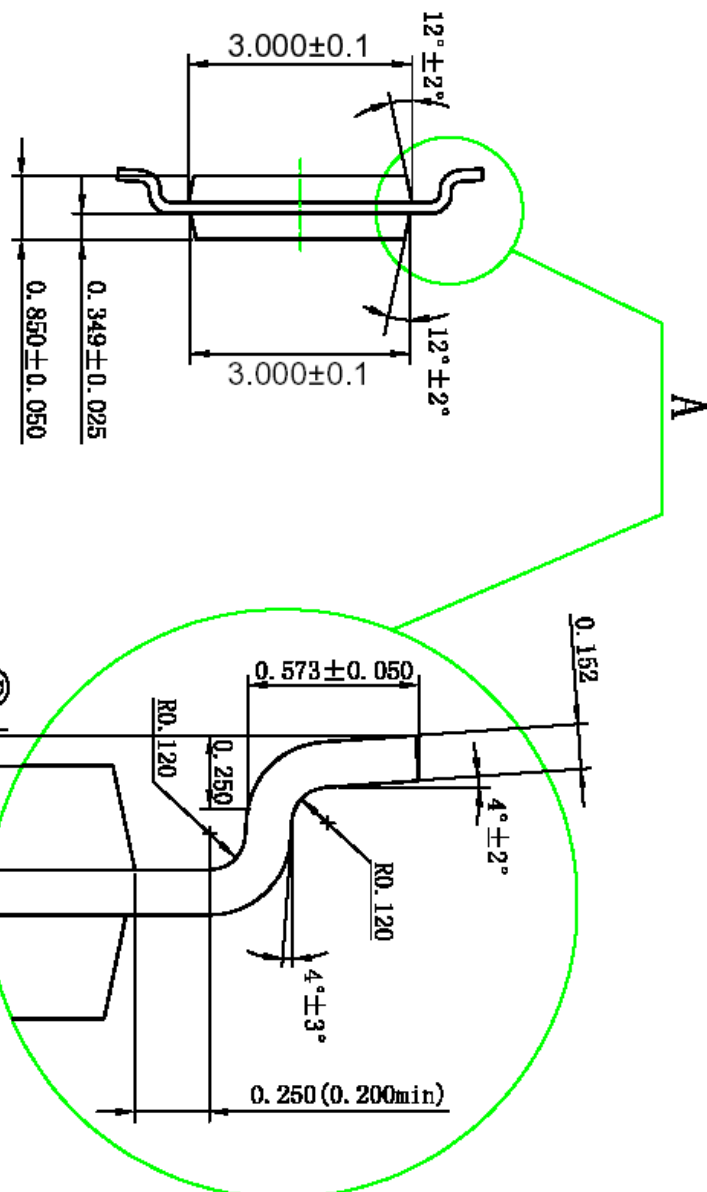
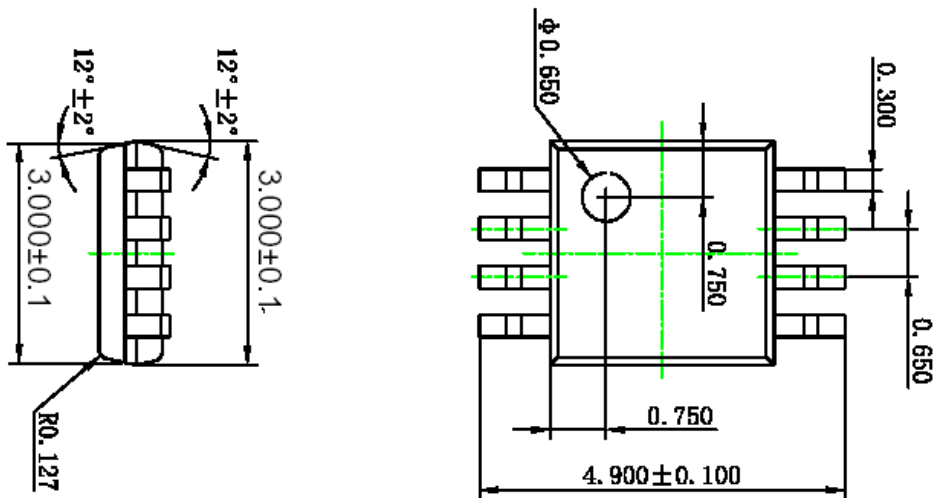
### Package Dimensions

#### DFN8



| SYMBOL | MILLIMETER |      |      |
|--------|------------|------|------|
|        | MIN        | NOM  | MAX  |
| A      | 0.70       | 0.75 | 0.80 |
| A1     | -          | 0.02 | 0.05 |
| b      | 0.25       | 0.30 | 0.35 |
| c      | 0.18       | 0.20 | 0.25 |
| D      | 2.90       | 3.00 | 3.10 |
| D2     | 2.50REF    |      |      |
| e      | 0.65BSC    |      |      |
| Nd     | 1.95BSC    |      |      |
| E      | 2.90       | 3.00 | 3.10 |
| E2     | 1.55REF    |      |      |
| L      | 0.30       | 0.40 | 0.50 |
| h      | 0.20       | 0.25 | 0.30 |

MSOP8



技术要求

1. 成型管脚各引线端相对于基准面B的距离偏差为±0.04 (共面性);
2. 所有尺寸为mm;
3. 视图方向:



SOP8

