

## 3 Watt Mono Filter-Free Class-D Audio Power Amplifier

### Features

- Efficiency With an 8-Ω Speaker:
  - 88% at 400 mW
  - 80% at 100 mW
- 2.6mA Quiescent Current
- 0.4μA Shutdown Current
- Optimized PWM Output Stage Eliminates LC Output Filter
- Internally Generated 250-kHz Switching Frequency Eliminates Capacitor and Resistor
- Improved PSRR (−75 dB) and Wide Supply Voltage (2.8 V to 5.5 V) Eliminates Need for a Voltage Regulator
- Fully Differential Design Reduces RF Rectification and Eliminates Bypass Capacitor
- Improved CMRR Eliminates Two Input Coupling Capacitors
- Available in space-saving package: 9-bump WLCSP

### General Description

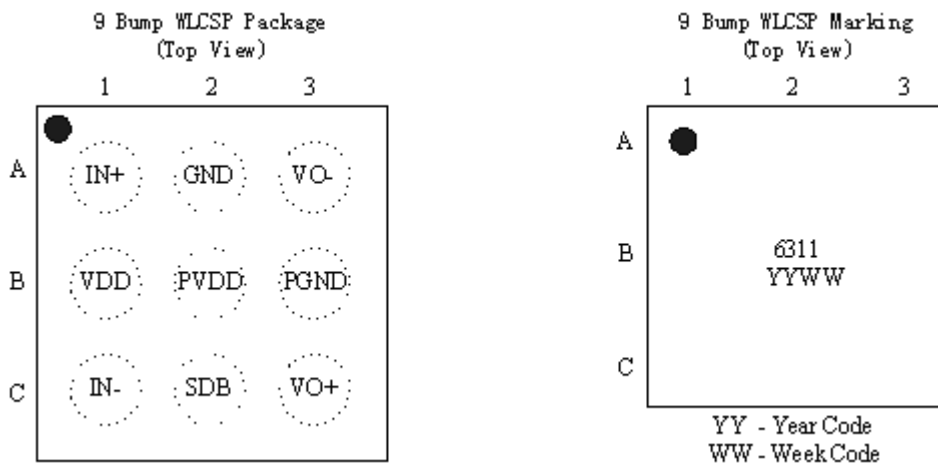
The BL6311B is a 3-W high efficiency filter-free class-D audio power amplifier in a wafer chip scale package (WCSP) that requires only three external components.

Features like 88% efficiency, −75dB PSRR, and improved RF-rectification immunity make the BL6311B ideal for cellular handsets. In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the BL6311B.

### Applications

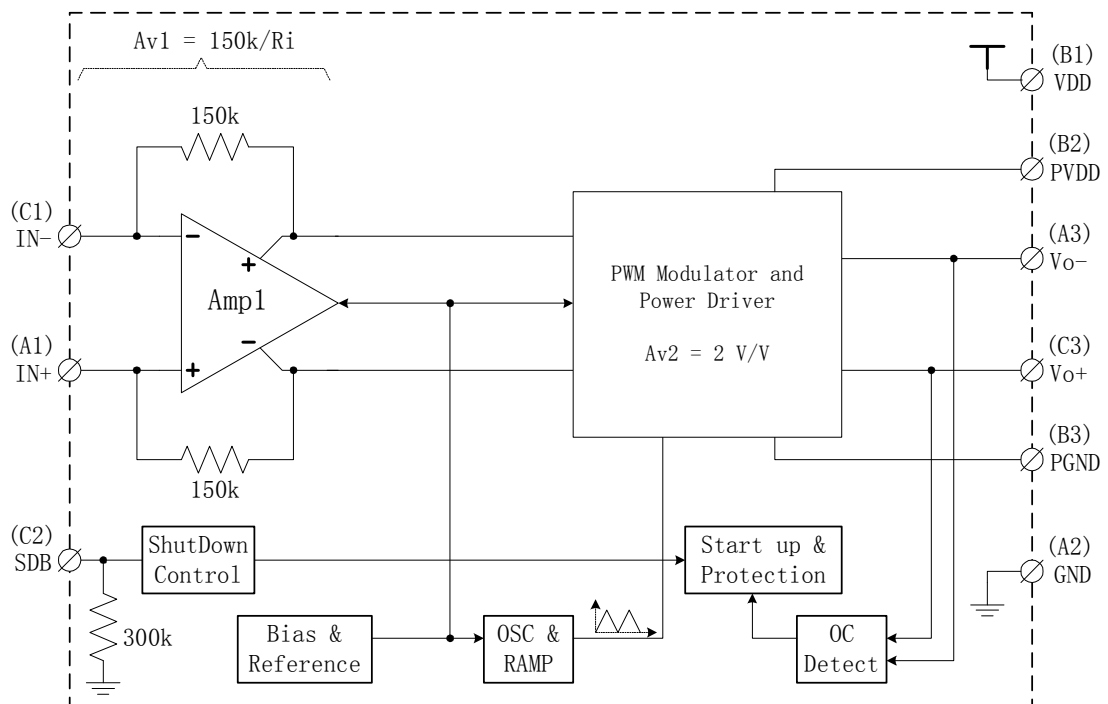
- Mobile phone、PDA
- MP3/4、PMP
- Portable electronic devices

### Pin Diagrams



**Pin Description**

Pin #	Name	Description
A1	IN+	Positive differential input
A2	GND	Power Ground
A3	VO-	Negative BTL output
B1	VDD	Power Supply
B2	PVDD	Power Supply
B3	PGND	Power Ground
C1	IN-	Negative differential input
C2	SDB	Shutdown terminal (low active)
C3	VO+	Positive BTL output

**Function Block Diagram**


Notes: Total Voltage Gain =  $Av1 \times Av2 = 2 \times \frac{150k}{R_i}$

Figure 1. Function Block Diagram

**Application Circuit**

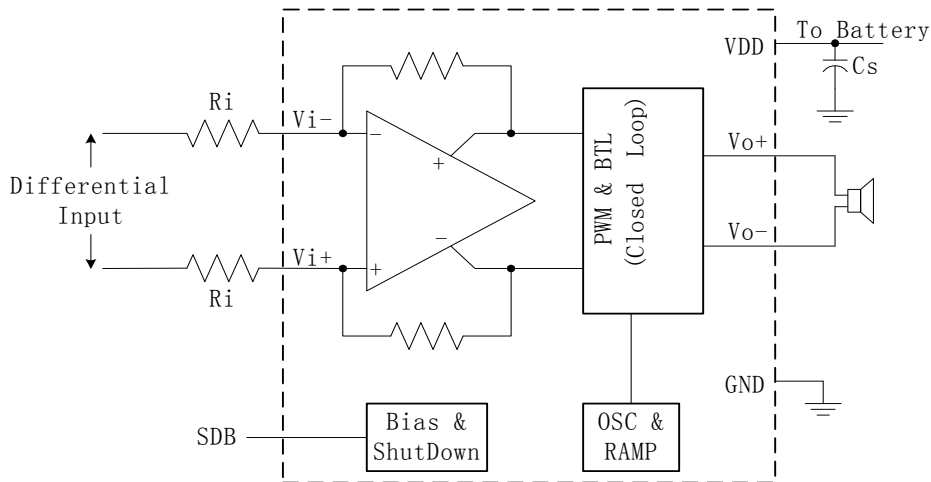


Figure 2. BL6311B Application Schematic With Differential Input

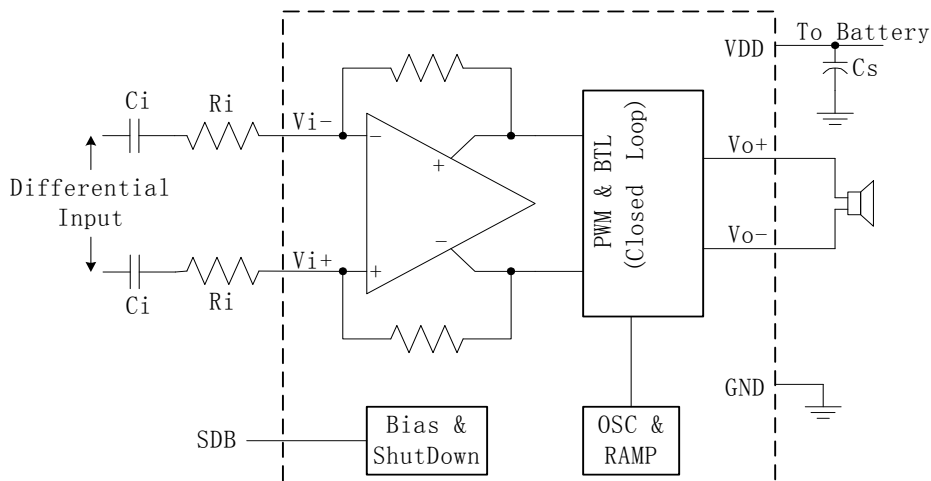


Figure 3. BL6311B Application Schematic With Differential Input and Input Capacitors

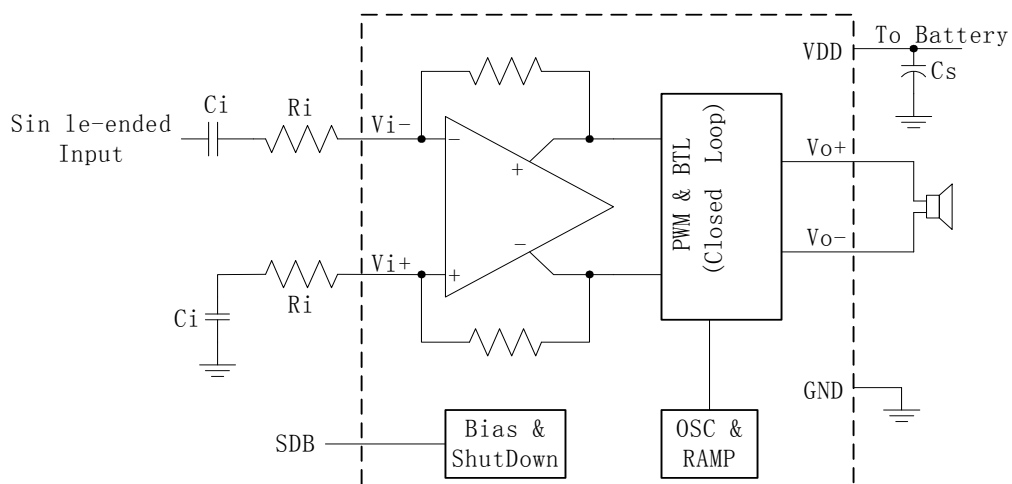


Figure 4. BL6311B Application Schematic With Single-Ended Input

**Absolute Maximum Ratings**

Supply voltage	-0.3V to 6V
Input voltage	-0.3V to VDD+0.3V
Junction Temperature	-40 to +150
Storage Temperature	-65 to +150

Note: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device.

**Recommended Operating Conditions**

	Min	Max	Unit
Supply Voltage	2.8	5.5	V
Shutdown Voltage Input High	1.3	VDD	V
Shutdown Voltage Input Low	0	0.4	V

**Electrical Characteristics**

The following specifications apply for the circuit shown in Figure 5.

$T_A = 25$  , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
$I_{SD}$	Shutdown Current	$V_{IN}=0V, V_{SDB}=0V, \text{No Load}$		0.4	2	$\mu A$
$I_Q$	Quiescent Current	$V_{DD} = 2.8V, V_{IN} = 0V, \text{No Load}$		2.2		mA
		$V_{DD} = 3.6V, V_{IN} = 0V, \text{No Load}$		2.6		
		$V_{DD} = 5.5V, V_{IN} = 0V, \text{No Load}$		4.0	8	
$ V_{OS} $	Output Offset Voltage	$V_{IN} = 0V, A_v = 2V/V,$ $V_{DD} = 2.8V \text{ to } 5.5V$		2	25	mV
PSRR	Power Supply Rejection Ratio	$V_{DD} = 2.8V \text{ to } 5.5V$		-75		dB
CMRR	Common Mode Rejection Ratio	$V_{DD} = 2.8V \text{ to } 5.5V,$ $V_{IC} = V_{DD}/2 \text{ to } 0.5V,$ $V_{IC} = V_{DD}/2 \text{ to } V_{DD} - 0.8V$		-68		dB
$F_{SW}$	Modulation frequency	$V_{DD} = 2.8V \text{ to } 5.5V$	200	250	300	kHz
$A_v$	Voltage gain	$V_{DD} = 2.8V \text{ to } 5.5V$	$\frac{285k}{R_I}$	$\frac{300k}{R_I}$	$\frac{315k}{R_I}$	V/V
$R_{SDB}$	Resistance from SDB to GND			300		k $\Omega$
$Z_I$	Input impedance		142	150	158	k $\Omega$
$T_{WU}$	Wake-up time from shutdown	$V_{DD} = 3.6V$		32		mS
$r_{DS(on)}$	Drain-Source resistance (on-state)	$V_{DD} = 2.8V$		700		m $\Omega$
		$V_{DD} = 3.6V$		500		
		$V_{DD} = 5.5V$		400		

**Operating Characteristics**

□  $V_{DD} = 5V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25$  , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		3.0		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		2.4		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		1.7		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		1.4		
THD+N	Total Harmonic Distortion + Noise	Po=1.0Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.1		%
SNR	Signal-to-Noise ratio	V <sub>DD</sub> =5V, Po=1.0Wrms, R <sub>L</sub> = 8Ω		97		dB

□  $V_{DD} = 3.6V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25$  , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		1.5		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		1.2		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		0.9		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		0.7		
THD+N	Total Harmonic Distortion + Noise	Po=0.5Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.1		%
K <sub>SVR</sub>	Supply ripple rejection ratio	V <sub>DD</sub> = 3.6V, input ac-grounded with C <sub>I</sub> = 2uF f=217Hz, V(Ripple)=200mV <sub>PP</sub>		-68		dB
V <sub>n</sub>	Output voltage noise	V <sub>DD</sub> = 3.6V, input ac-grounded with C <sub>I</sub> = 2uF, f=20~20kHz	No weighting	48		uV <sub>RMS</sub>
			A weighting	36		
CMRR	Common Mode Rejection Ratio	V <sub>DD</sub> = 3.6V, V <sub>IC</sub> = 1 V <sub>PP</sub> , f=217Hz		-70		dB

□  $V_{DD} = 2.8V$ ,  $R_I = 150k\Omega$ ,  $T_A = 25$  , unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P <sub>O</sub>	Output Power	THD+N=10%, f=1KHz, R <sub>L</sub> = 4Ω		0.92		W
		THD+N=1%, f=1KHz, R <sub>L</sub> = 4Ω		0.75		
		THD+N=10%, f=1KHz, R <sub>L</sub> = 8Ω		0.52		
		THD+N=1%, f=1KHz, R <sub>L</sub> = 8Ω		0.41		
THD+N	Total Harmonic Distortion + Noise	Po=0.2Wrms, f=1kHz, R <sub>L</sub> = 8Ω		0.1		%

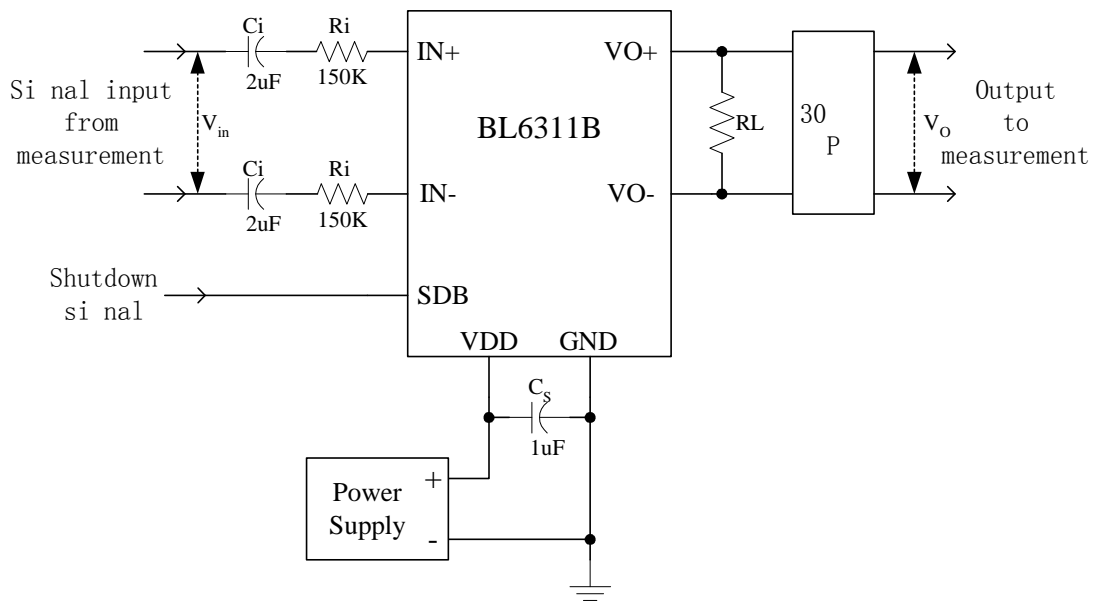
**Test Circuit**


Figure 5. BL6311B test setup circuit

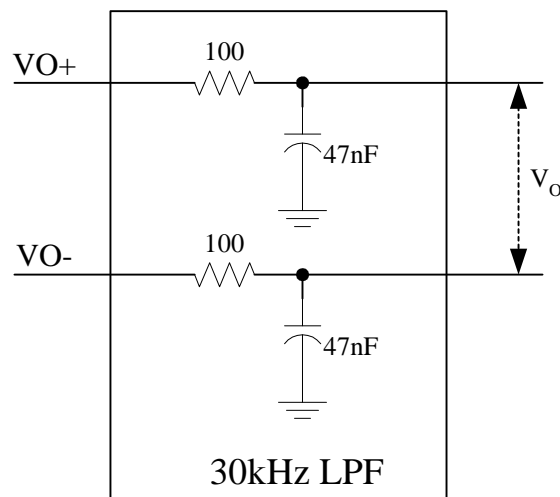


Figure 6. 30-kHz LPF for BL6311B test

- Notes:
- 1>.  $C_s$  should be placed as close as possible to VDD/GND pad of the device
  - 2>.  $C_i$  should be shorted for any Common-Mode input voltage measurement
  - 3>. A 33uH inductor should be used in series with  $R_L$  for efficiency measurement
  - 4>. The 30 kHz LPF (shown in figure 5) is required even if the analyzer has an internal LPF

**Component Recommended**

Due to the weak noise immunity of the single-ended input application, the differential input application should be used whenever possible. The typical component values are listed in the table:

$R_I$	$C_I$	$C_S$
150 k	3.3 nF	2.2 uF

- (1)  $C_1$  should have a tolerance of  $\pm 10\%$  or better to reduce impedance mismatch.
- (2) Use 1% tolerance resistors or better to keep the performance optimized, and place the  $R_1$  close to the device to limit noise injection on the high-impedance nodes.

### Input Resistors ( $R_1$ ) & Capacitors ( $C_1$ )

The input resistors ( $R_1$ ) set the total voltage gain of the amplifier according to Eq1

$$Gain = \frac{2 \times 150k\Omega}{R_1} \left( \frac{V}{V} \right) \quad Eq1$$

The input resistor matching directly affects the CMRR, PSRR, and the second harmonic distortion cancellation.

If a differential signal source is used, and the signal is biased from  $0.5V \sim V_{DD}-0.8V$  (shown in Figure2), the input capacitor ( $C_1$ ) is not required.

If the input signal is not biased within the recommended common-mode input range in differential input application (shown in Figure3), or in a single-ended input application (shown in Figure4), the input coupling capacitors are required.

If the input coupling capacitors are used, the  $R_1$  and  $C_1$  form a high-pass filter (HPF). The corner frequency ( $f_c$ ) of the HPF can be calculated by Eq2

$$f_c = \frac{1}{2\pi \cdot R_1 \cdot C_1} \quad (Hz) \quad Eq2$$

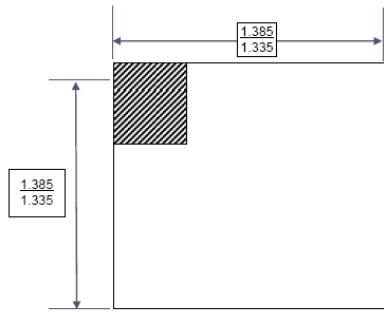
### Decoupling Capacitor ( $C_S$ )

A good low equivalent-series-resistance (ESR) ceramic capacitor ( $C_S$ ), used as power supply decoupling capacitor ( $C_S$ ), is required for high power supply rejection (PSRR), high efficiency and low total harmonic distortion (THD). Typically  $C_S$  is  $2 \sim 2\mu F$ , placed as close as possible to the device VDD pin.

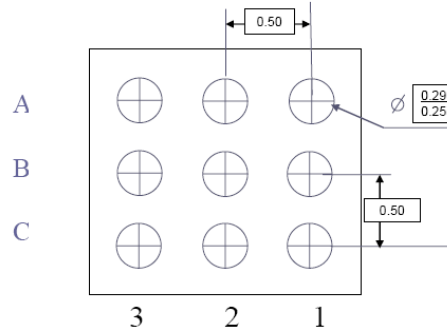
### Order Information

Part Number	Package	Shipping
BL6311B	CSP9	3000 pcs / Tape & Reel

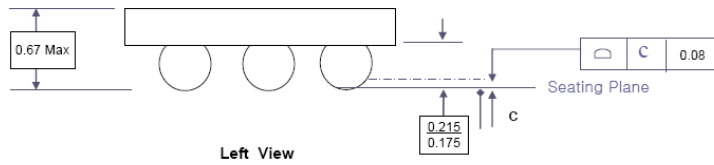
**Package Dimensions**



Top View



Bottom View



Left View

**NOTES:** All linear dimensions are in millimeters.

A1 is the location for Pin 1