2.7 W/CH Stereo Filter-Free Class-D Audio Power Amplifier

Features

- Output power:
  2.7W/Ch with 4Ω loader at V_{DD}=5V
  1.5W/Ch with 8Ω loader at V_{DD}=5V
- Low supply current (Typical 7mA quiescent current)
- Low shutdown current (Typical 0.4μA shutdown current)
- Thermal protection and output over current protection are designed
- Optimized PWM output stage eliminates LC output filter
- Independent shutdown control for each channel
- Select gain of 6, 12, 18, 24 dB
- Internally generated 300-kHz switching frequency eliminates capacitor and resistor
- Internal pull-down resistor on shutdown terminal

General Description

The BL6312 is a 2.7-W high efficiency, stereo, filter-free class-D audio power amplifier in QFN20 package that requires only two external components.

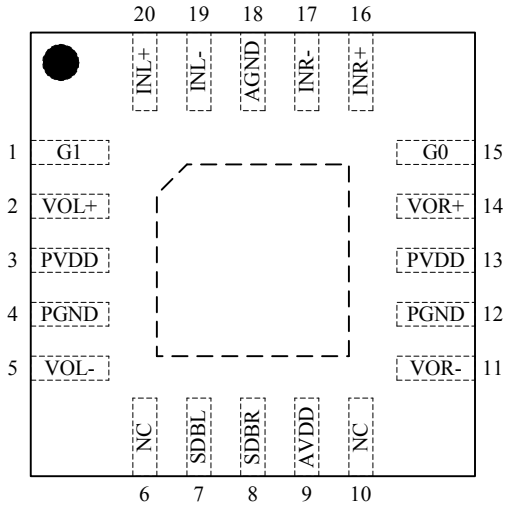
Features like 88% efficiency, improved RF-rectification immunity make the BL6312 ideal for cellular handsets. In cellular handsets, the earpiece, speaker phone, and melody ringer can each be driven by the BL6312.

Applications

- Mobile phone、PDA
- MP3/4、PMP
- Portable electronic devices
- USB Speakers
- Educational toys
- Notebook PC

Pin Diagrams

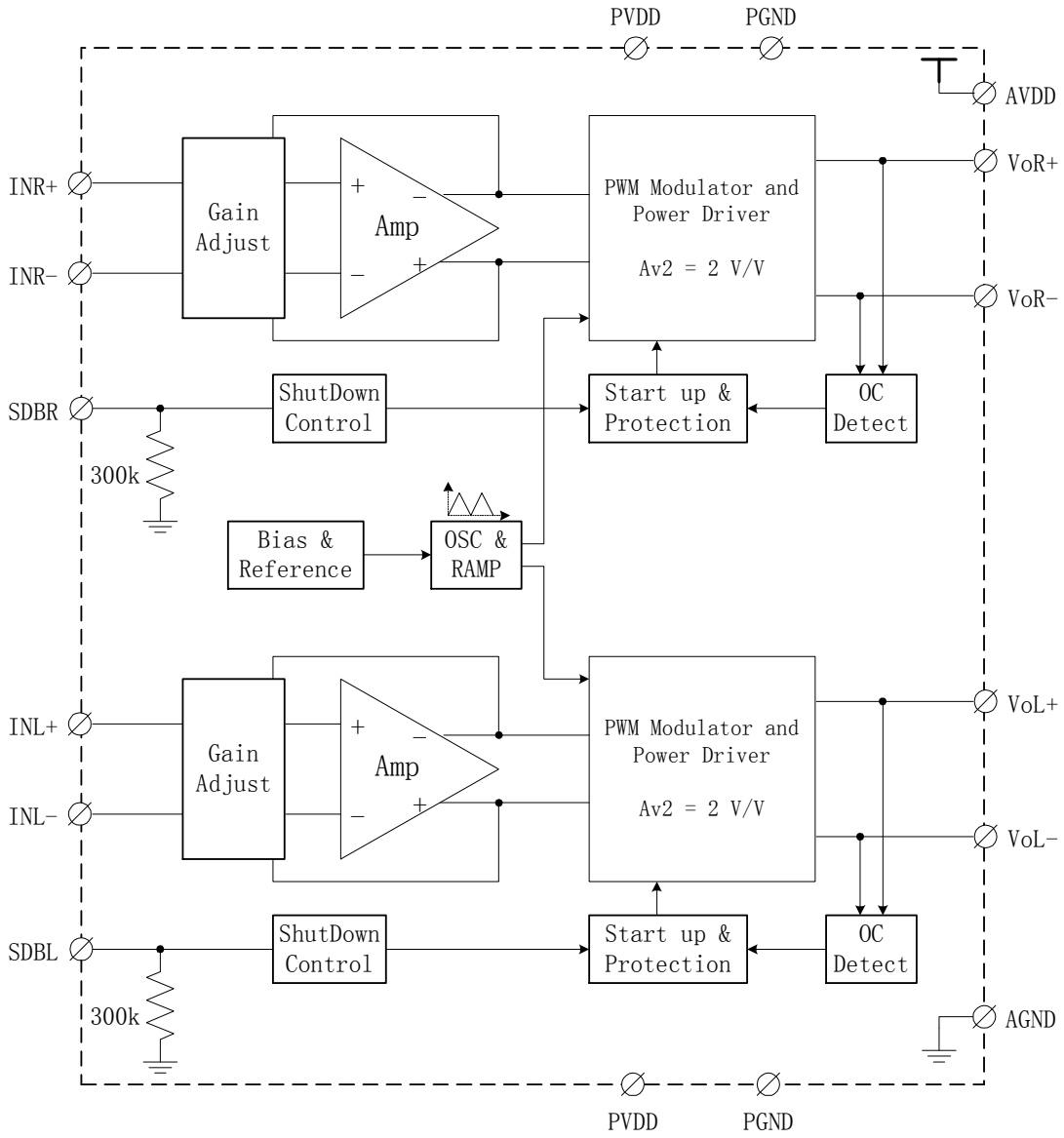
QFN20 PACKAGE
(Top View)



Pin Description

Pin #	Name	Description
1	G1	Gain select (MSB)
2	VOL+	Left channel positive differential output
3	PVDD	Power Supply (Must be the same voltage as AVDD)
4	PGND	Power Ground
5	VOL-	Left channel negative differential output
6	NC	No internal connection
7	SDBL	Left channel Shutdown terminal (low active)
8	SDBR	Right channel Shutdown terminal (low active)
9	AVDD	Analog supply (Must be the same voltage as PVDD)
10	NC	No internal connection
11	VOR-	Right channel negative differential output
12	PGND	Power Ground
13	PVDD	Power Supply (Must be the same voltage as AVDD)
14	VOR+	Right channel positive differential output
15	G0	Gain select (LSB)
16	INR+	Right channel positive input
17	INR-	Right channel negative input
18	AGND	Analog Ground
19	INL-	Left channel negative input
20	INL+	Left channel positive input
Thermal PAD		Connect the thermal pad of QFN package to GND

Function Block Diagram



Notes: Total Voltage Gain

G1	G0	V/V	dB
0	0	2	6
0	1	4	12
1	0	8	18
1	1	16	24

Figure 1. Function Block Diagram

Application Circuit

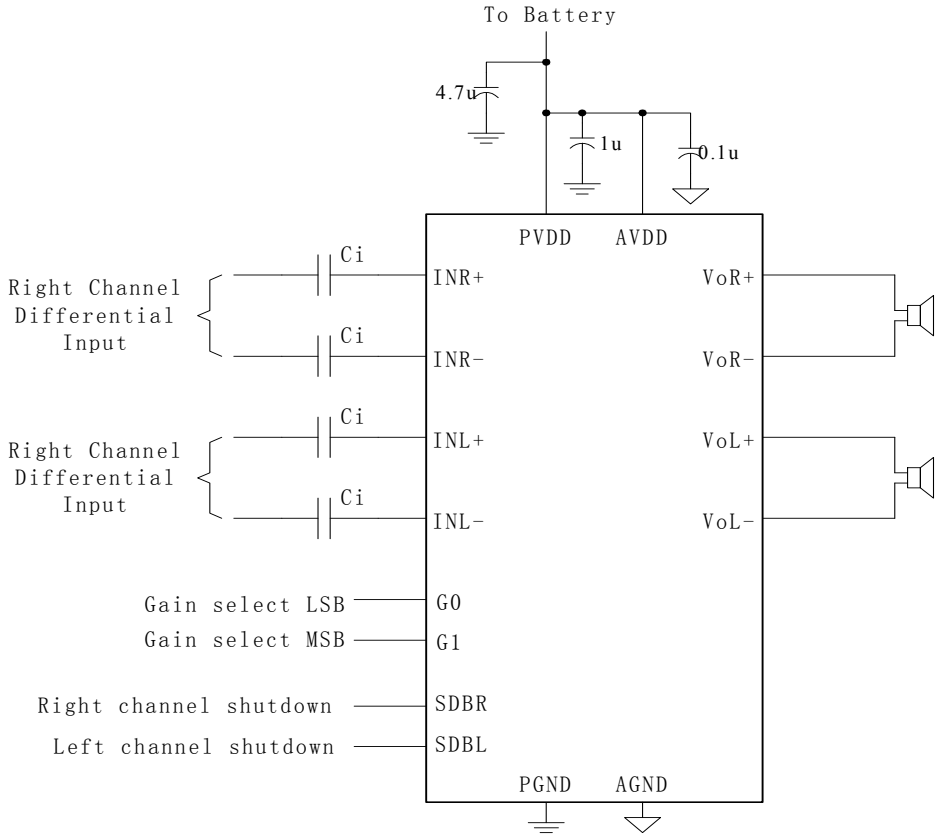


Figure 2. BL6312 Application Schematic With Differential Input

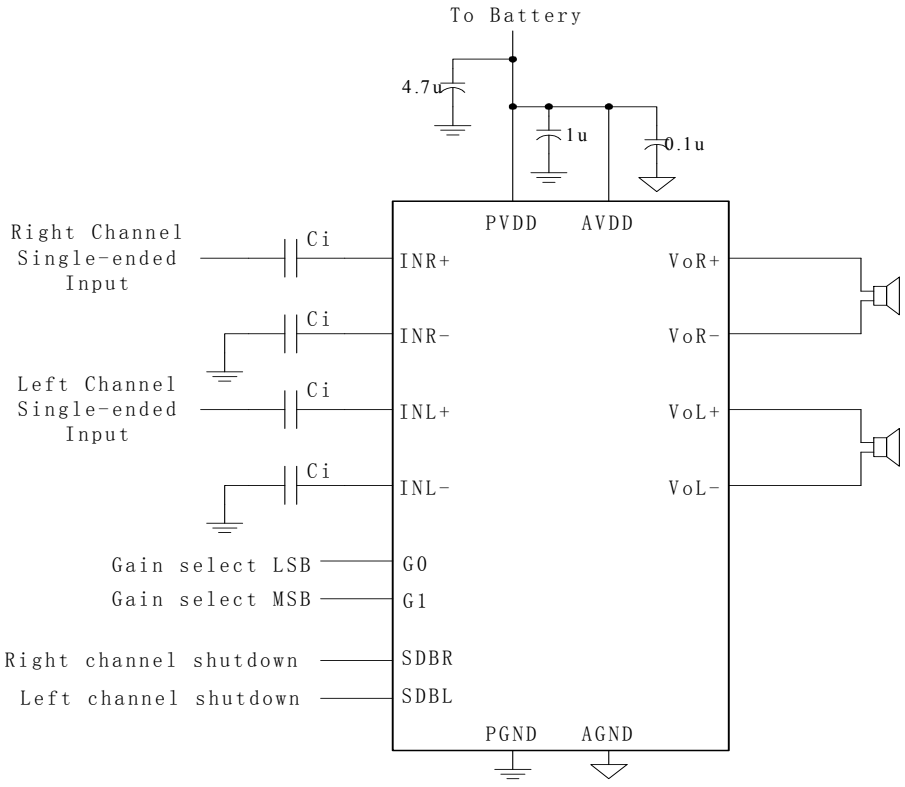


Figure 3. BL6312 Application Schematic With Single-Ended Input

Electrical Characteristics

The following specifications apply for the circuit shown in Figure 5.

T_A = 25℃, unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
I_{SD}	Shutdown Current	V_{IN}=0V, V_{SDB}=0V, No Load		0.1	1.5	uA
I_Q	Quiescent Current	V_{DD} = 2.5V, V_{IN} = 0V, No Load		3.5	6	mA
		V_{DD} = 3.6V, V_{IN} = 0V, No Load		4.3	7.5	
		V_{DD} = 5.5V, V_{IN} = 0V, No Load		7	11	
$\lvert V_{OS} \rvert$	Output Offset Voltage	V_{DD} = 2.5V to 5.5V		7	25	mV
CMRR	Common Mode Rejection Ratio	Inputs shorted together, V_{DD} = 2.5V to 5.5V		-70		dB
Channel crosstalk		f=1k Hz		-110		dB
F_{SW}	Modulation frequency	V_{DD} = 2.5V to 5.5V	250	300	350	kHz
A_V	Closed-loop voltage gain	G1=0.35v, G0=0.35v	5.5	6	6.5	dB
		G1=0.35v, G0= V_{DD}	11.5	12	12.5	
		G1= V_{DD} , G0=0.35v	17.5	18	18.5	
		G1= V_{DD} , G0= V_{DD}	23.5	24	24.5	
T_{WU}	Wake-up time from shutdown	V_{DD} = 3.6V		1		mS
Resistance from SDBR/SDBL to GND			142	150	158	kΩ
$r_{DS(on)}$	Drain-Source resistance (on-state)	V_{DD} = 5.5V		400		mΩ
		V_{DD} = 3.6V		500		
		V_{DD} = 2.5V		700		
Input impedance		A_V=6 dB		28.1		kΩ
		A_V=12dB		17.3		
		A_V=18dB		9.8		
		A_V=24dB		5.2		

Operating Characteristics

❑ **V_{DD} = 5V,** T_A = 25℃, unless otherwise specified.

Symbol	Parameter	Conditions	Spec			Units
			Min.	Typ.	Max.	
P_O	Output Power (per channel)	THD+N=10%, f=1KHz, R_L = 4Ω		2.7		W
		THD+N=10%, f=1KHz, R_L = 8Ω		1.6		
THD+N	Total Harmonic Distortion + Noise	Po=1.0Wrms, f=1kHz, R_L = 8Ω, A_V=6dB		0.12		%
		Po=0.5Wrms, f=1kHz, R_L = 8Ω, A_V=6dB		0.13		
K_{SVR}	Supply ripple rejection ratio	V_{DD} = 5V, A_V=6dB f=217Hz, V(Ripple)=200mV_{PP}		-63		dB
CMRR	Common Mode Rejection Ratio	V_{DD} = 5V, V_{IC} = 1 V_{PP}, f=217Hz		-70		dB

❑ **V_{DD} = 3.6V,** T_A = 25℃, unless otherwise specified.

Symbol	Parameter	Conditions		Spec			Units
				Min.	Typ.	Max.	
P_O	Output Power (per channel)	THD+N=10%, f=1KHz, R_L = 8Ω			0.8		W
K_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6V, input ac-grounded with C_I = 2uF f=217Hz, V(Ripple)=200mV_{PP}			-63		dB
CMRR	Common Mode Rejection Ratio	V_{DD} = 3.6V, V_{IC} = 1 V_{PP}, f=217Hz			-70		dB
V_n	Output voltage noise	V_{DD} = 3.6V, input ac-grounded with C_I = 2uF, f=20~20kHz	No weighting		50		uV_{RMS}
			A weighting		38		

Test Circuit

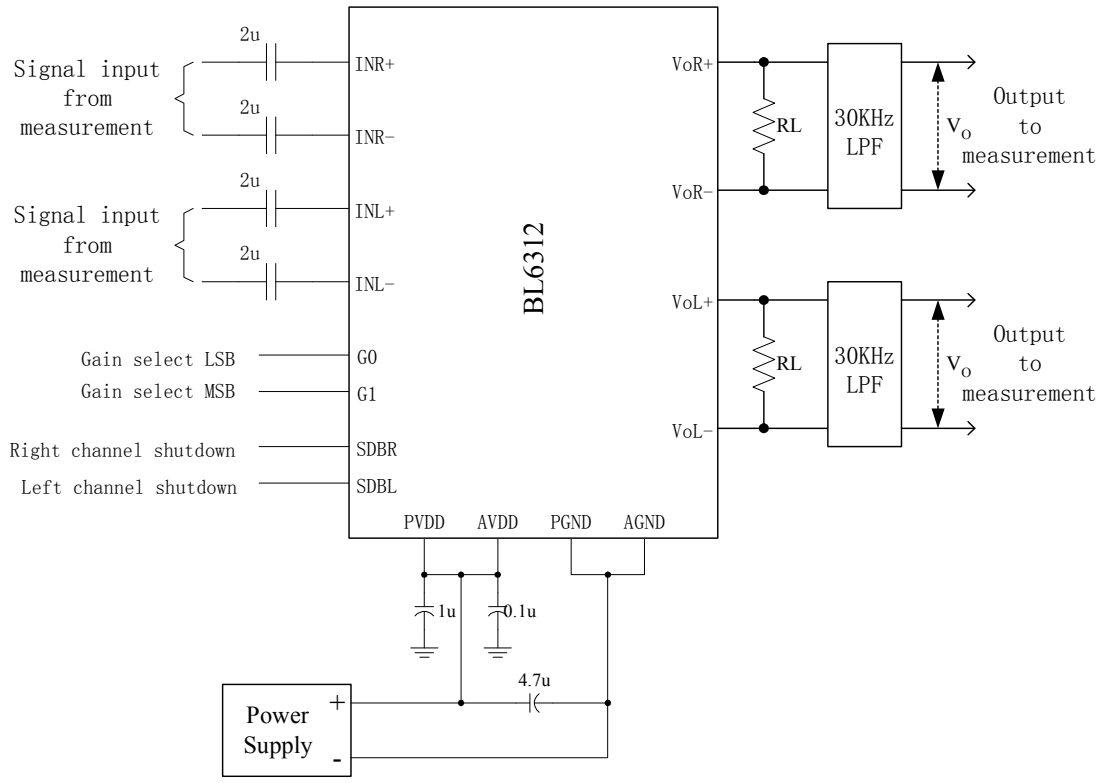


Figure 4. BL6312 test set up circuit

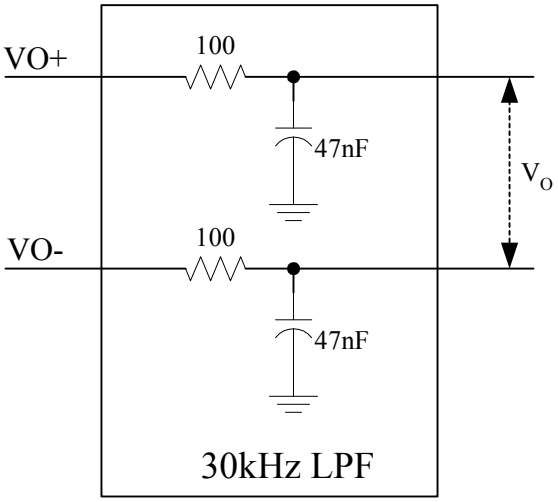


Figure 5. 30-kHz LPF for BL6312 test

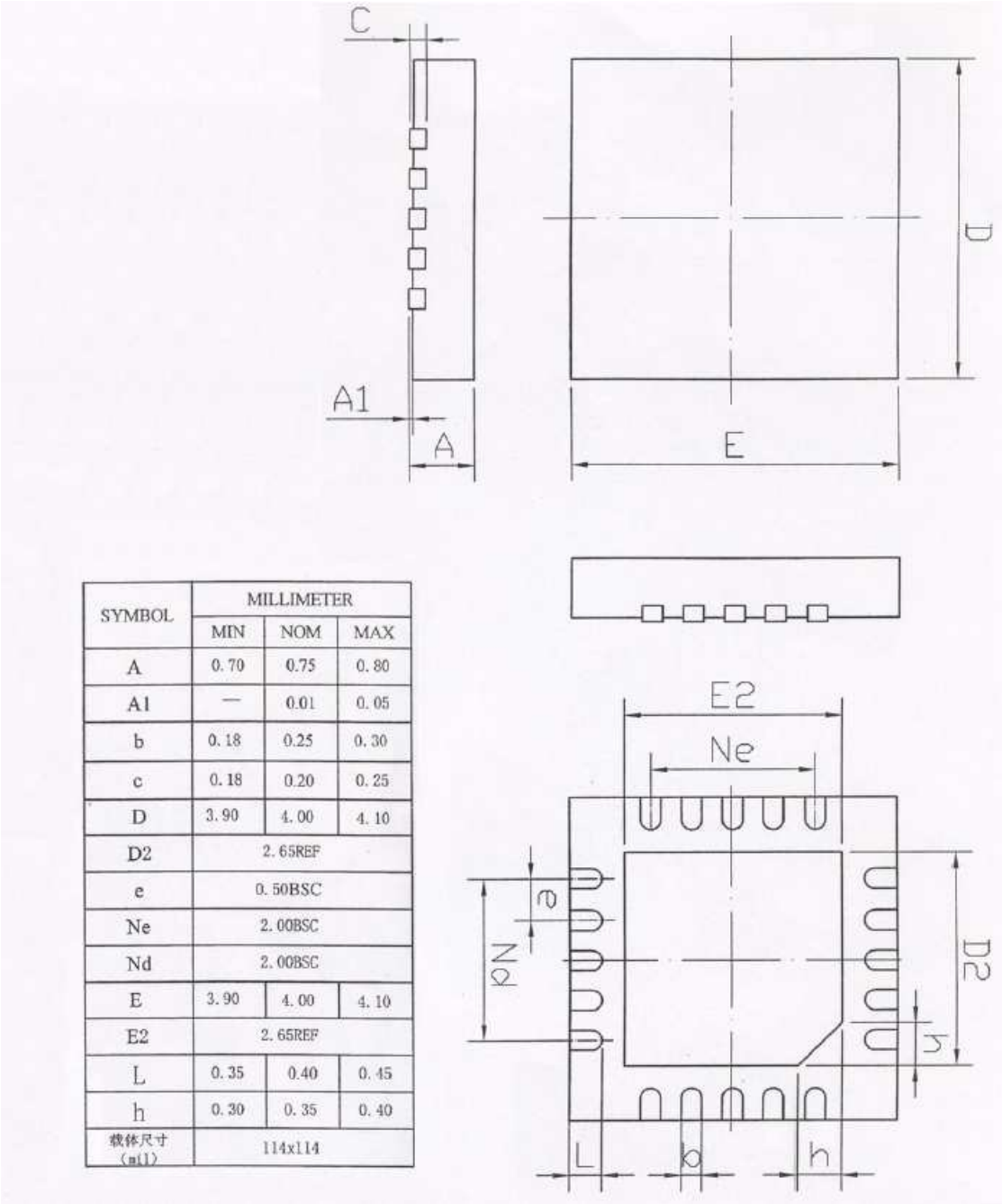
Notes: 1>. A 1uF capacitor should be placed as close as possible to PVDD pin, and a 0.1uF capacitor should be placed as close as possible to AVDD pin of the device

2>. Ci should be shorted for any Common-Mode input voltage measurement

3>. A 33uH inductor should be used in series with R_L for efficiency measurement

4>. The 30 kHz LPF (shown in figure 5) is required even if the analyzer has an internal LPF

Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.01	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.65REF		
e	0.50BSC		
Ne	2.00BSC		
Nd	2.00BSC		
E	3.90	4.00	4.10
E2	2.65REF		
L	0.35	0.40	0.45
h	0.30	0.35	0.40
载体尺寸 (mil)	114x114		