## FEATURES

- High accuracy, less than 0.3% error over a dynamic range of 500 : 1
- Exactly measure the real power in the positive orientation and negative orientation, calculate the energy in the same orientation
- Two current monitors continuously monitor the phase and neutral currents in two-wire distribution systems. Uses the larger of two currents to bill, even during a Fault condition
- A PGA in the current channel allows using small value shunt and burden resistance
- The low frequency outputs F1 and F2 can directly drive electromechanical counters and two phase stepper motors and the high frequency output CF, supplies instantaneous real power, is intended for calibration and communications
- Two logic outputs REVP and FAULT can be used to indicate a potential orientation or Fault condition
- On-Chip power supply detector
- On-Chip anti-creep protection
- On-Chip voltage reference of 2.44V ± 8% (typical temperature coefficient of 30ppm/℃), with external overdrive capability
- Single 5V supply
- Low static power (typical value of 15mW). The technology of SLiM (Smart–Low–current–Management ) is used.

Interrelated patents are pending

## DESCRIPTION

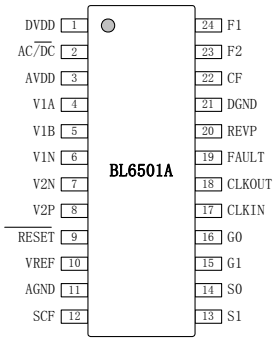
The BL6501A is a low cost, high accuracy, high stability, simple peripheral circuit electrical energy meter IC. The meter based on the BL6501A is intended for using in single-phase, two-wire distribution systems. It can exactly measure the real power in the positive orientation and negative orientation and calculate the energy in the same orientation.

The BL6501A incorporates a novel fault detection scheme that both warns of fault conditions and allows the BL6501A to continue accurate billing during a fault event. The BL6501A does this by continuously monitoring both the phase and neutral (return) currents. Fault condition is indicated by PIN19 (FAULT), when these currents differ by more than 12%. Billing is continued using the larger of the two currents when the difference is greater than 14%.

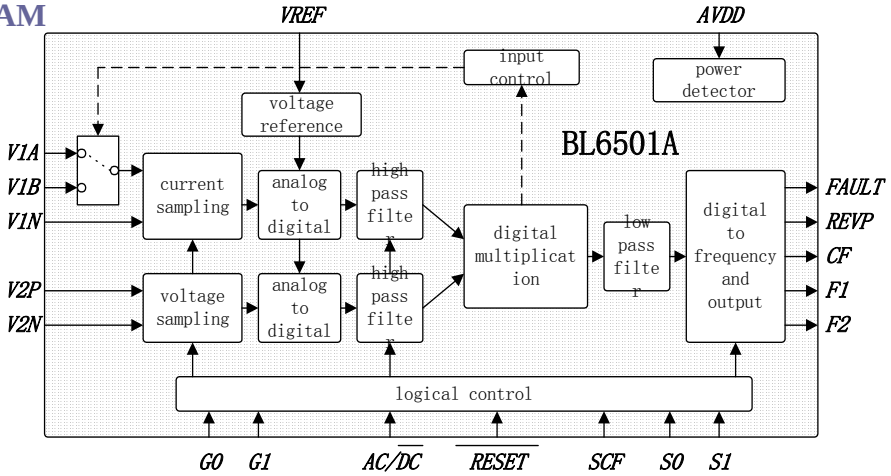
The BL6501A supplies average real power information on the low frequency outputs F1 (Pin23) and F2 (Pin24). These logic outputs may be used to directly drive an electromechanical counter and two-phase stepper motors. The CF (Pin22) logic output gives instantaneous real power information. This output is intended to be used for calibration purposes or interface to an MCU.

BL6501A thinks over the stability of reading error in the process of calibration.. An internal no-load threshold ensures that the BL6501A does not exhibit any creep when there is no load.

## BLOCK DIAGRAM




DIP/SSOP 24



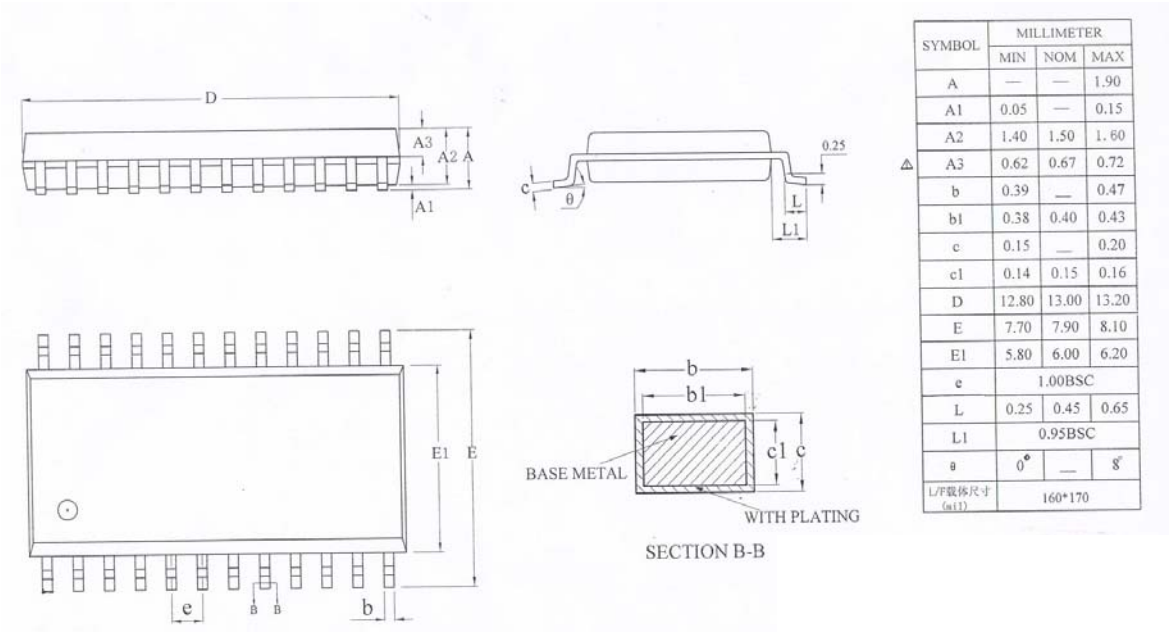
## ◆ PIN DESCRIPTIONS

| Pin | Symbol | DESCRIPTIONS |
|---|---|---|
| 1 | DVDD | Digital Power Supply (+5V). Provides the supply voltage for the digital circuitry. It should be maintained at 5 V±5% for specified operation. |
| 2 | AC/$\overline{DC}$ | High-Pass Filter Select. This logic input is used to enable the high pass filter in the current channel. Logic high on this pin enables the HPF. |
| 3 | AVDD | Analog Power Supply (+5V). Provides the supply voltage for the analog circuitry. It should be maintained at 5 V±5% for specified operation. |
| 4,5 | V1A,V1B | Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum signal level of ±660 mV with respect to pin6 (V1N) for specified operation. |
| 6 | V1N | Negative Input Pin for Differential Voltage Inputs V1A and V1B. |
| 7,8 | V2N,V2P | Negative and Positive Inputs for Voltage Channel. These inputs provide a fully differential input pair. The maximum differential input voltage is ±660 mV for specified operation. |
| 9 | $\overline{RESET}$ | Reset Pin. Logic low on this pin will hold the ADCs and digital circuitry in a reset condition and clear internal registers. |
| 10 | VREF | On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.44V ± 8% and a typical temperature coefficient of 30ppm/℃. An external reference source may also be connected at this pin. |
| 11 | AGND | Analog Ground Reference. Provides the ground reference for the analog circuitry. |
| 12 | SCF | Calibration Frequency Select. This logic input is used to select the frequency on the calibration output CF. |
| 13,14 | S1,S0 | Output Frequency Select. These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. |
| 15,16 | G1,G0 | Gain Select. These logic inputs are used to select one of four possible gains for current channel. The possible gains are 1, 2, 8, and 16. |
| 17 | CLKIN | Clock In. An external clock can be provided at this logic input. Alternatively, a crystal can be connected across this pin and pin18 (CLKOUT) to provide a clock source |
| 18 | CLKOUT | Clock Out. A crystal can be connected across this pin and pin17 (CLKIN) as described above to provide a clock source. |
| 19 | FAULT | Fault Indication. Logic high indicates fault condition. Fault is defined as a condition under which the signals on V1A and V1B differ by more than 12.5%. The logic output will be reset to zero when fault condition is no longer detected. |
| 20 | REVP | Negative Indication. Logic high indicates negative power, i.e., when the phase angle between the voltage and current signals is greater that 90°. This output is not latched and will be reset when positive power is once again detected. |
| 21 | DGND | Digital Ground Reference. Provides the ground reference for the digital circuitry. |
| 22 | CF | Calibration Frequency. The CF logic output gives instantaneous real power information. This output is intended to use for calibration purposes. |
| 23,24 | F1,F2 | Low-Frequency. F1 and F2 supply average real power information. The logic outputs |

| | | |
|---|---|---|
| | | can be used to directly drive electromechanical counters and 2-phase stepper motors. |

## ◆ PACKAGE DIMENSIONS

24 PIN SSOP




| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | — | — | 1.90 |
| A1 | 0.05 | — | 0.15 |
| A2 | 1.40 | 1.50 | 1.60 |
| A3 | 0.62 | 0.67 | 0.72 |
| b | 0.39 | — | 0.47 |
| b1 | 0.38 | 0.40 | 0.43 |
| c | 0.15 | — | 0.20 |
| c1 | 0.14 | 0.15 | 0.16 |
| D | 12.80 | 13.00 | 13.20 |
| E | 7.70 | 7.90 | 8.10 |
| E1 | 5.80 | 6.00 | 6.20 |
| e | 1.00BSC | | |
| L | 0.25 | 0.45 | 0.65 |
| L1 | 0.95BSC | | |
| θ | 0° | — | 8° |
| L/F载体尺寸 (unit) | 160*170 | | |

## ◆ ABSOLUTE MAXIMUM RATINGS

( T = 25 ℃ )

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Analog Power Voltage AVDD | AVDD | -0.3~+7(max) | V |
| Digital power Voltage DVDD | DVDD | -0.3~+7(max) | V |
| DVDD to AVDD | | -0.3~+0.3 | V |
| Analog Input Voltage of Channel 2 to AGND | V (V) | VSS+0.5≤V(v)≤VDD-0.5 | V |
| Analog Input Voltage of Channel 1 to AGND | V (I) | VSS+0.5≤V(i)≤VDD-0.5 | V |
| Operating Temperature Range | Topr | -40~+85 | ℃ |
| Storage Temperature Range | Tstr | -55~+150 | ℃ |
| Power Dissipation（DIP24） | | 15 | mW |

## ◆ Electronic Characteristic Parameter

(T=25℃, AVDD=5V, DVDD= 5V, CLKIN=3.58MHz)

| Parameter | Symbol | Test Condition | Measure Pin | Min Value | Typical Value | Max Value | Unit |
|---|---|---|---|---|---|---|---|
| 1 Analog Power Current | $I_{AVDD}$ | | Pin1 | | 2 | 3 | mA |
| 2 Digital Power Current | $I_{DVDD}$ | | Pin3 | | 1 | 2 | mA |
| 3 Logic Input Pins | | | Pin2, | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| G0, G1, SCF,S0,S1, ACDC, /RESET | | | 9,12,13,14, 15,16 | | | | |
| Input High Voltage | $V_{IH}$ | AVDD=5V DVDD=5V | | 2 | | | V |
| Input Low Voltage | $V_{IL}$ | | | | | 1 | V |
| Input Capacitance | $C_{IN}$ | | | | 10 | | pF |
| 4 Logic Output Pins F1, F2 | | | Pin23, 24 | | | | |
| Output High Voltage | $V_{OH1}$ | $I_H$=10mA | | 4.4 | | | V |
| Output Low Voltage | $V_{OL1}$ | $I_L$=10mA | | | | 0.5 | V |
| Output Current | $I_{O1}$ | | | | 10 | | mA |
| 5 Logic Output Pins CF, REVP, FAULT | | | Pin22, 20,19 | | | | |
| Output High Voltage | $V_{OH2}$ | $I_H$=10mA | | 4.4 | | | V |
| Output Low Voltage | $V_{OL2}$ | $I_L$=10mA | | | | 0.5 | V |
| Output Current | $I_{O2}$ | | | | 10 | | mA |
| 6 On-chip Reference | Vref | AVDD=5V | Pin10 | 2.245 | 2.44 | 2.635 | V |
| 7 Analog Input Pins V1A, V1B, V1N, V2N, V2P | | | Pin4, 5,6, 7,8 | | | | |
| Maximum Input Voltage | $V_{AIN}$ | | | | | ±1 | V |
| DC Input Impedance | | | | | 330 | | Kohm |
| Input Capacitance | | | | | 10 | | pF |
| 8 Accuracy | | | | | | | |
| Measurement Error on Channel 1 and 2 | | | | | | | |
| Gain=1 | ENL1 | Both Channels with Full-Scale Signal ±660mV Over a Dynamic Range 500 to 1 | Pin22 | | 0.1 | 0.3 | % |
| Gain=2 | ENL2 | | Pin22 | | 0.1 | 0.3 | % |
| Gain=8 | ENL8 | | Pin22 | | 0.1 | 0.3 | % |
| Gain=16 | ENL16 | | Pin22 | | 0.1 | 0.3 | % |
| Phase Error between Channels | | | | | | | |
| Channel 1 Lead 37° (PF=0.8Capacitive) | | | Pin22 | | 0.3 | | % |
| Channel 1 Lags (PF=0.5Inductive) | | | Pin22 | | 0.3 | | % |
| 9 Start Current | $I_{START}$ | Ib=5A C=3200, cosφ=1 Voltage Channel Inputs ±110mV Gain of Current Channel 16 | Pin5 | 0.2%Ib | | | A |
| 10 Positive and Negative Real | ENP | Vv=±110mV,V(I)= | Pin22 | | | 1 | % |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Power Error (%) | | 2mV, cosφ=1<br>Vv=±110mV,V(I)=<br>2mV, cosφ=-1 | | | | | |
| 11 Gain Error | Gain error | External 2.5V Reference,Gain=1, V1=V2=500mV DC | Pin22 | | | ±5 | % |

## ◆ TERMINOLOGY

**1) Nonlinear Error**

The Nonlinear Error is defined by the following formula:

eNL%＝[(Error at X-Error at Ib) / (1+Error at Ib )]*100%

When V(v)= ±110mV, cosφ=1, over the arrange of 5%Ib to 800%Ib, the nonlinear error should be less than 0.1%.

**2) Start Current**

When meter constant C=3200, Ib=5A, cosφ=1, V(V)=±110mV, 5％Ib error in normal range, the min AC current in current loop.

**3) Positive And Negative Real Power Error**

When the positive real power and the negative real power is equal, and V(v) =±110mV, the test current is Ib, then the positive and negative real power error can be achieved by the following formula:

eNP%=|[(eN%-eP%)/(1+eP%)]*100%|

Where: eP% is the Positive Real Power Error, eN% is the Negative Real Power Error.

**4) Phase Error Between Channels**

The HPF (High Pass Filter) in Channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in Channel 1. The phase correction network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range 40Hz to 1KHz.

**5) Gain Error**

The gain error of the BL6501A is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in channel V1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the BL6501A transfer function.

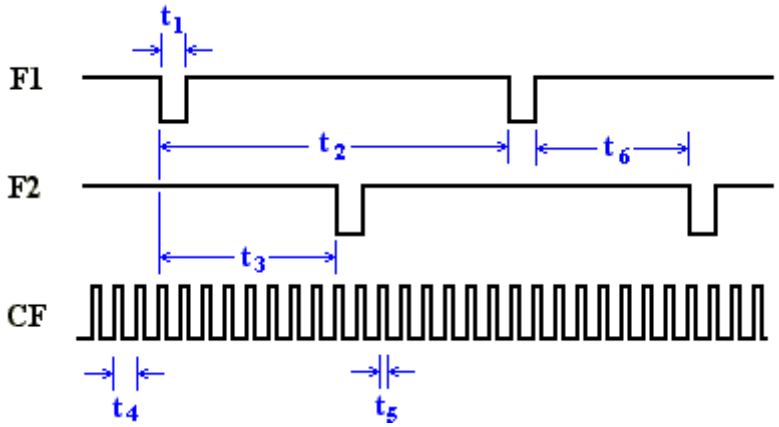
**6) Gain Error Match**

The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 2, 8, or 16. It is expressed as a percentage of the output frequency obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 8 or 16.

**7) Power Supply Monitor**

BL6501A has the on-chip Power Supply monitoring The BL6501A will remain in a reset condition until the supply voltage on AVDD reaches 4 V. If the supply falls below 4 V, the BL6501A will also be reset and no pulses will be issued on F1, F2 and CF.

## ◆ TIMING CHARACTERISTIC




(AVDD=DVDD=5V, AGND=DGND=0V, On-Chip Reference, CLKIN=3.58MHz, Temperature range: -40~+85°C)

| Parameter | Value | Comments |
|---|---|---|
| t1 | 275ms | F1 and F2 pulse-width (Logic Low). When the power is low, the t1 is equal to 275ms; when the power is high, and the output period exceeds 550ms, t1 equals to half of the output period. |
| t2 | | F1 or F2 output pulse period. |
| t3 | ½ t2 | Time between F1 falling edge and F2 falling edge. |
| t4 | 90ms | CF pulse-width (Logic high). When the power is low, the t4 is equal to 90ms; when the power is high, and the output period exceeds 180ms, t4 equals to half of the output period. |
| t5 | | CF Pulse Period. See Transfer Function section. |
| t6 | CLKIN/4 | Minimum Time Between F1 and F2. |

Notes:

1) CF is not synchronous to F1 or F2 frequency outputs.

2) Sample tested during initial release and after any redesign or process change that may affect this parameter.

## ◆ THEORY OF OPERATION

### ◆ Principle of Energy Measure

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions; Umax, Imax are the peak values of the voltage signal and the current signal; $\omega$ is the angle frequency of the input signals; the phase difference between the current signal and the voltage signal is expressed as $\phi$. Then the power is given as follows:

$$p(t) = U_{\max} \cos(wt) \times I_{\max} \cos(wt + \varphi)$$

If $\Phi=0$:

$$p(t)=\frac{U_{max}I_{max}}{2}[1+\cos(2wt)]$$

If $\Phi\neq0$:

$$p(t)=U_{max}\cos(\omega t)\times I_{max}\cos(\omega t+\Phi)$$
$$=U_{max}\cos(\omega t)\times\left[I_{max}\cos(\omega t)\cos(\Phi)+I_{max}\sin(\omega t)\sin(\Phi)\right]$$
$$=\frac{U_{max}I_{max}}{2}[1+\cos(2\omega t)]\cos(\Phi)+U_{max}I_{max}\cos(\omega t)\sin(\omega t)\sin(\Phi)$$
$$=\frac{U_{max}I_{max}}{2}[1+\cos(2\omega t)]\cos(\Phi)+\frac{U_{max}I_{max}}{2}\sin(2\omega t)\sin(\Phi)$$
$$=\frac{U_{max}I_{max}}{2}\cos(\Phi)+\frac{U_{max}I_{max}}{2}\left[\cos(2\omega t)\cos(\Phi)+\sin(2\omega t)\sin(\Phi)\right]$$
$$=\frac{U_{max}I_{max}}{2}\cos(\Phi)+\frac{U_{max}I_{max}}{2}\cos(2\omega t+\Phi)$$

P(t) is called as the instantaneous power signal. The ideal p(t) consists of the dc component and ac component whose frequency is $2\omega$. The dc component is called as the average active power, that is:

$$P=\frac{U_{max}I_{max}}{2}\cos(\varphi)$$

The average active power is related to the cosine value of the phase difference between the voltage signal and the current signal. This cosine value is called as Power Factor (PF) of the two channel signals.

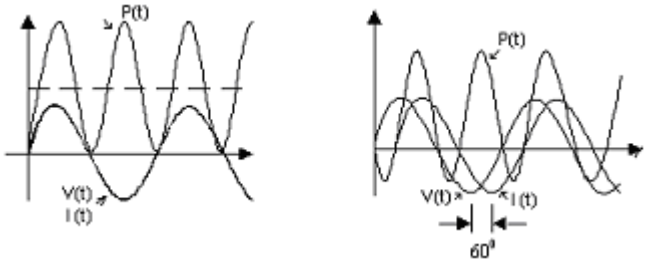



*Figure1. The Effect of phase*

When the signal phase difference between the voltage and current channels is more than 90°, the average active power is negative. It indicates the user is using the electrical energy reversely.

## ◆ Operation Process

In BL6501A, the two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit second order sigma-delta with an oversampling rate of 900 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high pass filter in the current channel removes any dc component from the current signal. This

eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals.

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 2 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates real power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

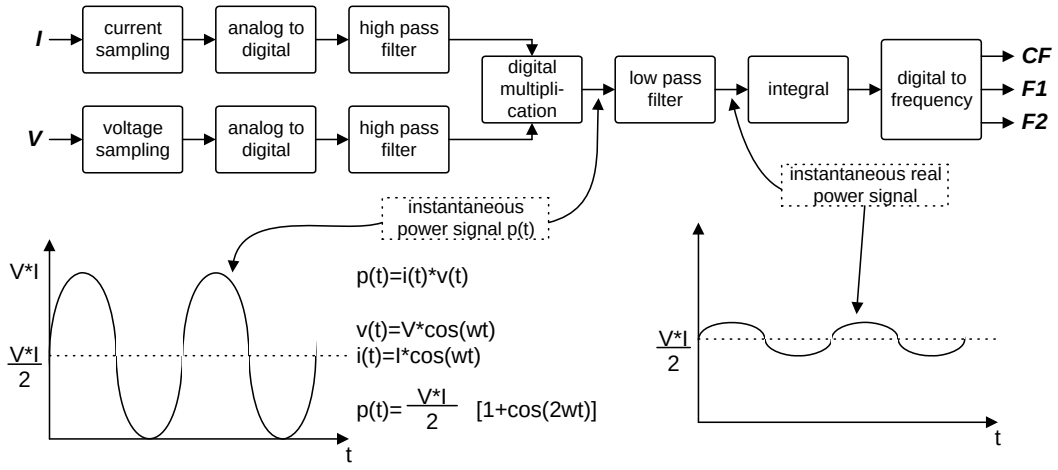



*Figure 2. Signal Processing Block Diagram*

The low frequency output of the BL6501A is generated by accumulatingm this real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and hence shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes that would take place under steady load conditions.

### ◆ Offset Effect

The dc offsets come from the input signals and the forepart analog circuitry.

Assume that the input dc offsets on the voltage channel and the current channel are $U_{offset}$ and $I_{offset}$, and PF equals 1 ( $\Phi$ =0).

$$p(t) = [U\cos(\omega t) + U_{offset}] \times [I\cos(\omega t + \Phi) + I_{offset}]$$

$$= \frac{UI}{2} + I_{offset}U\cos(\omega t) + U_{offset}I\cos(\omega t) + \frac{UI}{2}\cos(2\omega t)$$

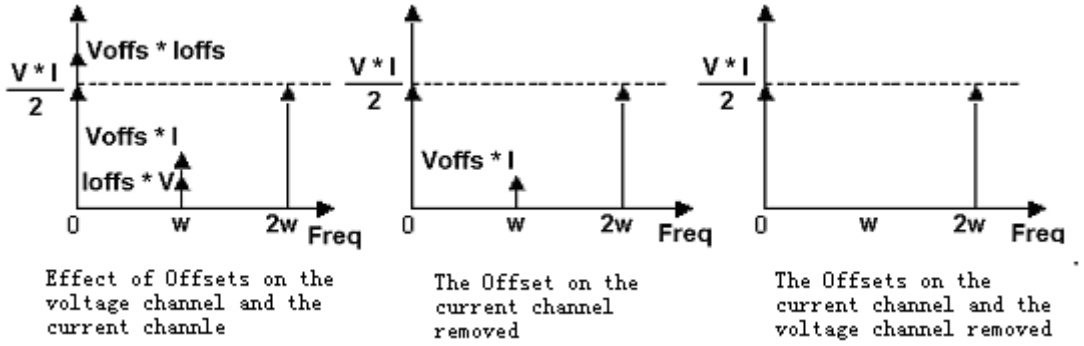



*Figure 3. Effect of Offset*

As can be seen, for each phase input, if there are simultaneous dc offsets on the voltage channel and the current channel, these offsets contribute a dc component for the result of multiplication. That is, the offsets bring the error of $U_{offset} \times I_{offset}$ to the final average real power. Additionally, there exists the component of $U_{offset} \times I + U \times I_{offset}$ at the frequency of $\omega$. The dc error on the real power will result in measure error, and the component brought to the frequency of $\omega$ will also affect the output of the average active power when the next low-pass filter can't restrain the ac component very completely.

When the offset on the one of the voltage and the current channels is filtered, for instance, the offset on the current channel is removed; the result of multiplication is improved greatly. There is no dc error, and the additional component at the frequency of $\omega$ is also decreased.

When the offsets on the voltage channel and the current channel are filtered respectively by two high-pass filters, the component at the frequency of $\omega$ (50Hz) is subdued, and the stability of the output signal is advanced. Moreover, in this case, the phases of the voltage channel and the current channel can be matched completely, and the performance when PF equal 0.5C or 0.5L is improved. In BL6501A, this structure is selected. Though it is given in the system specification that the ripple of the output signal is less than 0.1%, in real measure of BL6501A, the calibration output is very stable, and the ripple of the typical output signal is less than 0.05%.

Additionally, this structure can ensure the frequency characteristic. When the input signal changes from 45Hz to 65Hz, the complete machine error due to the frequency change is less than 0.1%. In such, the meter designed for the 50Hz input signal can be used on the transmission-line system of electric power whose frequency is 60Hz.

## ◆ VOLTAGE CHANNEL INPUT

The output of the line voltage transducer is connected to the BL6501A at this analog input. As Figure4 shows that channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±660mV. Figure4 illustrates the maximum signal levels that can be connected to the BL6501A Voltage Channel.

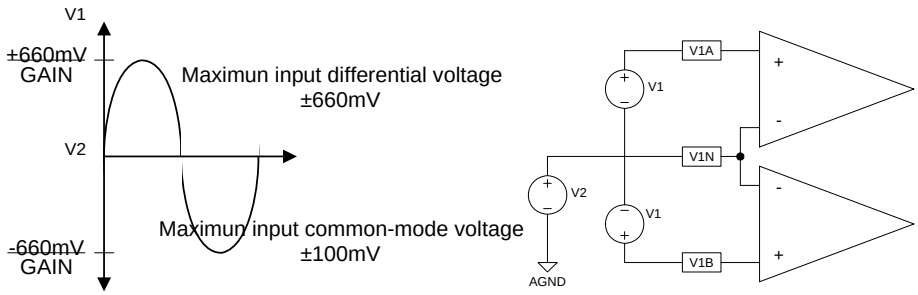



*Figure 4. Voltage Channels*

Voltage Channel must be driven from a common-mode voltage, i.e., the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the BL6501A can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

Figure5 shows two typical connections for Channel V2. The first option uses a PT (potential transformer) to provide complete isolation from the mains voltage. In the second option, the BL6501A is biased around the neutral wire and a resistor divider is used to provide a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra and Rb is also a convenient way of carrying out a gain calibration on the meter.

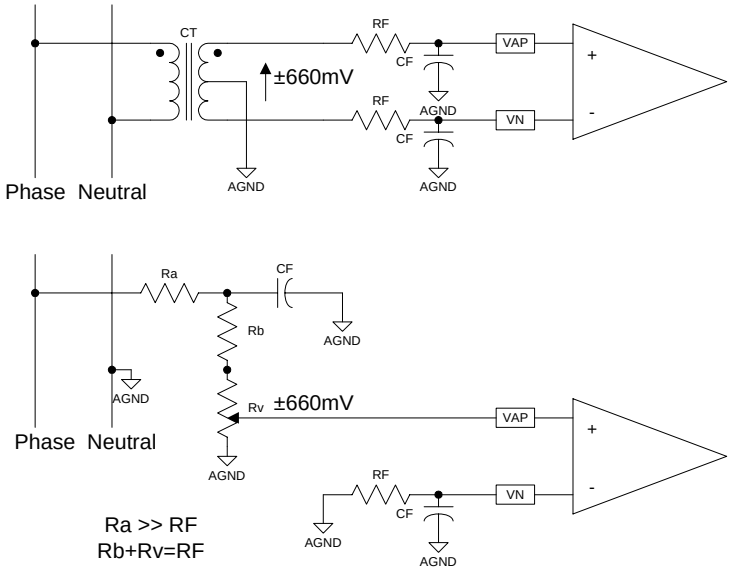



*Figure 5. Typical Connections for Voltage Channels*

## ◆ CURRENT CHANNEL INPUT

The voltage outputs from the current transducers are connected to the BL6501A here. As Figure6 shows that channel V1 has two voltage inputs, namely V1A and V1B. These inputs are fully differential with respect to V1N. However, at any one time, only one is selected to perform the power calculation.

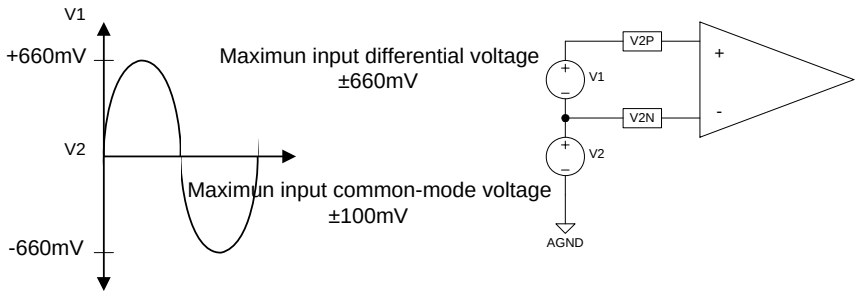



*Figure 6. Current Channels*

The analog inputs V1A, V1B and V1N have same maximum signal level restrictions as V2P and V2N. However, Channel 1 has a programmable gain amplifier (PGA) with user-selectable gains of 1, 2, 8, or 16I. These gains facilitate easy transducer interfacing. Figure illustrates the maximum signal levels on V1A, V1B, and V1N. The maximum differential voltage is ±660 mV divided by the gain selection. Again, the differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common-mode signal is ±100 mV.

Figure7 shows a typical connection diagram for Channel V1. Here the analog inputs are being used to monitor both the phase and neutral currents. Because of the large potential difference between the phase and neutral, two CTs (current transformers) must be used to provide the isolation. The CT turns ratio and burden resistor (Rb) are selected to give a peak differential voltage of ±660 mV/gain.

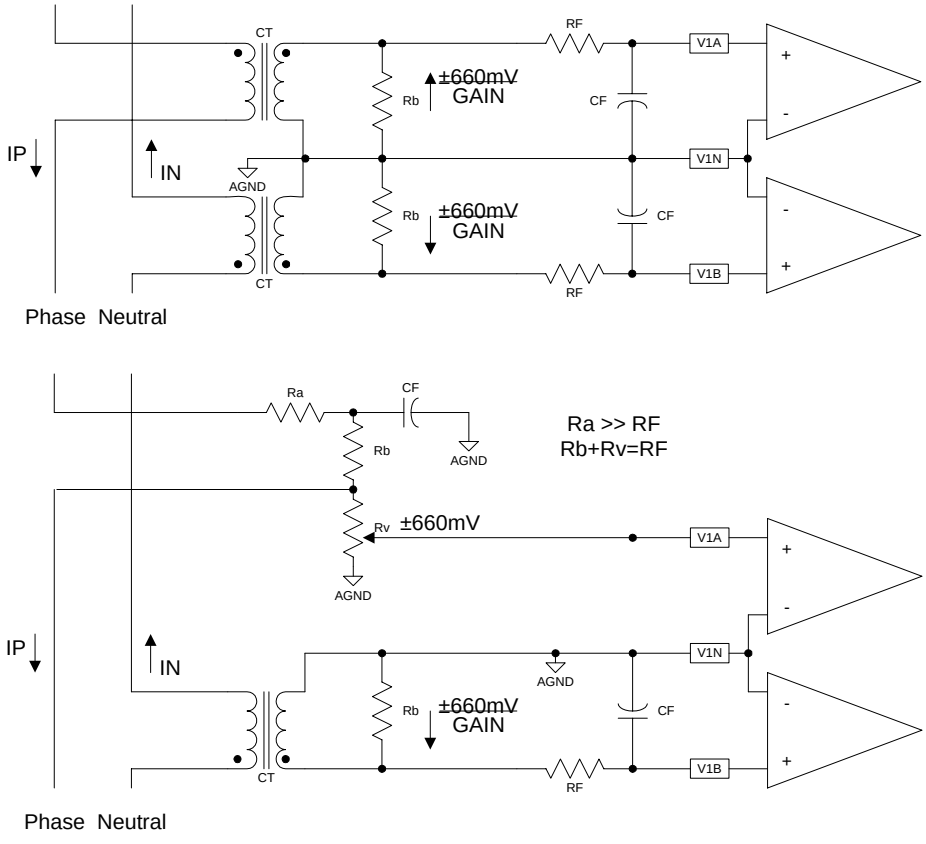



*Figure 7. Typical Connections for Current Channels*

## ◆ FAULT DETECTION

The BL6501A incorporates a novel fault detection scheme that warns of fault conditions and allows the BL6501A to continue accurate billing during a fault event. The BL6501A does this by continuously monitoring both the phase and neutral (return) currents. A fault is indicated when these currents differ by more than 12.5%. However, even during a fault, the output pulse rate on F1 and F2 is generated using the larger of the two currents. Because the BL6501A looks for a difference between the signals on V1A and V1B, it is important that both current transducers are closely matched. On power-up the output pulse rate of the BL6501A is proportional to the product of the signals on Channel V1A and Voltage Channel. If there is a difference of greater than 12.5% between V1A and V1B on power-up, the fault indicator (FAULT) will go active after about one second. In addition, if V1B is greater than V1A the BL6501A will select V1B as the input. The fault detection is automatically disabled when the voltage signal on Channel 1 is less than 0.5% of the full-scale input range. This will eliminate false detection of a fault due to noise at light loads.

If V1A is the active current input (i.e., is being used for billing), and the signal on V1B (inactive input) falls by more than 12.5% of V1A, the fault indicator will go active. Both analog inputs are filtered and averaged to prevent false triggering of this logic output. As a consequence of the filtering, there is a time delay of approximately one second on the logic output FAULT after the fault event. The FAULT logic output is independent of any activity on outputs F1 or F2. Figure 8 illustrates one condition under which FAULT becomes active. Since V1A is the active input and it is still greater than V1B, billing is maintained on VIA, i.e., no swap to the V1B input will occur. V1A remains the active input.

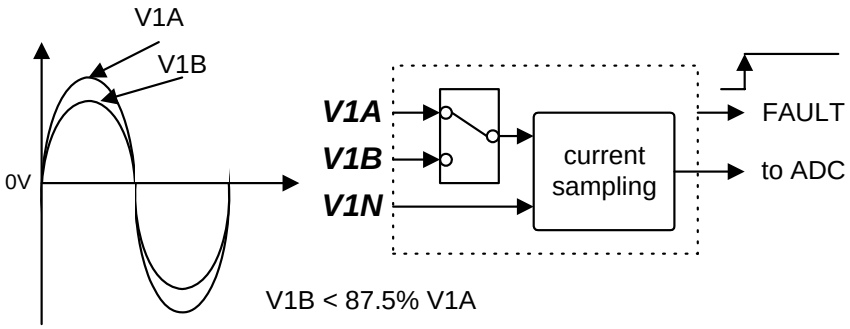



*Figure 8. Fault Conditions for Inactive Input Less than Active Input*

Figure 9 illustrates another fault condition. If V1A is the active input (i.e., is being used for billing) and the voltage signal on V1B (inactive input) becomes greater than 114% of V1A, the FAULT indicator goes active, and there is also a swap over to the V1B input. The analog input V1B has now become the active input. Again there is a time delay of about 1.2 seconds associated with this swap. V1A will not swap back to being the active channel until V1A becomes greater than 114% of V1B. However, the FAULT indicator will become inactive as soon as V1A is within 12.5% of V1B. This threshold eliminates potential chatter between V1A and V1B.

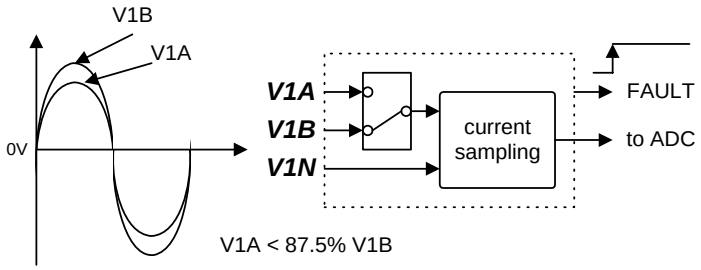



*Figure 9. Fault Conditions for Inactive Input Greater than Active Input*

### ◆ Power Supply Monitor

The BL6501A contains an on-chip power supply monitor. If the supply is less than 4V±5% then the BL6501A will go in an inactive state, i.e. no energy will be accumulated when the supply voltage is below 4V. This is useful to ensure correct device operation at power up and during power down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

The trigger level is nominally set at 4V, and the tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at VDD does not exceed 5V±5% as specified for normal operation.

### ◆ SLiM technology

The BL6501A adopts the technology of SLiM (Smart Low current Management) to decrease the static power greatly. The static power of BL6501A is about 12mW. It is half of the previous product BL0951 (about 25mW ).This technology also decreases the request for power supply design.

BL65XX series products used 0.35um CMOS process. The reliability and consistency are advanced.

## ◆ OPERATION MODE

### ◆ Transfer Function

The BL6501A calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low. It means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The average of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation. (use 3.58MHz oscillator)

$$Freq = \frac{5.74 \times V(v) \times V(i) \times gain \times F_Z}{V_{REF}^2}$$

Freq——Output frequency on F1 and F2 *(Hz)*

V(v)——Differential rms voltage signal on Channel 1 (volts)

V(i)——Differential rms voltage signal on Channel 2 (volts)

Gain——1, 2, 8 or 16, depending on the PGA gain selection, using logic inputs G0 and G1

Vref——The reference voltage (2.44 V±8%) (volts)

Fz——One of four possible frequencies selected by using the logic inputs S0 and S1.

| S1 | S0 | Fz(Hz) | XTAL/CLKIN |
|---|---|---|---|
| 0 | 0 | 1.7 | CLKIN/2^21 |
| 0 | 1 | 3.4 | CLKIN/2^20 |
| 1 | 0 | 6.8 | CLKIN/2^19 |
| 1 | 1 | 13.6 | CLKIN/2^18 |

## ◆ Frequency Output CF

The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 128 times the pulse rate on F1 and F2. The following Table shows how the two frequencies are related, depending on the states of the logic inputs S0, S1 and SCF.

| Mode | SCF | S1 | S0 | CF/F1 (or F2) |
|---|---|---|---|---|
| 1 | 1 | 0 | 0 | 128 |
| 2 | 0 | 0 | 0 | 64 |
| 3 | 1 | 0 | 1 | 64 |
| 4 | 0 | 0 | 1 | 32 |
| 5 | 1 | 1 | 0 | 32 |
| 6 | 0 | 1 | 0 | 16 |
| 7 | 1 | 1 | 1 | 16 |
| 8 | 0 | 1 | 1 | 8 |

Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Hence less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations.

## ◆ GAIN SELECTION

By select the digital input G0 and G1 voltage (5V or 0V), we can adjust the gain of current channel. We can see that while increasing the gain, the input dynamic range is decreasing.

| G1 | G0 | Gain | Maximum Differential Signal |
|---|---|---|---|
| 0 | 0 | 1 | ±660mV |
| 0 | 1 | 2 | ±330mV |
| 1 | 0 | 8 | ±82mV |
| 1 | 1 | 16 | ±41mV |

## ◆ ANALOG INPUT RANGE

The maximum peak differential signal on Voltage Channel is ± 660 mV, and the common-mode voltage is up to 100 mV with respect to AGND.

The analog inputs V1A, V1B, and V1N have the same maximum signal level restrictions as V2P and V2N. However, The Current Channel has a programmable gain amplifier (PGA) with user-selectable gains of 1, 2, 8, or 16. These gains facilitate easy transducer interfacing. The maximum differential voltage is ±660 mV and the maximum common-mode signal is ±100 mV.

The corresponding Max Frequency of CF/F1/F2 is shown in the following table.

| SCF | S1 | S0 | Fz | Max Frequency of F1, F2 (Hz) | | CF Max Frequency (Hz) | |
|---|---|---|---|---|---|---|---|
| | | | | DC | AC | DC | AC |
| 1 | 0 | 0 | 1.7 | 0.68 | 0.34 | 128×F1,F2=87.04 | 128×F1,F2=43.52 |
| 0 | 0 | 0 | 1.7 | 0.68 | 0.34 | 64×F1,F2=43.52 | 64×F1,F2=21.76 |
| 1 | 0 | 1 | 3.4 | 1.36 | 0.68 | 64×F1,F2=87.04 | 64×F1,F2=43.52 |
| 0 | 0 | 1 | 3.4 | 1.36 | 0.68 | 32×F1,F2=43.52 | 32×F1,F2=21.76 |
| 1 | 1 | 0 | 6.8 | 2.72 | 1.36 | 32×F1,F2=87.04 | 32×F1,F2=43.52 |
| 0 | 1 | 0 | 6.8 | 2.72 | 1.36 | 16×F1,F2=43.52 | 16×F1,F2=21.76 |
| 1 | 1 | 1 | 13.6 | 5.44 | 2.72 | 16×F1,F2=87.04 | 16×F1,F2=43.52 |
| 0 | 1 | 1 | 13.6 | 5.44 | 2.72 | 8×F1,F2=43.52 | 8×F1,F2=21.76 |

Notice： Sample tested during initial release and after any redesign or process change that may affect parameter. Specification subject to change without notice. Please ask for the newest product specification at any moment.