FEATURES

- High accuracy, less than 0.1% error over a dynamic range of 500:1
- High stability during calibration, the fluctuation of output CF is less than 0.1%.
- Low drift, the gain variety is less than 0.1% when input frequency changes from 45Hz to 65Hz
- Single 5V Supply, Static Power 25mW(typical), Power solution only with Resistor & Capacitor can be adopted.
- The Low Frequency Output (F1, F2) can drive motor directly;
- The High Frequency Output (CF) can be used in calibration and data processing.
- Selectable between the arithmetic sum of the three-phase active energies and the absolute value sum of these energies.
- Measure positive active power and negative active power.
- Anti-Fault, the Logic Output REVP indicates a Potential Miswiring or Negative Power for each phase.
- On-chip Creep Protection.
- On-chip Power Supply Monitoring.
- On-chip Reference 2.42V ± 8%,with External Overdrive Capability.
- SOP24 package.

Interrelated patents are pending

GENERAL DESCRIPTION

The BL0952A/BL6513/BL6511 is the chief IC of the three-phase electrical meter and a high accuracy energy measurement IC. With low power design, static power is only 25mW. Based on the features such as superior accuracy, high stability and simple peripheral circuit, the BL0952A/BL6513/BL6511 is compatible with 3-phase 3-wire and 3-phase 4-wire configurations.

BL0952A/BL6513/BL6511 is based on digital signal processing. BL0952A/BL6513/BL6511 can measure positive active power and negative active power; can select the way to calculate the sum of the three-phase active powers, between the arithmetic sum and the absolute value sum.

The high frequency output CF can be used in calibration and data processing. The low frequency outputs F1 and F2 can be used to drive a pulse-motor or an electromechanical counter. In this way, the power can be measured and the energy can be recorded.

The internal phase matching circuitry ensures that the current and voltage channels are phase matched.An internal no-load threshold ensures that the BL0952A/BL6513/BL6511 does not exhibit any creep when there is no load.

The BL0952A/BL6513/BL6511 consider emphatically the need of stability during calibration, the measure data of mass products show that the output pulse ripple of CF is less than 0.1%.

System Diagram Block

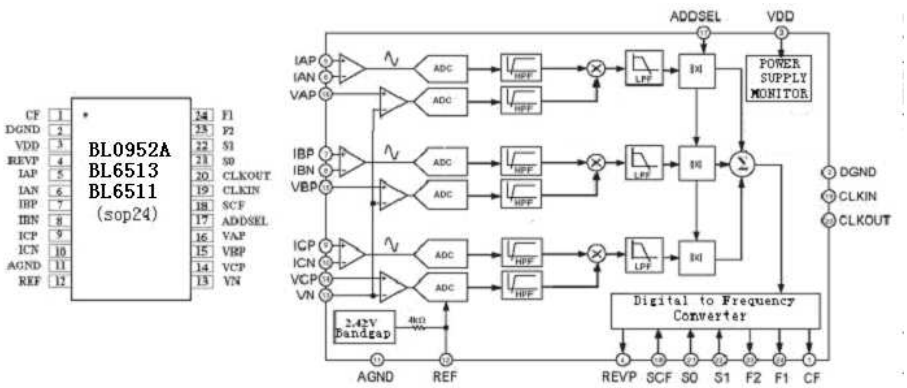


Fig.1 Functional block diagram

PIN FUNCTION DESCRIPTION

Pin No.	Mnemonic	Description
1	CF	High frequency calibration logic output. The output frequency is proportional to the average active power.
2	DGND	This provides the ground reference for the digital circuitry .
3	VDD	Power supply. This pin provides the supply voltage for the digital circuitry. The supply voltage should be maintained at 5V ± 5% for specified operation.
4	REVP	This logic output will go logic high when negative power is detected on any of the three phase inputs, i.e., when the phase angle between the voltage and the current signals is greater than 90°.
5,6; 7,8; 9,10	IAP,IAN; IBP,IBN; ICP,ICN	Analog inputs for current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±500mV
11	AGND	This pin provides the ground reference for the analog circuitry.
12	REF	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.42V ± 8% and a typical temperature coefficient of 30ppm/°C. An external reference source may also be connected at this pin.
13,14, 15,16	VN,VCP VBP,VAP	Analog inputs for the voltage channel. This channel is intended for use with the voltage VBP, VAP transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with maximum signal level of ±500mV with respect to VN for specified operation.
17	ADDSEL	The logic input is used to select the way the three active energies from the three phases are summed. This offers the designer the capability to do the arithmetic sum of the three energies (ADDSEL logic High) or the sum of the absolute value (ADDSEL logic low).
18	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF.
19	CLKIN	Master clock for ADCs and digital signal processing. An external clock can be provided at this logic input.3.58MHz
20	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source.
21,22	S0,S1	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter.
23,24	F1,F2	Low Frequency Logic Outputs. F1 and F2 supply average real power information. The logic outputs can be used to directly drive electromechanical counters and two-phase stepper motors.

PACKAGE DIMENSIONS

24 PIN SOP

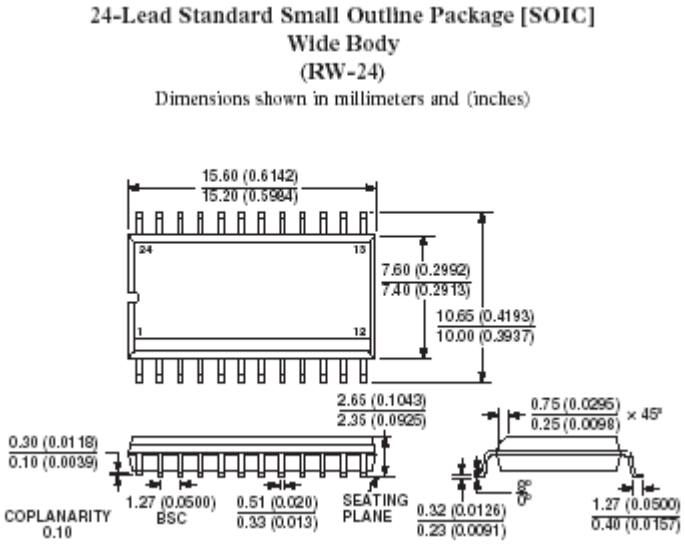


Fig.2 Package of BL0952A/BL6513/BL6511

Absolute Maximum Ratings

(T = 25℃)

Item	Symbol	Extremum	Unit
Power Voltage VDD	VDD	-0.3~+7(max)	V
Input Voltage to AGND	V_V	-VDD+0.5≤V_V≤VDD-0.5	V
Input Current to AGND	V_I	-VDD+0.5≤V_I≤VDD-0.5	V
Operating Temperature Range	Topr	-40~+85	℃
Storage Temperature Range	Tstr	-55~+150	℃
Power Dissipation（SOP24）		80	mW

Electronic Characteristic Parameter

(T=25℃, VDD=5V, CLKIN=3.58MHz)

Parameter	Symbol	Test Condition	Measure Pin	Min Value	Typical Value	Max Value	Unit
1 Power Current	I_{VDD}		Pin3			8	mA
2 Logic Input Pins SCF,S0,S1, ADDSEL			Pin17, 18,21,22				
Input High Voltage	V_{IH}	VDD=5V		3			V
Input Low Voltage	V_{IL}					1	V
Input Capacitance	C_{IN}				10		pF
3 Logic Output Pins F1/F2			Pin23,24				
Output High Voltage	V_{OH1}	I_H=10mA		4.4			V
Output Low Voltage	V_{OL1}	I_L=10mA				0.5	V

Output Current	I_{O1}				10		mA
4 Logic Output Pins REVP, CF			Pin1,4				
Output High Voltage	V_{OH2}	I_H=10mA		4.4			V
Output Low Voltage	V_{OL2}	I_L=10mA				0.5	V
Output Current	I_{O2}				5		mA
5 On-chip Reference	Vref	VDD=5V	Pin12		2.42		V
Temperature Coefficient					30		ppm/°C
6 Analog Input Pins IAP,IAN,IBP,IBN,ICP,ICN, VN,VCP,VBP,VAP			Pin5,6,7, 8,9,10,13 ,14,15,16				
Maximum Input Voltage	V_{AIN}				±500		mV
DC Input Impedance					330		Kohm
Input Capacitance				6		10	pF
ADC offset	Voff				±15		mV
7 Accuracy							
Measurement Error on Current Channel CFA,CFB,CFC,CF		Input on the voltage channel, ±500mVrms The dynamic range 500:1	Pin1		0.1		%
Phase Error between Channels							
Channel 1 Lead 37°C (PF=0.8Capacitive)			Pin1		0.1		Degrees
Channel 1 Lags 60°C (PF=0.5Inductive)			Pin1		0.1		Degrees
8 Start Current	I_{START}	Ib=5A C=800,cosφ=1̃, Voltage Channel Inputs ±110mVrms	Pin5,6,7, 8,9,10		0.2%Ib		A
9 Positive and Negative Real Power Error (%)	ENP	Vv=±110mVrms ,V(I)=50mVrms, cosφ=±1	Pin1		0.1		%
10 Gain Error	Gain error	Internal reference.	Pin1		±5	±9	%
11 Power Supply Monitor Voltage	V_{down}	Power Supply vary from 3.5V to 5V, and Current Channel with Full-Scale Signal			4		V

◆ **TERMINOLOGY**

1) MEASUREMENT ERROR

The error associated with the energy measurement made by the BL0952A/BL6513/BL6511 is defined by the following formula:

$$Pencentage\ Error = \frac{Energy\ \ Registered\ by\ the\ BL6513 - True\ Energy}{True\ Energy} \times 100\%$$

2) NONLINEAR ERROR

The Nonlinear Error is defined by the following formula:

eNL%＝[（Error at X-Error at Ib）/(1+Error at Ib)]*100%

When V(V)= ±110mV, cosφ=1, over the arrange of 5%Ib to500%Ib, the nonlinear error should be less than 0.1%.

3) POSITIVE AND NEGATIVE REAL POWER ERROR

When the positive real power and the negative real power is equal, and V(V) =±110mV, the test current is Ib, then the positive and negative real power error can be achieved by the following formula:

eNP%=|[(eN%-eP%)/(1+eP%)]*100%|

Where: eP% is the Positive Real Power Error; eN% is the Negative Real Power Error.

4) START-UP CURRENT

When Ib=5A,C=800,cosφ=1,Voltage Channel Input ±110mV rms, 5％Ib error in normal range, the min AC current in current loop.

5) GAIN ERROR

The gain error of the BL0952A/BL6513/BL6511 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the BL0952A/BL6513/BL6511 transfer function.

6) POWER SUPPLY MONITOR

BL0952A/BL6513/BL6511 has the on-chip Power Supply monitoring The BL0952A/BL6513/BL6511 will remain in a reset condition until the supply voltage on VDD reaches 4 V. If the supply falls below 4 V, the BL0952A/BL6513/BL6511 will also be reset and no pulses will be issued on F1, F2 and CF.

Timing Characteristics

(VDD=5V, AGND=DGND=0V, on chip Reference, CLKIN=3.58MHz, T_{MIN} to T_{MAX} = -40~+85°C)

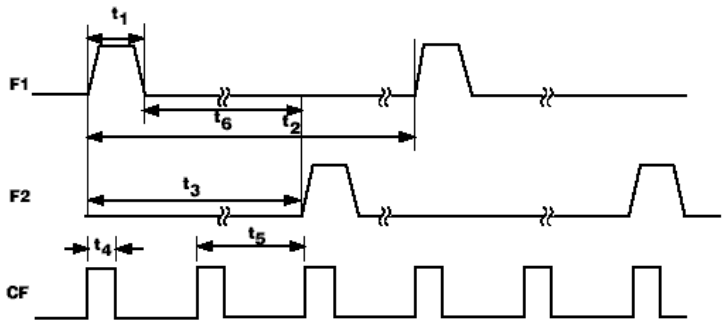


Fig.3 time characteristics of CF, F1 and F2

Parameter	Value	Description
T1	145ms	Pulse-width (Logic High) of F1 or F2. At small load, the pulse-widths of F1 and F2 are specified as 145ms. When the power is high, the output periods of F1 and F2 is less than 290ms, and the pulse-widths of F1 and F2 equal half of the F1 period.
T2		The low output pulse period. (see the formula of operation)
T3	1/2 t2	Time between F1 Rising Edge and F1 Rising Edge.
T4	90ms	CF Pulse-width. At small load, the pulse-width of CF is specified as 90ms. When the power is high, the output period of CF is less than 180ms, and the pulse-width of CF equals half of the CF period.
T5		CF output high frequency. (see the relative between CF and F1, F2)
T6	CLKIN/4	Minimum time between F1 and F2 pulse.

Notes

1) CF is not synchronous to F1 or F2 frequency outputs.

2) Sample tested during initial release and after any redesign or process change that may affect this parameter.

BASIC THEORY OF OPERATION

◆ ENERGY MEASURE THEORY

In energy measure, the power information varying with time is calculated by a direct multiplication of the voltage signal and the current signal. Assume that the current signal and the voltage signal are cosine functions; Umax, Imax are the peak values of the voltage signal and the current signal; w is the angle frequency of the input signals; the phase difference between the current signal and the voltage signal is expressed as φ. Then the power is given as follows:

$$p(t) = U_{\max}\cos(wt) \times I_{\max}\cos(wt+\varphi)$$

If $\varphi = 0$: $p(t) = \frac{U_{\max} I_{\max}}{2}[1+\cos(2wt)]$

If $\varphi \neq 0$:

$$
\begin{aligned}
&p(t) = U_{max}\cos(\omega t) \times I_{max}\cos(\omega t + \Phi) \\
&= U_{max}\cos(\omega t) \times [I_{max}\cos(\omega t)\cos(\Phi) + I_{max}\sin(\omega t)\sin(\Phi)] \\
&= \frac{U_{max}I_{max}}{2}[1+\cos(2\omega t)]\cos(\Phi) + U_{max}I_{max}\cos(\omega t)\sin(\omega t)\sin(\Phi) \\
&= \frac{U_{max}I_{max}}{2}[1+\cos(2\omega t)]\cos(\Phi) + \frac{U_{max}I_{max}}{2}\sin(2\omega t)\sin(\Phi) \\
&= \frac{U_{max}I_{max}}{2}\cos(\Phi) + \frac{U_{max}I_{max}}{2}[\cos(2\omega t)\cos(\Phi) + \sin(2\omega t)\sin(\Phi)] \\
&= \frac{U_{max}I_{max}}{2}\cos(\Phi) + \frac{U_{max}I_{max}}{2}\cos(2\omega t + \Phi)
\end{aligned}
$$

$p(t)$ is called as the instantaneous power signal. The ideal $p(t)$ consists of the dc component and ac component whose frequency is $2w$. The dc component is called as the average active power, that is:

$$P = \frac{U_{max}I_{max}}{2}\cos(\varphi)$$

The average active power is related to the cosine value of the phase difference between the voltage signal and the current signal. This cosine value is called as Power Factor (PF) of the two channel signals.

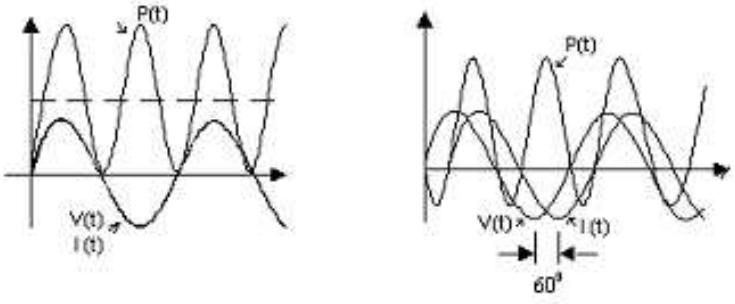


Fig.4 The Effect of phase

When the phase difference between the voltage signal and the current signal is more than 90°, the average active power is negative. This case indicates the user is using the electrical energy reversely.

The main function of the three phase measurement IC is calculating the sum of the three phase active power (the arithmetic sum or the absolute value sum), and supplying the frequency signals proportional to the active powers.

If the BL0952A/BL6513/BL6511 is configured to execute the arithmetic sum of the three active powers, the sum of the three-phase power is calculated as follows:

$$P_{TOTAL} = P_A + P_B + P_C$$

When one phase power of three phases is negative, it's value will counteract the other positive terms.

If the BL0952A/BL6513/BL6511 is configured to execute the absolute value sum of the three active powers, the sum of the three-phase power is calculated as follows:

$$P_{TOTAL} = |P_A| + |P_B| + |P_C|$$

◆ THE OPRATION PROCESS OF THREE PHASE ENERGY MEASURE SIGNAL

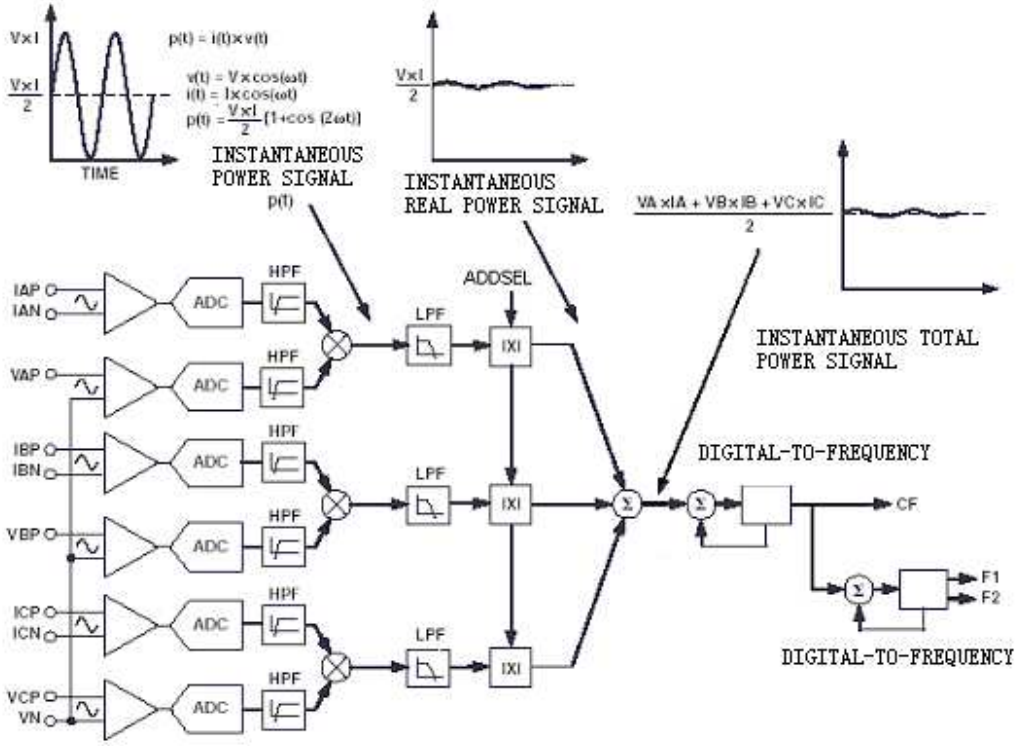


Fig.5 Signal Processing Block Diagram

In BL0952A/BL6513/BL6511, the six voltage signals from the current and voltage transducers are digitized with ADCs. The instantaneous power signal P(t) is generated by a direct multiplication of the current and voltage signals of each phase. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered on each phase. Then, The total real power information is then obtained by adding the individual phase real power (the arithmetic sum or the absolute value sum).

The output of three-phase power sum is sent to the digital-frequency module. In this module, the total real power is accumulated during the given time, and converted to the periodic frequency output which is therefore proportional to the average real power. Because of its high output frequency and therefore, shorter integration time, the CF output is proportional to the instantaneous real power. This pulse is useful for system calibration purposed that would take place under steady load conditions.

By dividing the high output CF, F1 and F2 can be obtained. The outputs F1 and F2 operate at a much lower frequency, which can drive the 2-phase stepper motors by eight kinds modes. The

output pulse is given to the counter motor out of the chip, and then the counter value proportional to the consumed energy is obtained.

◆ **Offset Effect**

The dc offsets come from the input signals and the forepart analog circuitry.

Assume that the input dc offsets on the voltage channel and the current channel are U_{offset} and I_{offset}, and PF equals 1 ($\varphi = 0^\circ$).

$$p(t) = [U\cos(\omega t) + U_{offset}] \times [I\cos(\omega t + \Phi) + I_{offset}]$$
$$= \frac{UI}{2} + I_{offset}U\cos(\omega t) + U_{offset}I\cos(\omega t) + \frac{UI}{2}\cos(2\omega t)$$

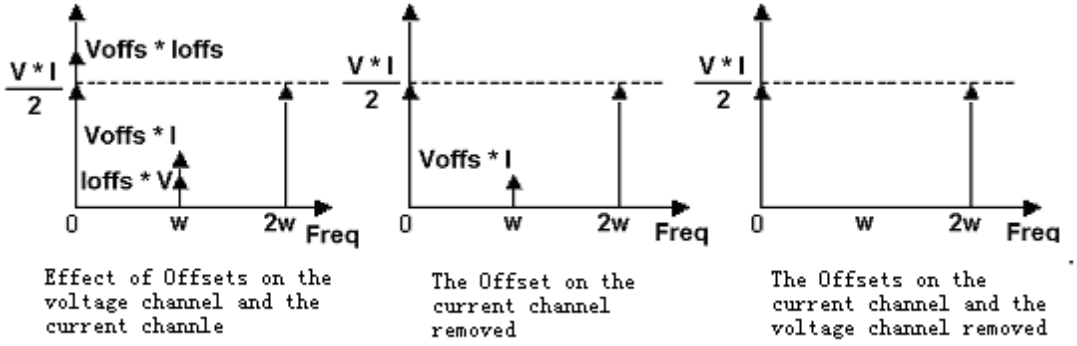


Fig.6 Effect of different offset cancellation methods

As can be seen, for each phase input, if there are simultaneous dc offsets on the voltage channel and the current channel, these offsets contribute a dc component for the result of multiplication. That is, the offsets bring the error of $U_{offset} \times I_{offset}$ to the final average real power. Additionally, there exists the component of $U_{offset} \times I + I_{offset} \times U$ at the frequency of w. The dc error on the real power will result in measure error, and the component brought to the frequency of w will also affect the output of the average active power when the next low-pass filter can't restrain the ac component very completely.

When the offset on the one of the voltage and the current channels is filtered, for instance, the offset on the current channel is removed; the result of multiplication is improved greatly. There is no dc error, and the additional component at the frequency of w is also decreased.

When the offsets on the voltage channel and the current channel are filtered respectively by two high-pass filters, the component at the frequency of w (50Hz) is subdued, and the stability of the output signal is advanced. Moreover, in this case, the phases of the voltage channel and the current channel can be matched completely, and the performance when PF equal 0.5C or 0.5L is improved. In BL0952A/BL6513/BL6511, this structure is selected. Though it is given in the system specification that the ripple of the output signal is less than 0.1%, in real measure of BL0952A/BL6513/BL6511, the calibration output is very stable, and the ripple of the typical output signal is less than 0.05%.

Additionally, this structure can ensure the frequency characteristic. When the input signal changes from 45Hz to 65Hz, the complete machine error due to the frequency change is less than 0.1%. In such, the meter designed for the 50Hz input signal can be used on the transmission-line system of electric power whose frequency is 60Hz.

◆ Current Channels

The voltage outputs from the current transducers are connected to the BL0952A/BL6513/BL6511 current channels, which are fully differential voltage inputs. IAP, BP, and ICP are the positive input for IAN, IBN, and ICN, respectively. The maximum peak differential signal on the current channel should be less than $\pm 500mV$ ($353mV$ rms for a pure sinusoidal signal) for the specified operation.

Fig.7 shows a typical connection diagram for the one current channel (IA).

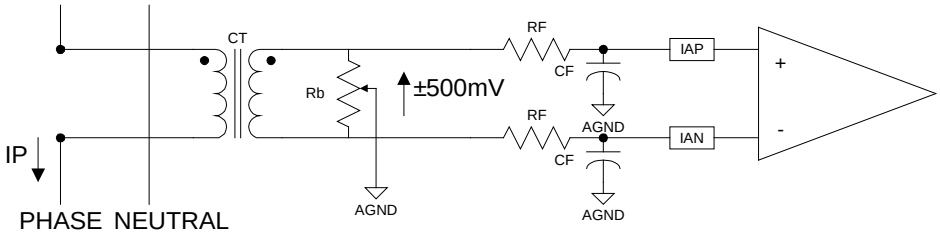


Fig.7 Typical Connection for Current Channels

◆ Voltage Channels

The output of the line voltage transducer is connected to the BL0952A/BL6513/BL6511 at this analog input. Voltage channels are a pseudo-differential voltage input. VAP, VBP, and VCP are the positive inputs with respect to VN. The maximum peak differential signal on the voltage channel is $\pm 500mV$ ($353mV$ rms for a pure sinusoidal signal) for the specified operation.

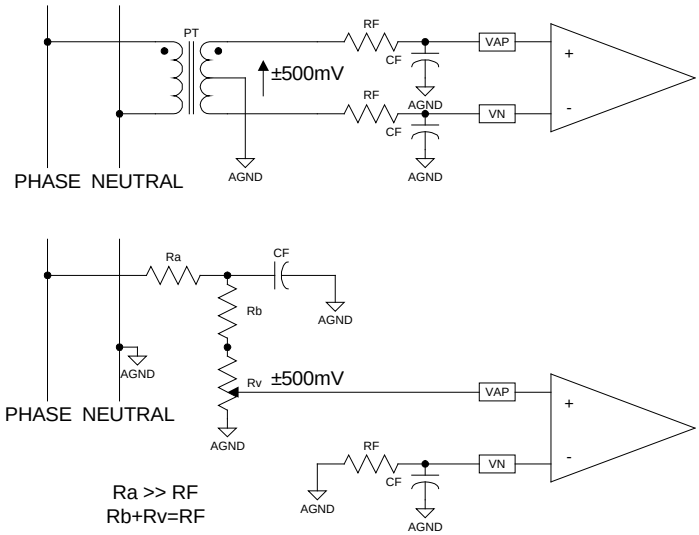


Fig.8 Typical Connections for Voltage Channels

Notes: Because of the various external devices, the current channel and the voltage channel may have the phase match error (mainly due to different RC constant and different phase delay).

By adjusting the external capacitor Cf, the phase error can be corrected. The phase error will affect the system gain when PF is 0.5, and bring error.

The process of BL0952A/BL6513/BL6511 can ensure the consistent compensatory value.

◆ Power Supply Monitor

The BL0952A/BL6513/BL6511 contains an on-chip power supply monitor. If the supply is less than $4V \pm 5\%$ then the BL0952A/BL6513/BL6511 will go in an inactive state, i.e. no energy will be accumulated when the supply voltage is below 4V. This is useful to ensure correct device operation at power up and during power down. The power supply monitor has built-in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

The trigger level is nominally set at 4V, and the tolerance on this trigger level is about $\pm 5\%$. The power supply and decoupling for the part should be such that the ripple at V_{DD} does not exceed $5V \pm 5\%$ as specified for normal operation.

◆ Digital-To-Frequency Conversion

After multiplication，the low-pass filter is used to attenuate the ac components at the line frequency and its harmonics. Then the three phase real powers are sent to the adder, and the arithmetic sum or the absolute value sum (selectable by the pin ADDSEL) can be obtained. The power sum is passed to the digital-to-frequency converter. In the digital-to-frequency, the power signal is integrated over time to produce an output frequency. This accumulation of the signal will suppress any non-dc component in the instantaneous real power signal. Because the average value of a sinusoidal signal is zero, the frequency generated by the digital-to-frequency is proportional to the average real power.

Figure 9 shows the calculating process of the output CF:

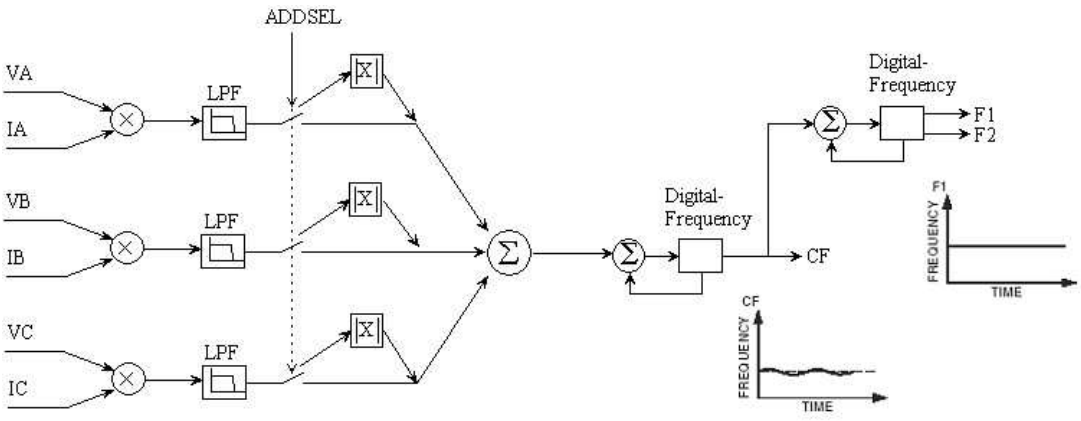


Fig.9 Real Power-to-Frequency Conversion

As can be seen in the diagram, the output frequency CF is generated by accumulating the instantaneous real power signal over a much shorter time, while converting it to a frequency. Due to the short accumulating time, there are still ripple in the CF. This will not be a problem in the application. Where CF is used for calibration purposes, the frequency should be averaged by the frequency counter. This will remove any ripple. After the output frequency CF, by other digital-to-frequency converter, the lower output frequency F1 and F2 are obtained. Because the outputs F1 and F2 operate at a much lower frequency, much more averaging of the instantaneous

real power signal is carried out. Thus the stability of the output frequency is ensured.

◆ Mode Selection of the Sum of the Three Active Energies

The BL0952A/BL6513/BL6511 can be set to execute the arithmetic sum of the three active energies,

$$Wh = Wh_{\phi A} + Wh_{\phi B} + Wh_{\phi C}$$

Or the sum of the absolute value of these energies,

$$Wh = \left|Wh_{\phi A}\right| + \left|Wh_{\phi B}\right| + \left|Wh_{\phi C}\right|.$$

The selection between the two modes can be made by setting the ADDSEL pin. Logic high and logic low applied on the ADDSEL pin correspond to the arithmetic sum and the sum of absolute values, respectively.

◆ Anti-Creep Threshold

In BL0952A/BL6513/BL6511, when the rms of current and the rms of voltage are 500mV, the anti-creep threshold is set as the 0.0020 percent of full-scale power. There are anti-creep logics in three phase circuits.

SCF	S0	S1	Min Freq On F1/F2 For AC input [Hz]	Min Freq On CF For AC input [Hz]
1	1	1	9.76E-06	1.56E-04
0	0	0	1.56E-05	2.50E-03
1	0	0	1.95E-05	1.56E-04
0	0	1	3.13E-04	5.00E-03
1	0	1	3.13E-04	2.50E-03
0	1	0	6.25E-05	1.00E-02
1	1	0	7.81E-05	1.25E-03
0	1	1	1.25E-03	1.00E-02

OPERATION MODE

◆ FORMULA of OPERATION

In the BL0952A/BL6513/BL6511, the output frequency or pulse rate is related to the input voltage signals by the following equation:

$$Freq = \frac{13.25 \times \left(U_{AP} \times I_A + U_{BP} \times I_B + U_{CP} \times I_C\right) \times F_{1-5}}{V_{REF}^2}$$

$Freq$ = Output frequency on F1 and F2 (Hz)

U_{AP}, U_{BP}, U_{CP} = Differential rms voltage signal on voltage channels (volts)

I_A, I_B, and I_C = Differential rms voltage signal on current channels (volts)

V_{ref} = The reference voltage (2.42 V ± 8%) (volts)

$F_{1\text{-}5}$ = One of five possible frequencies selected by using the logic inputs SCF, S0, and S1.

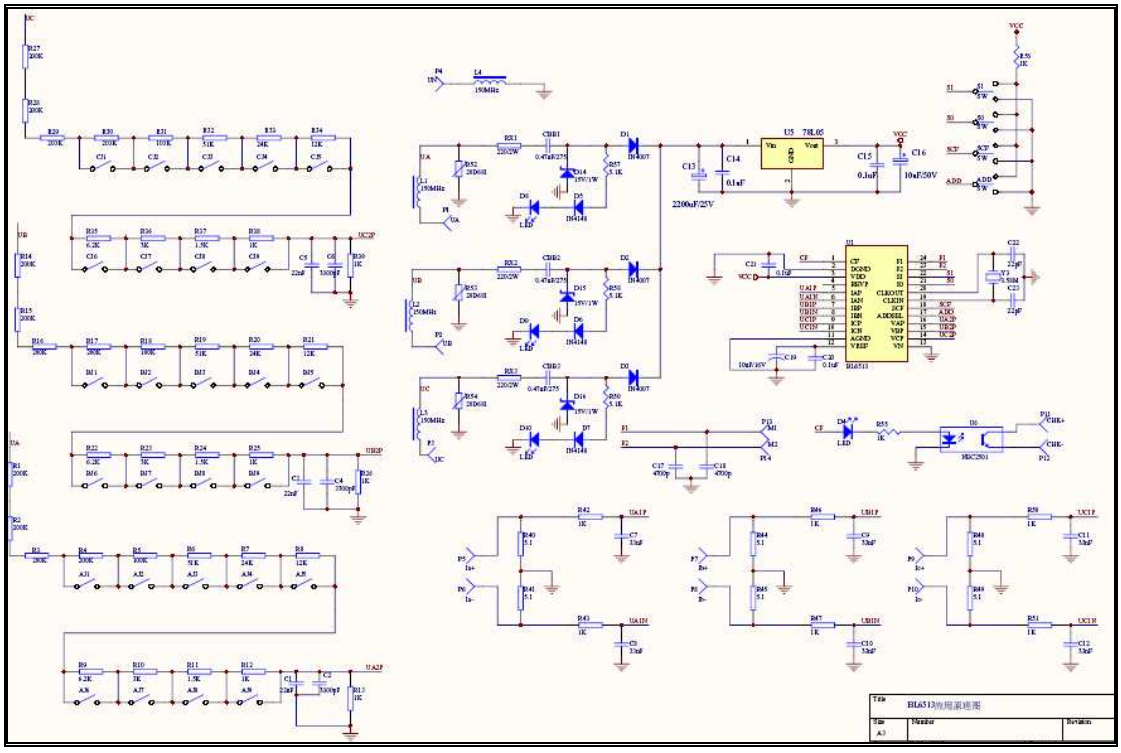
◆ Selecting the operation mode

In BL0952A/BL6513/BL6511, the different operation modes can be selected by the input SCF, S0 and S1. Table I shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF.

SCF	S0	S1	F1-5	Max Freq On F1/F2 For AC input[Hz]	CF vs. F1/F2	Max Freq On CF For AC input[Hz] ①
1	1	1	0.575	0.488	16	7.8
0	0	0	0.921	0.781	160	125
1	0	0	1.150	0.976	8	7.8
0	0	1	18.42	15.625	16	250
1	0	1	18.42	15.625	8	125
0	1	0	3.683	3.125	160	500
1	1	0	4.604	3.906	16	62.5
0	1	1	73.67	62.5	8	500

① The frequency of output CF when input current and Voltage are ± 500mV AC signal.

Application circuit



Notice: Sample tested during initial release and after any redesign or process change that may affect parameter. Specification subject to change without notice. Please ask for the newest product specification at any moment.