BL6552
Professional chip for three phase power monitoring and analysis
Data Sheet

V1.12

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1、 Product description

BL6552 is a 7-channel three-phase power monitoring and analysis chip, which is suitable for three-phase intelligent circuit breaker, three-phase guide rail meter, electrical measuring instrument, power supply monitoring of high-power equipment and other applications, with high cost performance.

BL6552 integrates seven high-precision Sigma-Delta ADCs, reference voltage circuits, temperature sensors and other analog circuit modules, as well as digital signal processing circuits for processing power, effective value, energy, temperature and other electrical parameters. It can be used to measure the total (fundamental and harmonic) active power and energy, reactive power and energy, apparent power and energy of three-phase split and combined phase; and fundamental active power and energy, reactive power and energy; And each phase current, voltage effective value, power factor and other parameters; with current loss monitoring, current and voltage peak detection, zero-crossing detection and other power quality management; can give real-time waveforms.

BL6552 integrates SPI and UART interfaces to facilitate the transfer of metering parameters and calibration parameters with an external MCU.

BL6552 internally uses data flow calculation method to process various signals, and it has good reliability in the case of external interference. The internal power supply voltage monitoring circuit can ensure normal operation during power-up and power-off.

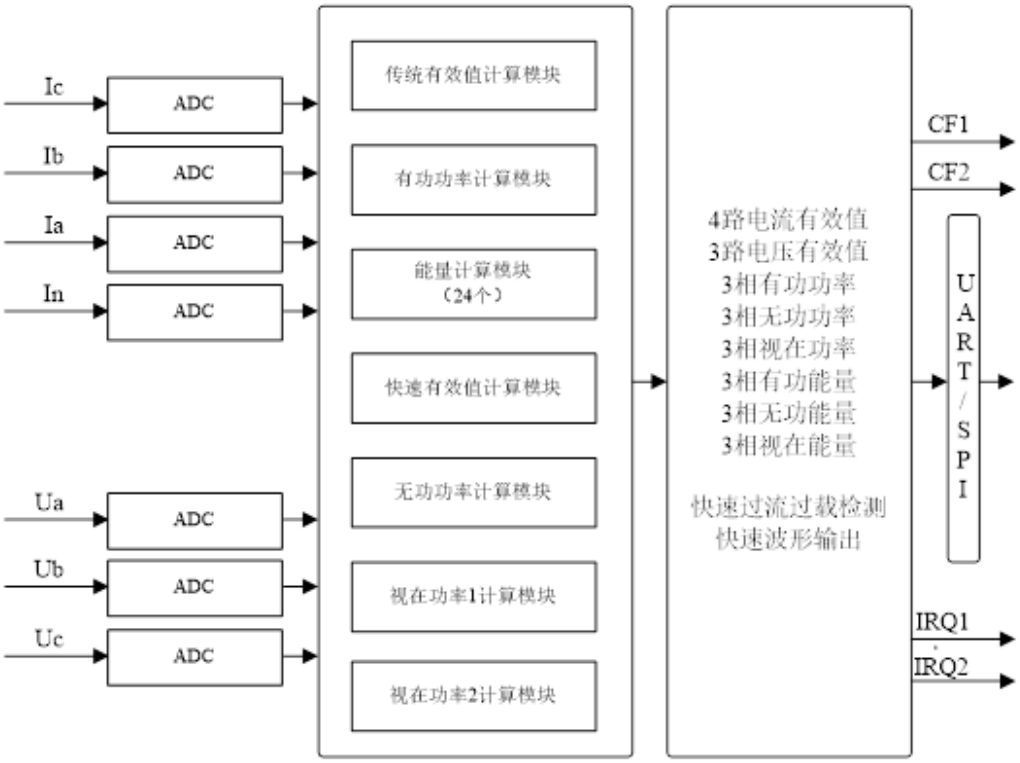
2、 Basic Features

2.1 Main feature

- ✓ High-precision, 8000:1 input dynamic range of active energy measurement nonlinear error <0.1%
- ✓ High stability, non-linear error of reactive energy measurement within the input dynamic range of 8000:1 <0.1%
- ✓ Provide neutral current measurement
- ✓ Provide split-phase and total (fundamental and harmonic) active, reactive, and apparent power (24bit, supporting two calculation methods); and fundamental active and reactive power (24bit)
- ✓ Provide the effective value of split-phase voltage and current (24bit), and the relative error within the detection range of 3000:1 is less than 0.1%
- ✓ Provide waveform sampling data of split-phase voltage, current and neutral current (24bit)
- ✓ Provide total (fundamental and harmonic) active, reactive, and apparent energy (24bit)
- ✓ Provide total (fundamental and harmonic) active and reactive line cycle energy
- ✓ Provide total (fundamental and harmonic) positive and negative active energy
- ✓ Provide the combined and four-quadrant reactive energy
- ✓ Provides 300 real-time waveforms per week
- ✓ Provide split-phase and combined-phase power factor
- ✓ With fast effective value output
- ✓ Provide voltage and current phase angle measurement
- ✓ Fast pulse output with active energy and reactive energy
- ✓ With voltage loss and phase failure detection function
- ✓ With current loss detection function
- ✓ With current and voltage peak detection and zero-crossing detection functions
- ✓ With voltage line frequency detection
- ✓ Programmable anti-creep threshold setting
- ✓ Programmable adjustment of pulse output frequency
- ✓ Programmable active power, reactive power, apparent power error and gain adjustment
- ✓ Programmable input active phase compensation

- ✓ The interrupt request signal can be given as needed to facilitate the control with the external MCU
- ✓ With UART/SPI communication interface for easy data transmission
- ✓ Built-in reference voltage source
- ✓ Single power supply 3.3V
- ✓ QFN36 PACKAGE

2.2 System Block Diagram



三相电能监测及分析专用芯片

It is mainly divided into analog signal processing and digital signal processing. The analog part mainly includes 7-channel high-precision Sigma-Delta ADC and related analog modules, and the digital part is a digital signal processor and related modules.

2.3 Pin arrangement

QFN36 PACKAGE

Serial number	Name	Input output	Description
1	INP	input	Positive terminal input of neutral current channel
2	VREF	input output	The reference voltage output pin is connected with a 0.1uF filter capacitor.
3	VAN	input	A phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
4	VAP	input	A phase voltage channel positive terminal input
5	VBN	input	B-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
6	VBP	input	B-phase voltage channel positive terminal input
7	VCN	input	C-phase voltage channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
8	VCP	input	C-phase voltage channel positive terminal input
9	NRST	input	Reset, active low
10	AGND	Power ground	Analog ground
11	DGND	Power ground	Digital ground
12	CS	input	SPI chip selection/UART rate selection
13	SDO	output	SPI/UART transmit data pin
14	SDI	input	SPI/UART receive data pin
15	SCLK	input	SPI clock input/UART rate selection
16	IRQ1	output	Interrupt status logic output 1
17	IRQ2	output	Interrupt status logic output 2
18	CLKOUT	output	Crystal oscillator pin
19	CLKIN	input	Crystal oscillator pin，external crystal oscillator frequency 8MHz
20	VPP	power supply	Reserved, can be left floating
21	CF1	output	Calibration pulse 1 (active power)
22	CF2	output	Calibration pulse 2 (reactive power)
23	AT1	output	Logic output pin, configurable output indication 1
24	AT2	output	Logic output pin, configurable output indication 2
25	AT3	output	Logic output pin, configurable output indication 3

26	DVDD18	output	Digital module voltage 1.8V, external 0.1uF filter capacitor
27	SEL	input	Default 0, select Uart; 1, select SPI
28	DVDD	power supply	Power supply 3.3V
29	AVDD	power supply	Power supply 3.3V
30	ICN	input	C-phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
31	ICP	input	C-phase current channel positive terminal input
32	IBN	input	B-phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
33	IBP	input	B-phase current channel positive terminal input
34	IAN	input	A phase current channel negative terminal input, the maximum differential voltage of each pair of pins is ±0.7V
35	IAP	input	A phase current channel positive terminal input
36	INN	input	Negative terminal input of the neutral current channel, the maximum differential voltage of each pair of pins is ±0.7V

Remarks: The maximum differential voltage of the analog input pins refers to the channel 1 times gain, if other gains are set, the maximum differential voltage of the channel will be reduced accordingly;

2.4 Performance indicators

2.4.1 Electrical parameter performance index

Parameter	Symbol	Test Condition	Measure Pin	Min	Typ	Max	Unit
Active power measurement error	$WATT_{ERR}$	8000:1 input DR			0.1		%
Reactive power measurement error	VAR_{ERR}	8000:1 input DR			0.1		%
Phase angle between channels causes measurement errors (PF=0.8 capacitive) (PF=0.5 inductive)	$PF08C_{ERR}$ $PF05L_{ERR}$	Phase lead 37° Phase lag 60°			0.1 0.1		% %
AC power supply suppression (variation of output frequency amplitude) DC power supply suppression	AC_{PSRR} DC_{PSRR}	Current channel current input pin IP\IN@100mV, voltage channel input pin VP\VN=100mV			0.01 0.1		% %

(variation of output frequency amplitude)							
Voltage RMS measurement accuracy, relative error	$VRMS_{ERR}$	3000:1 input DR			0.1		%
Current RMS measurement accuracy, relative error	$IRMS_{ERR}$	3000:1 input DR			0.1		%
Analog input input level (peak value) input resistance Signal bandwidth (-3dB) Gain error Phase gain matching error		PGA=1 Differential input External 1.2 reference voltage External 1.2 reference voltage		 370 	 14 0.5 0.3	700 	mV kΩ kHz % %
Internal voltage reference temperature coefficient	Vref TempCoef				1.097 20		V ppm/℃
Logic input pin Input high level Input low level		NRST、SDI、SCLK、/CS DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		 0.8	 V V
Logic output pin Output high level Output low level		SDO、CF1、CF2、AT1、AT2、AT3 DVDD=3.3V±2.5% DVDD=3.3V±2.5%		2.6		 1	 V V
power supply AVDD、DVDD DVDD18 AVDD DVDD	 V_{AVDD} V_{DVDD18} I_{AVDD} I_{DVDD}	 AVDD=3.3 DVDD=3.3		 3 1.6	 3.3 1.8 6 6	 3.6 2 9 9	 V V mA mA

2.4.2 Limit range

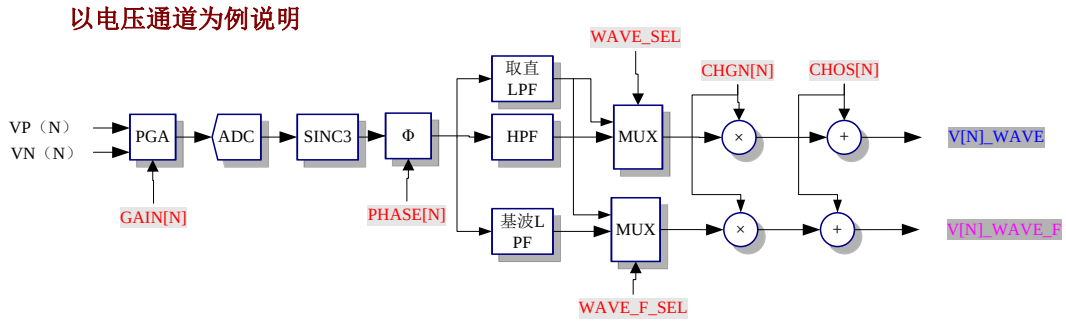
（T = 25 ℃）

Project	Symbol	Extremum	Unit
Power supply voltage VDD	AVDD、DVDD	-0.3 ~ +4	V
Power supply voltage DVDD18	DVDD18	-0.3 ~ +2.5	V

Analog input voltage (relative to GND)	ICN、ICP、IBN、IBP、IAN、IAP、INN、INP、VCN、VCP、VBN、VBP、VAN、VAP	-1 ~ +AVDD	V
Analog output voltage (relative to GND)	VREF	-0.3 ~ +AVDD	V
Digital input voltage (relative to GND)	SEL、NRST、SDI、SCLK、/CS、SEL	-0.3 ~ AVDD+0.3	V
Digital output voltage (relative to GND)	CF1、CF2、SDO	-0.3 ~ AVDD+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstr	-55 ~ +150	℃
Power consumption （QFN36）	P	200	mW

3、 Working principle

3.1 Principle of current and voltage waveform generation



There are 7 high-precision ADCs in total, using double-ended differential signal input: channel N input signal VP[N] and VN[N]. 7 waveform outputs, including 4 currents and 3 voltages. In each channel (the current and voltage are the same), the input signal passes the analog module amplifier (PGA) and high-precision analog-to-digital conversion (ADC) to get 1bit PDM to the digital module. The digital module undergoes phase calibration and down-sampling filter (SINC3), optional high-pass filter (HPF) or fundamental wave low-pass filter, through gain and offset correction modules, to obtain the required current waveform data and voltage waveform data (I[N]_WAVE, V[N]_WAVE).

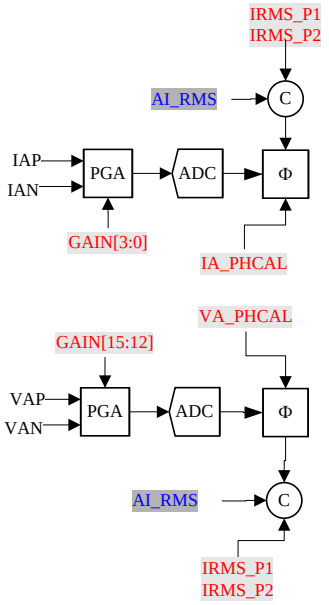
7-channel PGA gain is adjustable (0000=1 times; 0001=2 times; 0010=8 times; 0011=16 times), see GAIN register for adjustment

Address	Name	Bit width	Defaults	Description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register: [11:8]: C-phase current [15:12]: B-phase current [19:16]: Phase A current [23:20]: Neutral line current
61	GAIN2	20	0x00000	Channel PGA gain adjustment register: [11:8]: Phase A voltage [15:12]: Phase B voltage [19:16]: Phase C voltage

3.1.1 Active phase compensation

The chip provides a method for digital calibration of small phase errors. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Since this compensation needs to be timely, this method is only suitable for small phase errors in the range of <0.574°.

Since the transformer at the analog input terminal may have inconsistent angle differences when input signals of different amplitudes, increase the angle differential section compensation setting and allow three-section angle differential compensation.



Current channel angle differential segment definition register:

Address	Name	Bit width	Defaults	Description
62	IRMS_P1	24	0x010000	The angle difference segment point defines P1, which satisfies IRMSmin<P1<P2<IRMSmax
63	IRMS_P2	24	0x200000	The angle difference segment point defines P2, which satisfies IRMSmin<P1<P2<IRMSmax

The phase calibration register is a binary 24-bit register, and the data format of each register is as follows:

Address	Name	Bit width	Defaults	Description
64	IA_PHCAL	24	0x000000	A phase current channel angle difference correction register,
65	IB_PHCAL	24	0x000000	B-phase current channel angle difference correction register (same as above)
66	IC_PHCAL	24	0x000000	C-phase current channel angle difference correction register (same as above)
67	VA_PHCAL	24	0x000000	A phase voltage channel angle difference correction register,
68	VB_PHCAL	24	0x000000	B-phase voltage channel angle difference correction register (same as above)
69	VC_PHCAL	24	0x000000	C-phase voltage channel angle difference correction register (same as above)
90	IN_PHCAL	24	0x000000	The angle difference correction register of the IN phase current channel has the same adjustment accuracy as above.

3.1.2 Channel offset correction

Contains 7 16-bit channel offset calibration registers XX_CHOS, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel respectively. The deviation here may be due to the input and offset produced by the analog-to-digital conversion circuit itself. Deviation correction can make the waveform offset to 0 under no load.

Address	Name	Bit width	Defaults	Description
AC	IC_CHOS	16	0x0000	Current C channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Current B channel offset adjustment register, complement
AE	IA_CHOS	16	0x0000	Current A channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Current N channel offset adjustment register, complement

B2	VA_CHOS	16	0x0000	Voltage A channel offset adjustment register, complement
B3	VB_CHOS	16	0x0000	Voltage B channel offset adjustment register, complement
B4	VC_CHOS	16	0x0000	Voltage C channel offset adjustment register, complement

These registers are used for channel deviation calibration

Correction formula:

$$XX\_WAVE[N] = XX\_WAVE0[N] + XX\_CHOS$$

Where XX_WAVE0[N] is the measured value of the corresponding channel, XX_CHOS is the calibration value, and XX_WAVE is the output value after calibration.

3.1.3 Channel gain correction

Contains 7 16-bit channel gain calibration registers XX_CHGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They adjust the gain error caused by the analog-to-digital conversion of the current channel and the voltage channel with data in the form of 2's complement. The error here may be caused by the input and the analog-to-digital conversion circuit itself. Gain correction can be adjusted within ±50%.

Address	Name	Bit width	Defaults	Description
A1	IC_CHGN	16	0x0000	Current C channel gain adjustment register, complement
A2	IB_CHGN	16	0x0000	Current B channel gain adjustment register, complement
A3	IA_CHGN	16	0x0000	Current A channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Current N channel gain adjustment register, complement
A7	VA_CHGN	16	0x0000	Voltage A channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Voltage B channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Voltage C channel gain adjustment register, complement

These registers are used for channel gain calibration

Correction formula:

$$XX\_WAVE = XX\_WAVE0[N] * (1 + \frac{XX\_CHGN}{2^{16}})$$

Where XX_WAVE0 is the measurement value of the corresponding channel, XX_CHGN is the gain calibration value, and XX_WAVE is the calibration output value.

3.1.4 Current and voltage waveform output

The current load current and voltage waveform data can be collected, the sampling current and voltage are updated at a rate of 15.6ksps, and about 312 points can be sampled per cycle. Each sampled data is a 24-bit signed number, and is stored in the waveform register (I[N]_WAVE, V[N]_WAVE). The maximum SPI rate is 1.5Mbps, and the waveform values of multiple channels can be read continuously.

The channels can be selected through HPF, fundamental wave LPF, and finally 7-channel waveforms are obtained.

Address	Name	Bit width	Defaults	Description
2	IC_WAVE	24	0x000000	C-phase current waveform register
3	IB_WAVE	24	0x000000	B-phase current waveform register
4	IA_WAVE	24	0x000000	A-phase current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	A-phase voltage waveform register
9	VB_WAVE	24	0x000000	B-phase voltage waveform register
A	VC_WAVE	24	0x000000	C-phase voltage waveform register

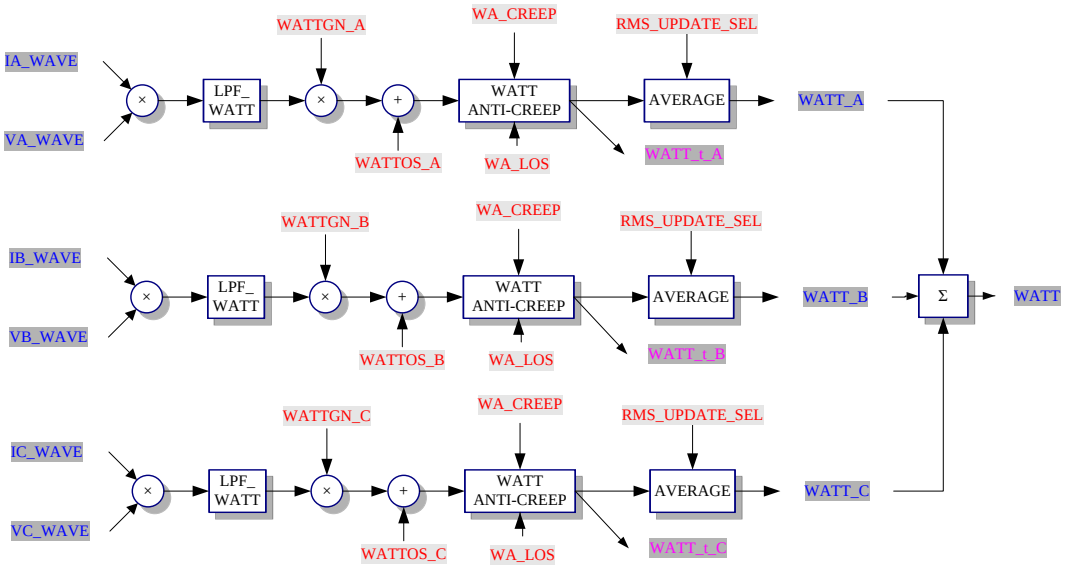
The waveform is divided into full wave and fundamental wave. The HPF is the AC measurement mode, and the full-wave waveform is output. Through fundamental

wave LPF as fundamental wave measurement mode, output fundamental wave waveform.

The waveform output selection is fixed, and it is set by the user mode register MODE1[23].

0x96	MODE1	Operating mode register	
No.	name	default value	description
[23]	WAVE_REG_SEL	1'b0	Current WAVE waveform register output selection, default 0 to select the waveform of the normal current channel, 1 to select the waveform output of the fast current channel

3.2 Principle of active power calculation



The three-phase current and voltage waveforms are respectively digitally multiplied, and then passed through the low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging in order to obtain the split-phase power signal, which is added to obtain the total active power.

3.2.1 Active power output

Corresponding to the three-phase currents are multiplied by the three-phase voltages to obtain the three-phase power signal, which is added to obtain the total power.

Address	Name	Bit width	Defaults	Description

22	WATT_A	24	0x000000	A-phase active power register (full wave and fundamental wave optional)
23	WATT_B	24	0x000000	B-phase active power register (full wave and fundamental wave optional)
24	WATT_C	24	0x000000	C-phase active power register (full wave and fundamental wave optional)
25	WATT	24	0x000000	Combined active power register (full wave and fundamental wave optional)

It can be set by the add_sel register, the power sum is absolute value addition or algebraic sum addition.

0x98	MODE3	Operating mode register	
No.	name	default value	description
[8]	add_sel	1'b0	watt and var conjoint sum accumulation method: 0-absolute value addition, |a|+|b|+|c|; 1-algebraic sum addition, a+b+c

Note: If four-quadrant reactive energy is required, MODE3[8] needs to be set to 1;

3.2.2 Active power calibration

Contains three 16-bit active power offset correction registers WATTOS_A/B/C and three 16-bit active power gain correction registers WATTGN_A/B/C, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

WATTOS is used to eliminate the DC deviation in the active power calculation, and WATTGN is used to eliminate the gain deviation in the active power calculation. The deviation here may be due to the crosstalk between the two channels generated on the PCB board and the integrated circuit itself in the power calculation, or it may be the gain deviation of the ADC channel itself.

Deviation correction can make the value in the active power register close to 0 under no load.

Address	Name	Bit width	Defaults	Description
B6	WATTGN_A	16	0x0000	A-phase active power gain adjustment register, complement

B7	WATTGN_B	16	0x0000	B-phase active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	C-phase active power gain adjustment register, complement
C2	WATTOS_A	16	0x0000	A-phase active power bias adjustment register, complement
C3	WATTOS_B	16	0x0000	B-phase active power bias adjustment register, complement
C4	WATTOS_C	16	0x0000	C-phase active power bias adjustment register, complement

For details of the correction formula, please refer to the register detailed description chapter.

3.2.3 Active power anti-creeping

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input. Active anti-creep threshold register (WA_CREEP), a 12-bit unsigned number, the default is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input active power signal. When the absolute value of the input active power signal is less than this value, the output active power is set to zero. This can make the value of the output to the active power register 0 under no load, even if there is a small noise signal.

Address	Name	Bit width	Defaults	Description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] is the reactive anti-creeping power threshold register [11:0] is the active anti-creeping power threshold register

$$\textbf{\textit{Corresponding to CREEP value}} = \frac{\textbf{\textit{Corresponding power register value}}}{2}$$

The WA_CREEP can be set according to the WATT value of the power register, and their corresponding relationship, the default anti-submarine value is about 20 parts per million of the power full scale.

When a phase is in the anti-submarine state, the power of the phase below the threshold does not participate in the energy accumulation.

The combined active anti-creep threshold register (WA_CREEP2) is a 12-bit unsigned number, and the default is 00H. This value is internally expanded by 1 and

compared with the absolute value of the input combined active power signal. When the absolute value of the input combined active power signal is less than this value, the output combined active power is set to zero. This is used to prevent creeping of the combined power.

Address	Name	Bit width	Defaults	Description
89	VAR_CREEP2/ WA_CREEP2	24	0x000000	[23:12] is the combined reactive anti-creeping power threshold register VAR_CREEP2; [11:0] is the combined active anti-creeping threshold register WA_CREEP 2

3.2.4 Active power small signal compensation

For the calculation of active power, in order to reduce the noise error in the small signal section, you can pass to the small signal compensation register to adjust the non-linear error of the small signal section.

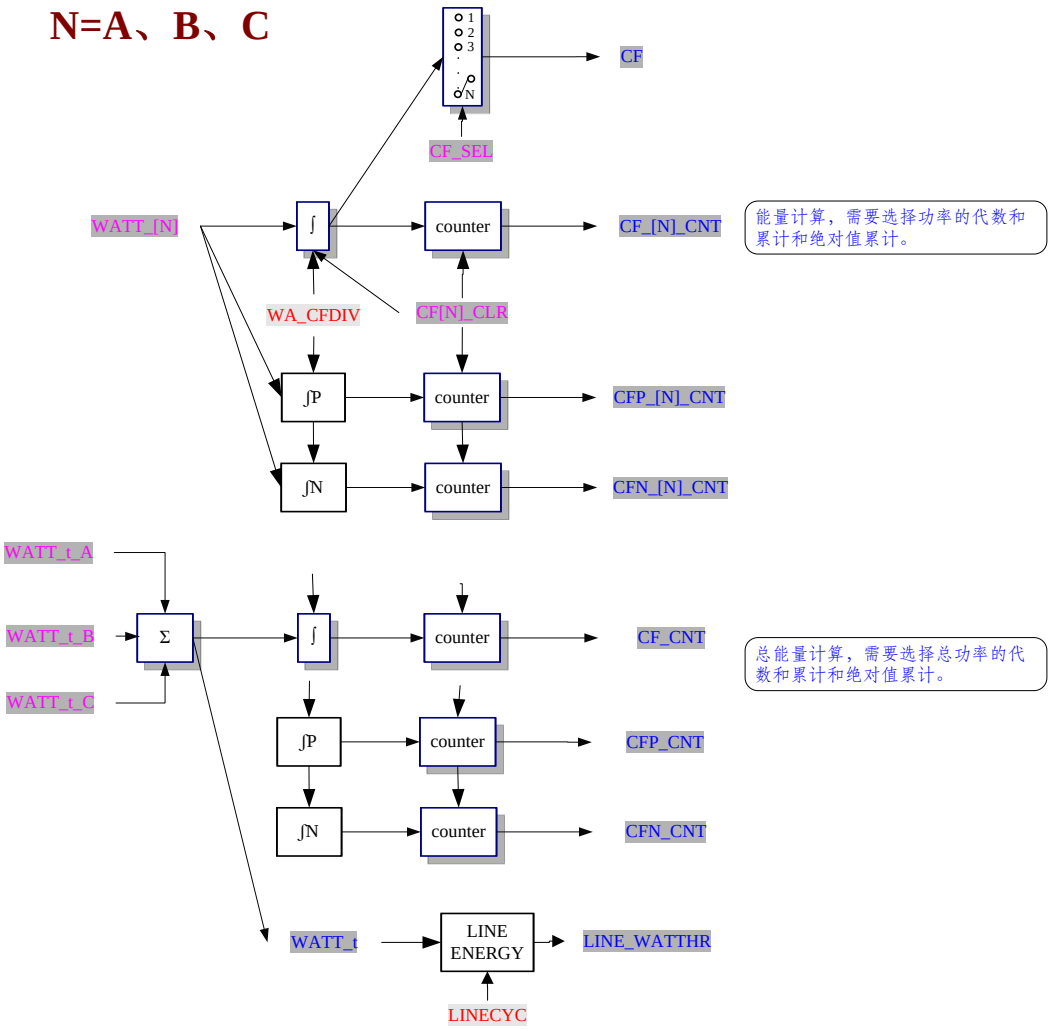
Address	Name	Bit width	Defaults	Description
82	WA_LOS_A	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.
83	WA_LOS_B	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.
84	WA_LOS_C	24	0x000	[23:12] Corresponding to active power small signal compensation register, complement.

3.2.5 Active power selection

Active power calculation method, you can select fundamental active power or full-wave active power through watt_sel, and the default is full-wave active power.

0x98	MODE3	Operating mode register	
No.	name	default value	description
[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave, 1-fundamental wave

3.3 Principles of active energy measurement



Provide three-phase electric energy pulse accumulation. The principle is that the active power of each phase can be integrated for a period of time to obtain the functional energy during this period, and further convert the energy into the corresponding frequency check pulse CF. The more electricity is used, the CF frequency will be faster, and the less electricity will be slow. Active energy accumulation includes positive power accumulation, negative power accumulation, algebraic and/absolute value accumulation.

3.3.1 Active energy output

The energy (power consumption) can be obtained by counting the CF pulse, which is stored in the Nth phase energy accumulation register CF[N]_CNT and the total energy register CF_CNT, as shown in the figure below.

Address	Name	Bit width	Defaults	Description
2F	CF_A_CNT	24	0x000000	A-phase active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B-phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C-phase active pulse count, unsigned
32	CF_CNT	24	0x000000	Combined phase active pulse count, unsigned
33	CFP_A_CNT	24	0x000000	A-phase positive active pulse count, unsigned
34	CFP_B_CNT	24	0x000000	B-phase positive active pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C-phase positive active pulse count, unsigned
36	CFP_CNT	24	0x000000	Combined phase positive active pulse count, unsigned
37	CFN_A_CNT	24	0x000000	A-phase negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B-phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C-phase negative active pulse count, unsigned
3A	CFN_CNT	24	0x000000	Combined phase negative active pulse count, unsigned

3.3.2 Active energy pulse output selection

0x98	MODE3	Operating mode register	
No.	name	default	description
[9]	cf_enable	1'b0	0-cf disable，default；1-cf enable

[13:10]	CF_SEL	4'b0000	Channel CF1/CF2 output selection, Default 0000, turn off CF1/CF2; 1111, turn off CF; 0001,watt_a/var_a electric energy CF; 0010,watt_b/var_b electric energy CF; 0011, watt_c/var_c electric energy CF; 0100, watt/var electric energy CF; 0101,watt_p_a/var1 electric energy CF; 0110,watt_p_b/var2 electric energy CF; 0111,watt_p_c/var3 electric energy CF; 1000,watt_p/var4 electric energy CF; 1001,watt_n_a/va_a electric energy CF; 1010,watt_n_/va_b electric energy CF; 1011,watt_n_c/va_c electric energy CF; 1100,watt_n/va electric energy CF 1101, (same as 0100); 1110, apparent energy CF;
[15]	cf_add_sel	1'b0	watt and var energy addition methods: 0-absolute value addition; 1-algebra and addition (phase separation and combination)

First set MODE3[9]=1 to select the CF pin to output electric energy pulses, and then set CF_SEL to select the corresponding electric energy pulses.

CF_add_sel is used to set the accumulating method of combined phase electric energy and split phase electric energy: algebraic sum or absolute value addition.

The count results of CF pulses are stored in the CF*_*_CNT registers, and the number of pulses can also be counted directly from the CF pin through I/O interrupts. When the cycle of CF is less than 180ms, it is a pulse with a 50% duty cycle. , When it is greater than or equal to 180ms, the pulse width is fixed to 90ms.

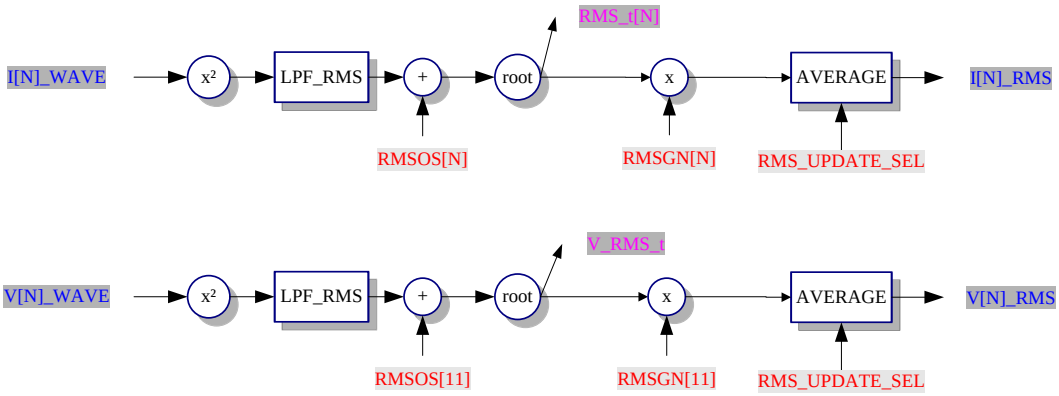
3.3.3 Active energy pulse output ratio

In the energy accumulation, the speed of energy accumulation can be set through the CF_DIV register, each gear *2 times relationship, a total of 12 gears.

Address	Name	Bit width	Defaults	Description
CE	CFDIV	12	0x010	Active CF scaling register [11:0]

3.4 Calculation principle of the effective value of current and voltage

The calculation principle of the effective value of the channel, as shown in the figure below



The original waveform of each channel passes through the square circuit (X^2), the effective value low-pass filter (LPF_RMS), and the root circuit (ROOT) to obtain the instantaneous value RMS_t of the effective value, and then average the average value of each channel The values I[N]RMS and V[N]_RMS.

3.4.1 Effective value output

The effective value calculation result is output and sum to 7 registers

Address	Name	Bit width	Defaults	Description
D	IC_RMS	24	0x000000	C-phase current RMS register, unsigned
E	IB_RMS	24	0x000000	B-phase current RMS register, unsigned
F	IA_RMS	24	0x000000	A-phase current RMS register, unsigned
10	IN_RMS	24	0x000000	Zero wire current RMS register, unsigned
13	VA_RMS	24	0x000000	A-phase voltage RMS register, unsigned
14	VB_RMS	24	0x000000	B-phase voltage RMS register, unsigned

15	VC_RMS	24	0x000000	C-phase voltage RMS register, unsigned

For the conversion formula of voltage RMS and current RMS, please refer to the detailed description chapter of the register.

3.4.2 Setting of effective value input signal

Set MODE2[21:0].WAVE_RMS_SEL to select the effective value to calculate the input waveform. Each channel can be selected by two bits, 00-high pass, 01-select fundamental wave, 11-select sinc for direct output.

0x97	MODE2	Operating mode register	
No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection, 00-high pass, 01-select fundamental wave, 11-select sinc output [3,2]: C-phase current; [5,4]: B-phase current [7,6]: Phase A current; [9:8]: Neutral line current [15,14]: Phase A voltage; [17,16]: Phase B voltage [19,18]: Phase C voltage

3.4.3 Valid value refresh rate setting

Set MODE2[22].RMS_UPDATE_SEL, you can choose the effective value average refresh time is 525ms or 1050ms, the default is 525ms.

0x97	MODE2	Operating mode register	
No.	name	default value	description
[22]	RMS_UPDATE_SEL	1'b0	Valid value register update speed selection, 1 is 1050ms, 0 is 525ms, 525ms is selected by default;

3.4.4 Current and voltage RMS calibration

Contains 7 24-bit RMS offset correction registers RMSOS[N] and 7 16-bit RMS gain correction registers RMSGN[N], the default value is 0x0000.

They use data in the form of 2's complement to calibrate the deviation in the effective value calculation. This deviation may come from input noise, because there

is a step of square operation in calculating the effective value, which may introduce a DC offset caused by noise. Gain and offset correction can make the value in the effective value register close to 0 under no load.

Address	Name	Bit width	Defaults	Description
6D	IC_RMSGN	16	0x0000	Current C channel RMS gain adjustment register
6E	IB_RMSGN	16	0x0000	Current B channel RMS gain adjustment register
6F	IA_RMSGN	16	0x0000	Current A channel RMS gain adjustment register
70	IN_RMSGN	16	0x0000	Current N channel RMS gain adjustment register
73	VA_RMSGN	16	0x0000	Voltage A channel RMS gain adjustment register
74	VB_RMSGN	16	0x0000	Voltage B channel RMS gain adjustment register
75	VC_RMSGN	16	0x0000	Voltage C channel RMS gain adjustment register
78	IC_RMSOS	24	0x000000	Current C channel RMS offset correction register
79	IB_RMSOS	24	0x000000	Current B channel RMS offset correction register
7A	IA_RMSOS	24	0x000000	Current A channel RMS offset correction register
7B	IN_RMSOS	24	0x000000	Current N channel RMS offset correction register
7E	VA_RMSOS	24	0x000000	Voltage A channel RMS offset correction register
7F	VB_RMSOS	24	0x000000	Voltage B channel RMS offset correction register
80	VC_RMSOS	24	0x000000	Voltage C channel RMS offset correction register

For details of the calibration formula, please refer to the register detailed description chapter.

3.4.5 Effective value of anti-creeping

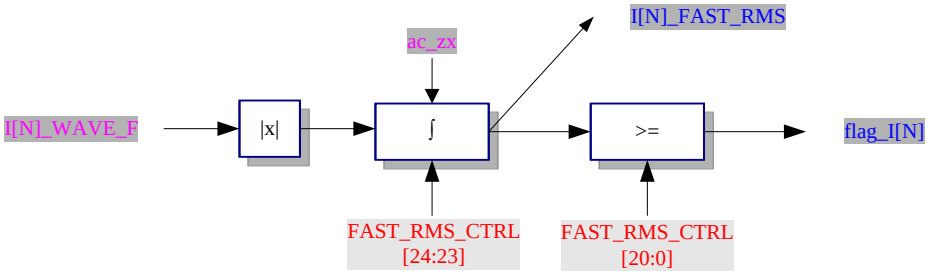
It has a patented effective value anti-submarine function to ensure that the effective value output is 0 when there is no current input.

The effective value anti-creep threshold register (RMS_CREEP) is a 12-bit unsigned number, and the default value is 0x200. This value is internally expanded by 1 and compared with the absolute value of the input effective value signal. When the input effective value signal is less than this value, the output effective value is set to zero. This can make the value output to the effective value register 0 even if there is a small noise signal under no load.

Address	Name	Bit width	Defaults	Description
8A	REVP_CREEP/ RMS_CREEP	24	0x04C200	[23:12] is the reverse indication threshold register REVP_CREEP; [11:0] is the effective value small signal threshold register RMS_CREEP;

3.5 Fast RMS detection principle

Fast RMS calculation principle see below,



7 channels have fast effective value registers, which can detect half cycle or cycle effective value. This function can be used for overcurrent detection.

The input waveform is obtained by taking the absolute value and then integrating within the specified time to obtain a fast effective value.

3.5.1 Fast RMS output

Fast RMS output register shown below channel 7

Address	Name	Bit width	Defaults	Description
18	IC_FAST_RMS	24	0x000000	C-phase current rapidly RMS register unsigned

19	IB_FAST_RMS	24	0x000000	B-phase current rapidly RMS register unsigned
1A	IA_FAST_RMS	24	0x000000	A-phase current rapidly RMS register unsigned
1B	IN_FAST_RMS	24	0x000000	Neutral current rapidly RMS register unsigned
1E	VA_FAST_RMS	24	0x000000	A-phase voltage rapidly RMS register unsigned
1F	VB_FAST_RMS	24	0x000000	B-phase voltage rapidly RMS register unsigned
20	VC_FAST_RMS	24	0x000000	C-phase voltage rapidly RMS register unsigned

3.5.2 Fast RMS input selection

Referring to a block diagram of the waveform of the source waveform channel. You can choose to pass HPF and not pass HPF.

0x96	MODE1	Operating mode register	
No.	name	default value	description
[22]	L_F_SEL	1'b0	Over current select through high pass, the default is 0 to select no high pass, and 1 to select high pass

3.5.3 Fast RMS cumulative time

Computing fast RMS, to take the absolute value, and a good set according to the cumulative time integral. Generally, it is an integer multiple of half cycle and cycle time.

Address	Name	Bit width	Defaults	Description
8B	FAST_RMS_CTRL	24	0x20FFFF	[23:21] Channel fast effective value register refresh time, half cycle and N cycle can be selected, the default is cycle; [20:0] reserved

Choose cumulative time by FAST_RMS_CTRL[23:21], which can be divided into six types: 000-10ms, 001-20ms, 010-40ms, 011-80ms, 100-160ms, 101-320ms. By default, the cycle cumulative response time is 20ms, and the cumulative time is selected. The longer the beating, the smaller the beating.

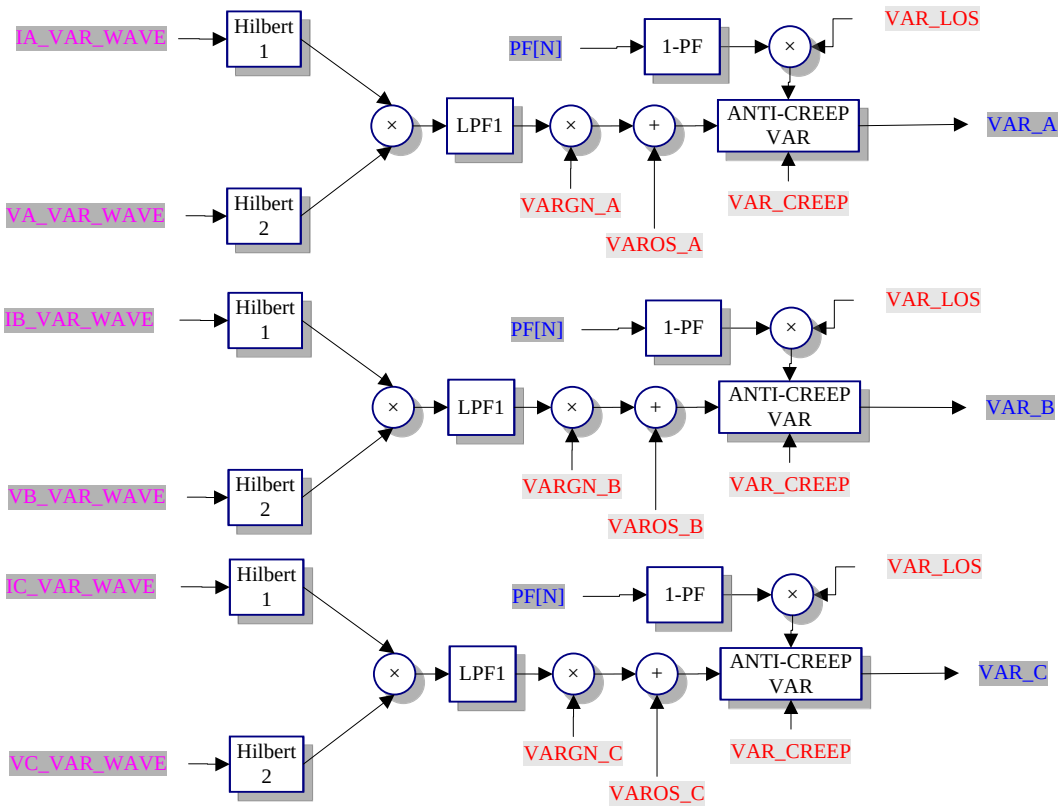
3.5.4 Grid frequency selection

In addition, it is necessary to distinguish between 50Hz and 60Hz half cycle time (AC_FREQ_SEL).

0x97	MODE2	Operating mode register	
No.	name	default value	description
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1 is 60Hz, 0 is 50Hz, 50Hz is selected by default

3.6 Reactive power calculation

The principle of reactive power calculation is shown in the figure below



After the current and voltage waveforms of each phase pass through the Hilbert filter, digital multiplication is performed, and then the reactive power signal can be obtained after the low-pass filter, gain and deviation calibration, anti-creeping judgment and averaging processing in order. After integration, the reactive energy pulse accumulation is obtained.

3.6.1 Reactive phase compensation

At the ADC output position, a digital calibration method for small phase errors is provided. It can introduce a small time delay or lead into the signal processing circuit to compensate for small phase errors. Since this compensation needs to be timely, this method is only suitable for small phase errors in the range of <0.6°. Using time-shift technology to correct large phase errors will introduce significant phase errors in higher harmonics.

Regarding the current and voltage signals for reactive power calculation, each is adjusted by a 4-bit register:

Address	Name	Bit width	Defaults	Description
6A	VAR_PHCAL_I	15	0x0000	Reactive power phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase current channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase current channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the reactive power calculation;
6B	VAR_PHCAL_V	15	0x0000	Reactive power phase correction (fine adjustment): [3:0] bits fine-tune the phase of the A-phase voltage channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase voltage channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase voltage channel in the reactive power calculation;

3.6.2 Reactive power output

Output 3 phase and combined phase reactive power, fundamental wave and full wave reactive power are given at the same time

Address	Name	Bit width	Defaults	Description
5A	VAR_A	24	0x000000	A-phase (full wave) reactive power register

5B	VAR_B	24	0x000000	B-phase (full wave) reactive power register
5C	VAR_C	24	0x000000	C-phase (full wave) reactive power register
5D	VAR	24	0x000000	Combined phase (full wave) reactive power register
2A	FVAR_A	24	0x000000	A-phase (fundamental wave) reactive power register
2B	FVAR_B	24	0x000000	B-phase (fundamental wave) reactive power register
2C	FVAR_C	24	0x000000	C-phase (fundamental wave) reactive power register
2D	FVAR	24	0x000000	Combined phase (fundamental wave) reactive power register

3.6.3 Reactive power calibration

Contains three 16-bit reactive power offset correction registers VAROS and three 16-bit reactive power gain correction registers VARGN, the default value is 0x0000.

Contains three 16-bit fundamental reactive power offset correction registers FVAROS and three 16-bit fundamental reactive gain correction registers FVARGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to calibrate the deviation in the reactive power calculation. This deviation may come from input noise or phase difference, which may introduce DC offset and gain errors caused by noise. Gain and deviation correction can correct the reactive power measurement curve.

Address	Name	Bit width	Defaults	Description
B9	VARGN_A	16	0x0000	A-phase reactive power gain adjustment register, complement
BA	VARGN_B	16	0x0000	B-phase reactive power gain adjustment register, complement
BB	VARGN_C	16	0x0000	C-phase reactive power gain adjustment register, complement
C5	VAROS_A	16	0x0000	A-phase reactive power offset adjustment register, complement

C6	VAROS_B	16	0x0000	B-phase reactive power offset adjustment register, complement
C7	VAROS_C	16	0x0000	C-phase reactive power offset adjustment register, complement

Address	Name	Bit width	Defaults	Description
BC	FVARGN_A	16	0x0000	A-phase fundamental reactive power gain adjustment register, complement
BD	FVARGN_B	16	0x0000	B-phase fundamental reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	A-phase fundamental reactive power gain adjustment register, complement
C8	FVAROS_A	16	0x0000	A-phase fundamental reactive power offset adjustment register, complement
C9	FVAROS_B	16	0x0000	B-phase fundamental reactive power offset adjustment register, complement
CA	FVAROS_C	16	0x0000	C-phase fundamental reactive power offset adjustment register, complement

For the calibration formula, please refer to the register detailed description chapter

3.6.4 Anti-creeping of reactive power

It has a patented power anti-submarine function to ensure that the power output is 0 when there is no current input.

The reactive power anti-creep threshold register (VAR_CREEP) is a 12-bit unsigned number, and the default value is 0x04C. This value is internally expanded by 1 and compared with the absolute value of the input reactive power signal. When the absolute value of the input reactive power signal is less than this value, the output reactive power is set to zero. This can make in the case of reactive power measurement, even if there is a small noise signal, the value output to the reactive power register is 0.

Address	Name	Bit width	Defaults	Description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] is the reactive anti-creeping power threshold register; [11:0] is the active anti-creeping power threshold register;

VAR_CREEP can be set according to the VAR value of the power register, and their corresponding relationship, the default anti-submarine value is 20 parts per million of the reactive power full scale.

When the channel is in the anti-submarine state, the power of the channel below the threshold does not participate in the energy accumulation.。

3.6.5 Reactive power small signal compensation

For the calculation of reactive power, in order to reduce the noise error in the small signal section, you can pass to the small signal compensation register to adjust the non-linear error of the small signal section.

Address	Name	Bit width	Defaults	Description
82	VAR_LOS_A	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement.
83	VAR_LOS_B	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement。
84	VAR_LOS_C	24	0x000	[11:0] Corresponding to the small reactive power compensation register, complement。
85	FVAR_LOS_A	24	0x000	[11:0] Corresponding to the reactive (fundamental) power small signal compensation register, complement.
86	FVAR_LOS_B	24	0x000	[11:0] Corresponding to the reactive (fundamental) power small signal compensation register, complement.
87	FVAR_LOS_C	24	0x000	[11:0] Corresponding to the reactive (fundamental) power small signal compensation register, complement.

3.6.6 Reactive energy output

The reactive energy can be obtained by counting the reactive CF pulse, which is stored in the reactive energy accumulation register CFQ_CNT, as shown in the figure below.

Address	Name	Bit width	Defaults	Description
3B	CFQ_A_CNT	24	0x000000	A phase reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	B phase reactive pulse count, unsigned

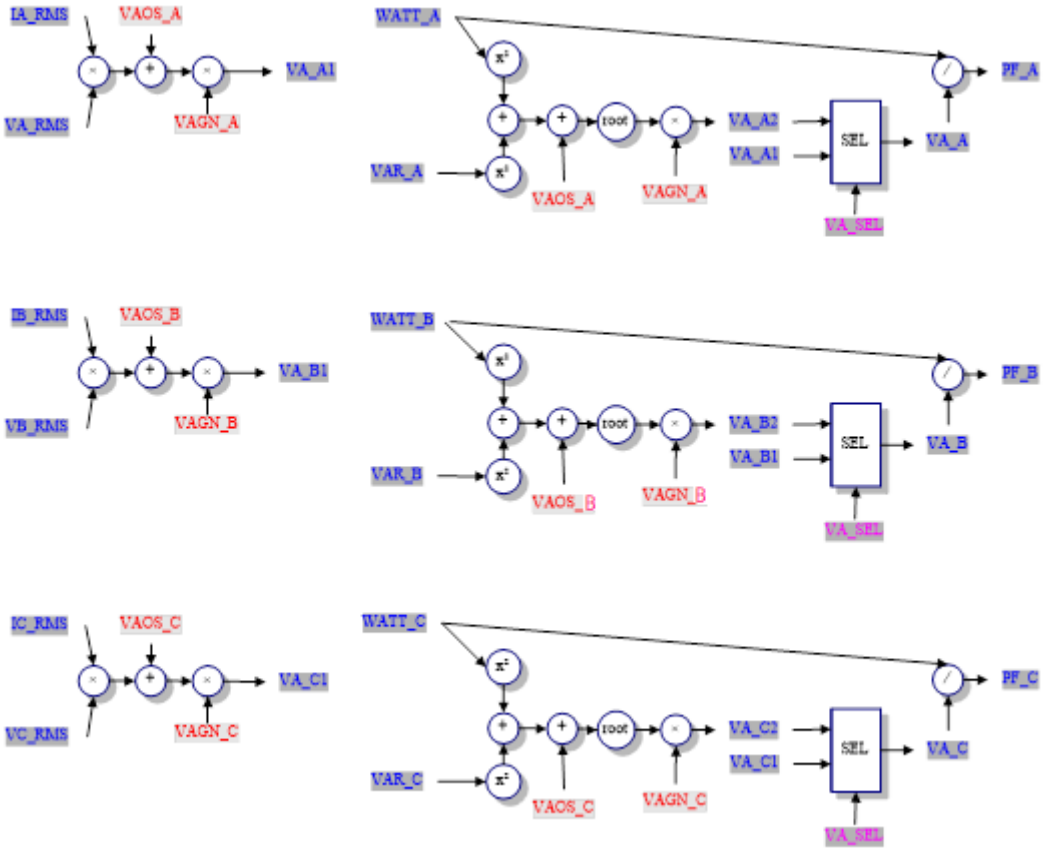
3D	CFQ_C_CNT	24	0x000000	C phase reactive pulse count, unsigned
3E	CFQ_CNT	24	0x000000	Combined phase reactive pulse count, unsigned
3F	CFQ1_CNT	24	0x000000	The first quadrant reactive pulse count, unsigned
40	CFQ2_CNT	24	0x000000	The second quadrant reactive pulse count, unsigned
41	CFQ3_CNT	24	0x000000	The third quadrant reactive pulse count, unsigned
42	CFQ4_CNT	24	0x000000	The fourth quadrant reactive pulse count, unsigned

Reactive energy calculation method, you can select fundamental reactive power or full-wave reactive power through var_sel, the default is fundamental reactive power:

0x98	MODE3	Operating mode register	
No.	name	default value	description
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave

3.7 Calculation of Apparent and Power Factor

Apparent calculation principles shown below



There are two ways of apparent calculation: One is the digital multiplication of the effective value of the current and voltage, and then the apparent power signal can be obtained after gain and offset calibration. The active power is divided by the apparent power to obtain the power factor.

The second is obtained by adding the square of active power to the square of reactive power, and then opening the root sign.

The reactive power and power factor calculated by the second method have better accuracy when measuring small signals.

3.7.1 Apparent power and energy output

Can output split-phase and combined-phase apparent power and apparent energy accumulation.

Address	Name	Bit width	Defaults	Description

26	VA_A	24	0x000000	A phase apparent power register
27	VA_B	24	0x000000	B phase apparent power register
28	VA_C	24	0x000000	C phase apparent power register
29	VA	24	0x000000	Combined phase apparent power register
43	CFS_A_CNT	24	0x000000	A phase apparent pulse count, unsigned
44	CFS_B_CNT	24	0x000000	B phase apparent pulse count, unsigned
45	CFS_C_CNT	24	0x000000	C phase apparent pulse count, unsigned
46	CFS_CNT	24	0x000000	Combined phase apparent pulse count, unsigned

3.7.2 Apparent power calibration

Contains three 16-bit apparent offset correction registers VAOS and three 16-bit apparent gain correction registers VAGN, the default value is 0x0000.

These registers can be used for digital calibration or error pre-calibration before leaving the factory.

They use the data in the form of 2's complement to calibrate the deviations that appear in the calculation. This deviation may originate from the previous stage, which may introduce offset and gain errors. Gain and deviation correction can correct the apparent measurement curve.

Address	Name	Bit width	Defaults	Description
BF	VAGN_A	16	0x0000	A phase apparent power gain adjustment register, complement
C0	VAGN_B	16	0x0000	B phase apparent power gain adjustment register, complement
C1	VAGN_C	16	0x0000	C phase apparent power gain adjustment register, complement
CB	VAOS_A	16	0x0000	A phase apparent power offset adjustment register, complement
CC	VAOS_B	16	0x0000	B phase apparent power offset adjustment register, complement
CD	VAOS_C	16	0x0000	C phase apparent power offset adjustment register, complement

For the calibration formula, please refer to the register detailed description chapter

3.7.3 Power factor

Output split-phase and combined-phase power factor.

Address	Name	Bit width	Defaults	Description
47	PF_A	24	0x000000	A phase power factor register
48	PF_B	24	0x000000	B phase power factor register
49	PF_C	24	0x000000	C phase power factor register
4A	PF	24	0x000000	Combined phase power factor register

24-bit signed number, complement. Bit[23] is the sign bit,

$$Power\ factor = \frac{PF}{2^{23}}$$

VA_SEL register selected by the calculated apparent power and power factor.

0x98	MODE3	Operating mode register	
No.	name	default value	description
[7]	va_sel	1'b0	va algorithm selection : 0-RMSI*RMSV ; 1-(watt^2+var^2)^0.5

3.8 Calculation of the sum of three-phase currents

3.8.1 The output of the current sum

The three-phase current sum can choose algebraic sum calculation, algebraic sum effective value calculation, or fast effective value calculation, and output to:

Address	Name	Bit width	Defaults	Description
57	I_SUM	24	0x000000	The sum of the instantaneous waveforms of the three-phase current
58	I_SUM_RMS	24	0x000000	The effective value of the sum of the three-phase current instantaneous waveforms, unsigned
59	I_SUM_FAST_RMS	24	0x000000	The fast effective value of the sum of the three-phase current instantaneous waveforms, unsigned

3.8.2 Adjustment of current sum

Contains a 24-bit current and effective value offset correction register ISUM_RMSOS and a 16-bit current and effective value gain correction register ISUM_RMSGN, the default value is 0000H.

Address	Name	Bit width	Defaults	Description

91	ISUM_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
92	ISUM_RMSOS	24	0x000000	Corresponding channel effective value offset correction register

3.8.3 Comparison of current sum

For the comparison of the neutral current, see the following register:

0x98	MODE3	Operating mode register	
No.	name	default value	description
[4]	isumlvl_sel	1'b0	When it is 0, compare the rms value of isumlvl and NI_RMS output neutral current; when it is 1, isumlvl and the rms value of the sum of the instantaneous waveforms of the output three-phase current;

Address	Name	Bit width	Defaults	Description
8D	ISUMLVL	24	0xFFFFFF	For the current comparison threshold register, select NI_RMS to compare with the ISUMLVL register. If IN_RMS is less than ISUMLVL, the interrupt status ISUMLVL_out is 0; if IN_RMS is less than ISUMLVL, the interrupt status ISUMLVL_out is 1. Note that IN_RMS can be selected as the effective value of the algebraic sum of three-phase transient currents or the actual measured effective value of the neutral line. The function is the same as PKLVL. Mode3[4]

3.9 Small signal compensation

For the calculation of active power (fundamental wave and full wave), reactive power (fundamental wave and full wave), and apparent power, in order to reduce the noise error in the small signal section, you can pass to the small signal compensation register to adjust the small signal section non-linear error.

Address	Name	Bit width	Defaults	Description
82	WA_LOS_A/ VAR_LOS_A	24	0x000000	[23:12] Corresponding to phase A active power small signal compensation register,

				complement. [11:0] Corresponding to phase A reactive power small signal compensation register, complement.
83	WA_LOS_B/ VAR_LOS_B	24	0x000000	[23:12] Corresponding to phase B active power small signal compensation register, complement. [11:0] Corresponding to phase B reactive power small signal compensation register, complement.
84	WA_LOS_C/ VAR_LOS_C	24	0x000000	[23:12] Corresponding to phase C active power small signal compensation register, complement. [11:0] Corresponding to phase C reactive power small signal compensation register, complement.
85	NC /FVAR_LOS_A	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
86	NC/ FVAR_LOS_B	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
87	NC/ FVAR_LOS_C	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.

3.10 Electrical parameter measurement

3.10.1 Line cycle measurement

With line cycle energy accumulation calculator, including active and reactive power.

Address	Name	Bit width	Defaults	Description
4B	LINE_ WATTHR	24	0x000000	Line cycle cumulative active energy register
4C	LINE_ VARHR	24	0x000000	Line cycle cumulative reactive energy register

The number of line cycles can be selected through the LINECYC register:

Address	Name	Bit width	Defaults	Description
8F	SAGLVL/ LINECYC	24	0x100009	[23:12] Drop voltage threshold register SAGLVL, voltage channel input continuously lower than the value of this

				register for more than the time in SAGCYC, will generate line voltage drop interrupt, the default is 100H, about 1/16 full amplitude voltage input; [11:0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles.

3.10.2 Line frequency measurement

For the grid line frequency test, the line frequency measured by the designated voltage input channel is tested. The count of the line period recorded in the PERIOD register, if the input signal deviates from 50Hz/60Hz, the corresponding count value will change.

Address	Name	Bit width	Defaults	Description
2E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)

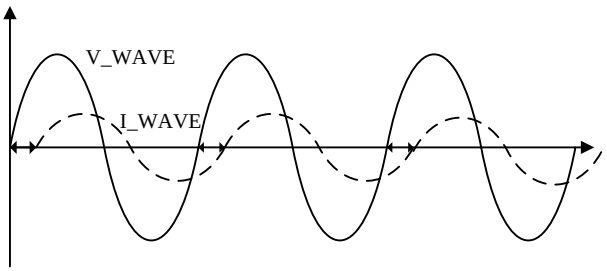
Measure the frequency of the sine wave signal of the voltage channel.

$$\boldsymbol{Line\ voltage\ frequency} = \frac{10000000}{PERIOD}\ \text{Hz}$$

The default is the frequency corresponding to the voltage channel A, set to other channels, see MODE3[6:5] register description

3.10.3 Phase angle calculation

Phase angle measurement principle, see the figure below



The phase difference is obtained by calculating the time difference between the positive phase zero crossing of the current and the voltage, and the corresponding time value is updated to the register CORNER[N]. Each register is a 16-bit unsigned number.

Address	Name	Bit width	Defaults	Description

4E	ANGLE_AB	16	0x0000	Phase-to-phase time register of voltage A phase and voltage B phase
4F	ANGLE_BC	16	0x0000	Phase-to-phase time register of voltage B phase and voltage C phase
50	ANGLE_AC	16	0x0000	Phase-to-phase time register of voltage A phase and voltage C phase
51	ANGLE_A	16	0x0000	Output phase A voltage and current time register
52	ANGLE_B	16	0x0000	Output phase B voltage and current time register
53	ANGLE_C	16	0x0000	Output C phase voltage and current time register

3.10.4 Power sign bit

For active and reactive power pulse CF output, there is a sign bit register to indicate the direction of each CF. The direction indicates the direction of the corresponding accumulated energy (electricity or power supply) from the last CF to the current CF pulse.

Address	Name	Bit width	Defaults	Description
4D	SIGN	24	0x0000	CF sign bit

SIGN[0]~ SIGN[23] correspond to the following CFs respectively

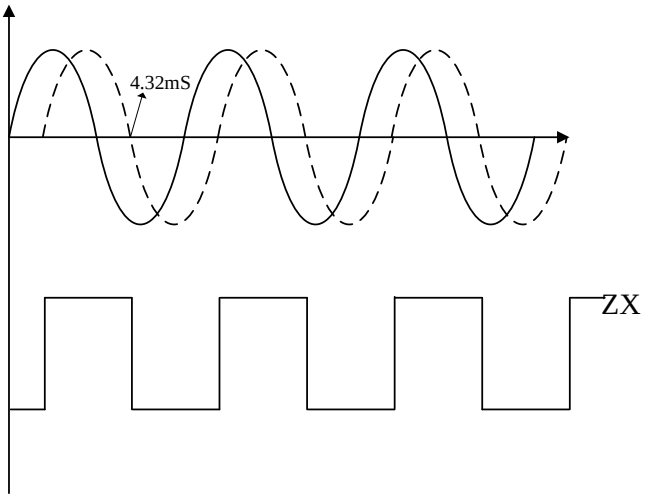
0	CF_A_CNT	8	Reserved	16	Reserved
1	CF_B_CNT	9		17	
2	CF_C_CNT	10		18	
3	CF_CNT	11		19	
4	Reserved	12	CFQ_A_CNT	20	
5		13	CFQ_B_CNT	21	
6		14	CFQ_C_CNT	22	
7		15	CFQ_CNT	23	

3.11 Fault detection

3.11.1 Zero crossing detection

Provides voltage/current zero-crossing detection, which can be configured to output zero-crossing signals through IRQ1 and AT1~3 pins. ZS is zero to indicate the positive half cycle of the waveform, and zx is 1 to indicate the negative half cycle of the waveform. What the chip detects is the fundamental zero-crossing signal, which

passes through the fundamental wave filter, and the time delay with the actual input signal is about 4.32mS.



Note: In order to prevent the uncertainty caused by the presence of noise signals or spurious signals in the presence of small signals, the current zero-crossing threshold is 70,000, and the voltage zero-crossing threshold is 200,000. If the instantaneous effective value is smaller than the threshold, there is no ZX signal.

If the instantaneous effective value of the voltage channel is smaller than the voltage drop threshold, it is in the SAG state and there is no corresponding ZX signal output.

3.11.2 Peak Detection

The threshold value of the current and voltage peak values can be set by programming, which is set by the peak value threshold register (I_PKLVL, V_PKLVL).

Address	Name	Bit width	Defaults	Description
8C	I_PKLVL/ V_PKLVL	24	0xFFFFFF	[23:12] Current peak value threshold register I_PKLVL; [11:0] Voltage peak value threshold register V_PKLVL

For example: when the instantaneous effective value of channel IA current is greater than the threshold set by the current peak limit register (I_PKLVL), the current overload indication PK_IA is given. If the corresponding PK_IA enable position in

the interrupt mask register (MASK1) is logic 1, then / The IRQ logic output becomes active low.

Similar to other current and voltage channels, the output is placed in the STATUS1 register

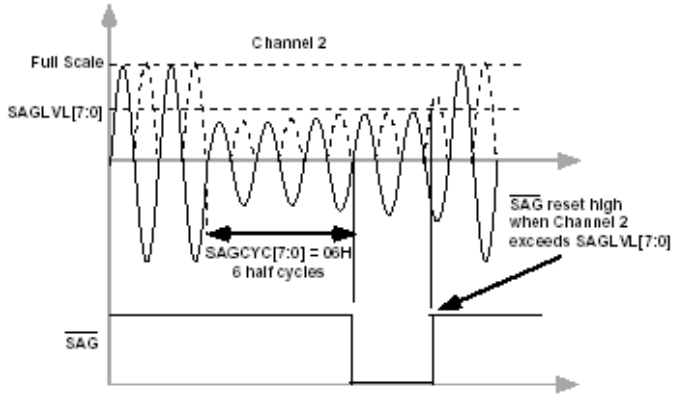
Address	Name	Bit width	Defaults	Description
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned

The corresponding positions are as follows:

position	Interrupt flag	Defaults	Description
13	PK_VA	0	Indicates that the peak value of the effective value of the phase A voltage channel exceeds the PKVLVL interrupt, which is 1
14	PK_IA	0	Indicates that the peak value of the effective value of the phase A current channel exceeds PKILVL interrupt, which is 1
15	PK_VB	0	Indicates that the peak value of the effective value of the phase B voltage channel exceeds the PKVLVL interrupt, which is 1
16	PK_IB	0	Indicates that the peak value of the effective value of the phase B current channel exceeds the PKILVL interrupt, which is 1
17	PK_VC	0	Indicates that the peak value of the effective value of the phase C voltage channel exceeds PKVLVL interrupt, which is 1
18	PK_IC	0	Indicates that the peak value of the effective value of the phase C current channel exceeds PKILVL interrupt, which is 1
19	PK_NI	0	Indicates that the peak value of the effective value of the N-phase current channel exceeds the PKILVL interrupt, which is 1

3.11.3 SAG Detection

It can be indicated by programming. When the instantaneous effective value of the line voltage is lower than a certain peak value for more than a certain number of half cycles, an indication of the line voltage drop will be given.



As shown in the figure above, when the instantaneous effective value of the voltage is less than the threshold set in the drop voltage threshold register (SAGLVL) and the drop time exceeds the set time in the drop line period register (SAGCYC) (the figure shows after the sixth half cycle is exceeded, SAGCYC[11:0]=06H), the line voltage drop event is recorded by setting the SAG flag bit in the interrupt status STATUS1 register

position	Interrupt flag	Defaults	Description
0	SAG_A	0	Indicates an A phase line voltage drop interruption, drop 1
1	SAG_B	0	Indicates the B phase line voltage drop generated interruption, drop 1
2	SAG_C	0	Indicates the C phase line voltage drop generated interruption, drop 1

If the corresponding SAG enable position in the interrupt mask register (MASK1) is logic 1, the /IRQ logic output becomes active low

Address	Name	Bit width	Defaults	Description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] The drop line period register SAGCYC, the default is 04H. [15:0] Zero-crossing time-out register ZXTOUT, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing time-out interrupt will be generated, the default is FFFFH.

8F	SAGLVL/ LINECYC	24	0x100009	[23:12] Drop voltage threshold register SAGLVL, voltage channel input continuously lower than the value of this register for more than the time in SAGCYC, will generate line voltage drop interrupt, the default is 100H, about 1/16 full amplitude voltage input; [11:0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles. The line period is related to the external crystal oscillator, the recommended crystal oscillator is 8MHz

The drop voltage threshold register (SAGLVL) can be written or read by the user, and the initial value is FFFH. The drop line period register (SAGCYC) can also be written or read by the user, and the initial value is FFH. The resolution of this register is 10ms/LSB, so the maximum delay time of an interrupt is limited to 2.55s.

3.11.4 Zero-crossing Timeout

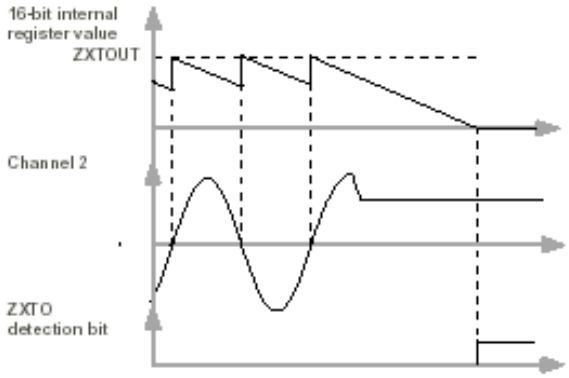
The zero-crossing detection circuit is also connected to a register ZXTOUT that detects the time-out of the zero-crossing signal, and ZXTOUT is set to the initial value whenever there is a zero-crossing signal in the detection voltage channel. If there is no zero-crossing signal, it will decrement. If there is no zero-crossing signal output for a long time, the value in this register will become 0. At this time, the corresponding bit ZXTO in the interrupt status register is set to 1, if the interrupt mask register is when the corresponding enable bit ZXTO is also 1, the zero-crossing signal timeout event will also be reflected on the interrupt pin/IRQ. Regardless of whether the corresponding enable bit in the interrupt register is set or not, the ZXTO flag bit in the interrupt status register (STATUS1) is always set to valid 1 when the ZXTOUT register is reduced to 0.

Address	Name	Bit width	Defaults	Description
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] The drop line period register SAGCYC, the default is 04H. [15:0] Zero-

				crossing time-out register ZXTOUT, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing time-out interrupt will be generated, the default is FFFFH.

The zero-crossing timeout register ZXTOUT can be written or read by the user, and the initial value is FFFFH. The resolution of this register is 70.5us/LSB, so the maximum delay time of an interrupt is limited to 4.369s.

The following figure shows the mechanism of detecting zero-crossing timeout when the line voltage is always a fixed DC signal:



The comparison result is placed in the STATUS1 register, corresponding to the location:

position	Interrupt flag	Defaults	Description
3	ZXTO_A	0	Indicates the generation of phase A zero-crossing timeout interrupt, the timeout is 1
4	ZXTO_B	0	Indicates that phase B zero-crossing timeout interrupt is generated, and the timeout is 1
5	ZXTO_C	0	Indicates that phase C zero-crossing timeout interrupt is generated, and the timeout is 1

3.11.5 Zero-crossing Detection

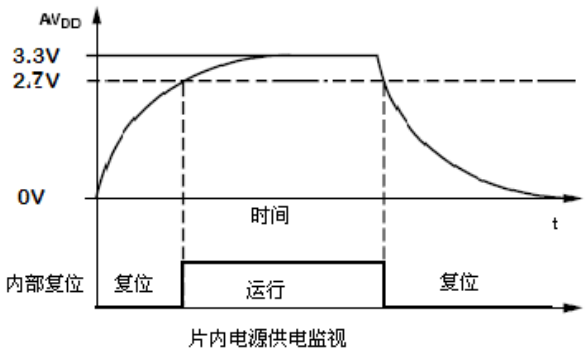
The result is placed in the STATUS1 register, the corresponding location::

position	Interrupt flag	Defaults	Description

6	ZX_VA	0	Indicate the sign bit of the phase A voltage waveform
7	ZX_IA	0	Indicate the sign bit of the phase A current waveform
8	ZX_VB	0	Indicate the sign bit of the phase B voltage waveform
9	ZX_IB	0	Indicate the sign bit of the phase B current waveform
10	ZX_VC	0	Indicate the sign bit of the phase C voltage waveform
11	ZX_IC	0	Indicate the sign bit of the phase C current waveform
12	ZX_IN	0	Indicate the sign bit of the phase N current waveform

3.11.6 Power supply Detection

Contains an on-chip power supply monitoring circuit that can continuously detect the analog power supply (AVDD). If the power supply voltage is less than 2.7V±5%, the entire circuit is not activated (not working), that is, when the power supply voltage is less than 2.7V, no energy accumulation is performed. This approach can ensure that the device maintains correct operation when the power is turned on and off. This power monitoring circuit has a hysteresis and filtering mechanism, which can eliminate false triggers caused by noise to a large extent. In general, the decoupling part of the power supply should ensure that the ripple on AVDD does not exceed 3.3V±5%.



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4、 Internal registers

4.1 Electrical parameter register (external read)

Address	Name	Bit width	Defaults	Description
2	IC_WAVE	24	0x000000	C-phase current waveform register
3	IB_WAVE	24	0x000000	B-phase current waveform register
4	IA_WAVE	24	0x000000	A-phase current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	A phase voltage waveform register
9	VB_WAVE	24	0x000000	B phase voltage waveform register
A	VC_WAVE	24	0x000000	C phase voltage waveform register
D	IC_RMS	24	0x000000	C-phase current RMS register, unsigned
E	IB_RMS	24	0x000000	B-phase current RMS register, unsigned
F	IA_RMS	24	0x000000	A-phase current RMS register, unsigned
10	IN_RMS	24	0x000000	Neutral current RMS register, unsigned
13	VA_RMS	24	0x000000	A-phase voltage RMS register, unsigned
14	VB_RMS	24	0x000000	B-phase voltage RMS register, unsigned
15	VC_RMS	24	0x000000	C-phase voltage RMS register, unsigned
18	IC_FAST_RMS	24	0x000000	C-phase current fast RMS register, unsigned
19	IB_FAST_RMS	24	0x000000	B-phase current fast RMS register, unsigned
1A	IA_FAST_RMS	24	0x000000	A-phase current fast RMS register, unsigned
1B	IN_FAST_RMS	24	0x000000	Neutral current fast RMS register, unsigned
1E	VA_FAST_RMS	24	0x000000	A phase voltage fast RMS register, unsigned
1F	VB_FAST_RMS	24	0x000000	B phase voltage fast RMS register, unsigned
20	VC_FAST_RMS	24	0x000000	C phase voltage fast RMS register, unsigned
22	WATT_A	24	0x000000	A phase active power register
23	WATT_B	24	0x000000	B phase active power register
24	WATT_C	24	0x000000	C phase active power register
25	WATT	24	0x000000	Combined phase active power register
26	VA_A	24	0x000000	A phase apparent power register
27	VA_B	24	0x000000	B phase apparent power register
28	VA_C	24	0x000000	C phase apparent power register

29	VA	24	0x000000	Combined phase apparent power register
2A	FVAR_A	24	0x000000	A phase (fundamental wave) reactive power register
2B	FVAR_B	24	0x000000	B phase (fundamental wave) reactive power register
2C	FVAR_C	24	0x000000	C phase (fundamental wave) reactive power register
2D	FVAR	24	0x000000	Combined phase (fundamental wave) reactive power register
2E	PERIOD	20	0x000000	Line voltage frequency period register (optional channel)
2F	CF_A_CNT	24	0x000000	A phase active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C phase active pulse count, unsigned
32	CF_CNT	24	0x000000	Combined phase active pulse count, unsigned
33	CFP_A_CNT	24	0x000000	A phase positive active pulse count, unsigned
34	CFP_B_CNT	24	0x000000	B phase positive active pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C phase positive active pulse count, unsigned
36	CFP_CNT	24	0x000000	Combined phase positive active pulse count, unsigned
37	CFN_A_CNT	24	0x000000	A phase negative active pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B phase negative active pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C phase negative active pulse count, unsigned
3A	CFN_CNT	24	0x000000	Combined phase negative active pulse count, unsigned
3B	CFQ_A_CNT	24	0x000000	A phase reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	B phase reactive pulse count, unsigned
3D	CFQ_C_CNT	24	0x000000	C phase reactive pulse count, unsigned
3E	CFQ_CNT	24	0x000000	Combined phase reactive pulse count, unsigned
3F	CFQ1_CNT	24	0x000000	The first quadrant reactive pulse count, unsigned
40	CFQ2_CNT	24	0x000000	The second quadrant reactive pulse count, unsigned

41	CFQ3_CNT	24	0x000000	The third quadrant reactive pulse count, unsigned
42	CFQ4_CNT	24	0x000000	The fourth quadrant reactive pulse count, unsigned
43	CFS_A_CNT	24	0x000000	A phase pulse count apparent, unsigned
44	CFS_B_CNT	24	0x000000	B phase pulse count apparent, unsigned
45	CFS_C_CNT	24	0x000000	C phase pulse count apparent, unsigned
46	CFS_CNT	24	0x000000	Combined phase pulse count apparent, unsigned
47	PF_A	24	0x000000	A phase power factor register
48	PF_B	24	0x000000	B phase power factor register
49	PF_C	24	0x000000	C phase power factor register
4A	PF	24	0x000000	Combined phase power factor register
4B	LINE_ WATTHR	24	0x000000	Line cycle cumulative active energy register
4C	LINE_ VARHR	24	0x000000	Line cycle cumulative reactive energy register
4D	SIGN	24	0x0000	CF sign bit
4E	ANGLE_AB	16	0x0000	Waveform angle register of voltage A phase and voltage B phase
4F	ANGLE_BC	16	0x0000	Waveform angle register of voltage B phase and voltage C phase
50	ANGLE_AC	16	0x0000	Waveform angle register of voltage A phase and voltage C phase
51	ANGLE_A	16	0x0000	A phase voltage and current waveform angle register
52	ANGLE_B	16	0x0000	B phase voltage and current waveform angle register
53	ANGLE_C	16	0x0000	C phase voltage and current waveform angle register
54	STATUS1	24	0x000000	Interrupt status register 1, unsigned
55	STATUS2	24	0x000000	Interrupt status register 2, unsigned
57	I_SUM	24	0x000000	The sum of the instantaneous waveforms of the three-phase current
58	I_SUM_RMS	24	0x000000	The RMS of the three-phase current instantaneous waveform sum, unsigned
59	I_SUM_FAST_RMS	24	0x000000	The fast RMS of the three-phase current instantaneous waveform sum, unsigned
5A	VAR_A	24	0x000000	A phase (full wave) reactive power register
5B	VAR_B	24	0x000000	B phase (full wave) reactive power register

5C	VAR_C	24	0x000000	C phase (full wave) reactive power register
5D	VAR	24	0x000000	Combined phase (full wave) reactive power register
5E	Reserved	10	0x000	Reserved

4.2 Calibration register 1

Address	Name	Bit width	Defaults	Description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register, [11:8]: C-phase current; [15:12]: B-phase current [19:16]: Phase A current; [23:20]: Neutral line current
61	GAIN2	20	0x00000	Channel PGA gain adjustment register, [11:8]: Phase A voltage; [15:12]: Phase B voltage [19:16]: Phase C voltage
62	IRMS_P1	24	0x010000	The angle difference segment point defines P1, which satisfies IRMSmin<P1<P2<IRMSmax
63	IRMS_P2	24	0x200000	The angle difference segment point defines P2, which satisfies IRMSmin<P1<P2<IRMSmax
64	IA_PHCAL	24	0x000000	Phase calibration of Phase A Current channel
65	IB_PHCAL	24	0x000000	Phase calibration of Phase B Current channel
66	IC_PHCAL	24	0x000000	Phase calibration of Phase C Current channel
67	VA_PHCAL	24	0x000000	Phase calibration of Phase A Voltage channel
68	VB_PHCAL	24	0x000000	Phase calibration of Phase B Voltage channel
69	VC_PHCAL	24	0x000000	Phase calibration of Phase C Voltage channel
6A	VAR_PHCAL_I	15	0x0000	Reactive power phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase current channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase

				current channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the reactive power calculation;
6B	VAR_PHCAL_V	15	0x0000	Reactive power phase correction (fine adjustment): [3:0] bits fine-tune the phase of the A-phase voltage channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase voltage channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase voltage channel in the reactive power calculation;
6D	IC_RMSGN	16	0x0000	Phase C Current RMS gain adjust
6E	IB_RMSGN	16	0x0000	Phase B Current RMS gain adjust
6F	IA_RMSGN	16	0x0000	Phase A Current RMS gain adjust
70	IN_RMSGN	16	0x0000	Phase N Current RMS gain adjust
73	VA_RMSGN	16	0x0000	Phase A Voltage RMS gain adjust
74	VB_RMSGN	16	0x0000	Phase B Voltage RMS gain adjust
75	VC_RMSGN	16	0x0000	Phase C Voltage RMS gain adjust
78	IC_RMSOS	24	0x000000	Phase C Current RMS offset
79	IB_RMSOS	24	0x000000	Phase B Current RMS offset
7A	IA_RMSOS	24	0x000000	Phase A Current RMS offset
7B	IN_RMSOS	24	0x000000	Phase N Current RMS offset
7E	VA_RMSOS	24	0x000000	Phase A Voltage RMS offset
7F	VB_RMSOS	24	0x000000	Phase B Voltage RMS offset
80	VC_RMSOS	24	0x000000	Phase C Voltage RMS offset
82	WA_LOS_A/ VAR_LOS_A	24	0x000000	[23:12] Corresponding to phase A active power small signal compensation register, complement. [11:0] Corresponding to phase A reactive power small signal compensation register, complement.
83	WA_LOS_B/ VAR_LOS_B	24	0x000000	[23:12] Corresponding to phase B active power small signal compensation register, complement. [11:0] Corresponding to phase B reactive power small signal compensation register, complement.
84	WA_LOS_C/ VAR_LOS_C	24	0x000000	[23:12] Corresponding to phase C active power small signal compensation

				register, complement. [11:0] Corresponding to phase C reactive power small signal compensation register, complement.
85	FVAR_LOS_A	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
86	FVAR_LOS_B	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
87	FVAR_LOS_C	24	0x000000	[11:0] Corresponding to the reactive power small signal compensation register, complement.
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] Reactive anti-creeping power threshold register [11:0] is the active anti-creeping power threshold register
89	VAR_CREEP2/ WA_CREEP2	24	0x000000	[23:12] is the combined reactive power anti-creeping power threshold register [11:0] is the combined active anti-creeping power threshold register;
8A	REVP_CREEP/ RMS_CREEP	24	0x04C200	[23:12] is the reverse indication threshold register REVP_CREEP; [11:0] is the effective value small signal threshold register RMS_CREEP
8B	FAST_RMS_CTRL	24	0x20FFFF	[23:21] Channel fast effective value register refresh time, half cycle and N cycle can be selected, the default is cycle; [20:0] channel fast effective value threshold register
8C	I_PKLVL/ V_PKLVL	24	0xFFFFFF	[23:12] Current peak value threshold register I_PKLVL; [11:0] Voltage peak threshold register V_PKLVL
8D	ISUMLVL	24	0xFFFFFF	For the current comparison threshold register, select NI_RMS to compare with the ISUMLVL register. If IN_RMS is less than ISUMLVL, the interrupt status ISUMLVL_out is 0; if IN_RMS is less than ISUMLVL, the interrupt status ISUMLVL_out is 1. Note that IN_RMS can be selected as the effective value of the algebraic sum of three-phase transient currents or the actual measured effective value of the

				neutral line. The function is the same as PKLVL. Mode3[4]
8E	SAGCYC/ ZXTOUT	24	0x04FFFF	[23:16] The SAG period register SAGCYC, the default is 04H. [15:0] Zero-crossing time-out register ZXTOUT, if there is no zero-crossing signal within the time indicated by this register, a zero-crossing time-out interrupt will be generated, the default is FFFFH.
8F	SAGLVL/ LINECYC	24	0x100009	[23:12] SAG threshold register SAGLVL, voltage channel input continuously lower than the value of this register for more than the time in SAGCYC, will generate line voltage drop interrupt, the default is 100H, about 1/16 full amplitude voltage input; [11:0] Line energy accumulation cycle number register LINECYC, default 009H, representing 10 cycles.
90	IN_PHCAL	24	0x000000	Phase calibration of Phase N current channel
91	ISUM_RMSGN	16	0x0000	Corresponding channel effective value gain adjustment register
92	ISUM_RMSOS	24	0x000000	Corresponding channel effective value offset correction register
93	ADC_PD	11	0x000	7 channels ADC enable control; when set to 1, the corresponding channel ADC is closed. [2]: C-phase current; [3]: B-phase current; [4]: Phase A current; [5]: Neutral line current; [8]: Phase A voltage; [9]: Phase B voltage; [10]: Phase C voltage
94	Reserved	16	0x07FF	Reserved
96	MODE1	24	0x000000	User mode selection register 1
97	MODE2	24	0x000000	User mode selection register2
98	MODE3	24	0x000000	User mode selection register 3
9A	MASK1	24	0x000000	Interrupt mask register, which controls whether an interrupt generates a valid IRQ1 output, please refer to the

				description of "Interrupt Mask Register" for details
9B	MASK2	24	0x000000	Interrupt mask register, which controls whether an interrupt generates a valid IRQ2 output, please refer to the description of "Interrupt Mask Register" for details
9D	RST_ENG	24	0x000000	Energy clearing setting register, see the description of "Energy clearing setting register" for details
9E	USR_WRPROT	16	0x0000	User write protection setting register
9F	SOFT_RESET	24	0x000000	When the input is 5A5A5A, reset the electrical parameter register; When the input is 55AA55, the calibration register is reset: Reg60~reg9F, RegA0~RegD0

4.3 Calibration register 2

Calibration register

Address	Name	Bit width	Defaults	Description
A1	IC_CHGN	16	0x0000	Current C channel gain adjustment register, complement
A2	IB_CHGN	16	0x0000	Current B channel gain adjustment register, complement
A3	IA_CHGN	16	0x0000	Current A channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Current N channel gain adjustment register, complement
A7	VA_CHGN	16	0x0000	Voltage A channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Voltage B channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Voltage C channel gain adjustment register, complement
AC	IC_CHOS	16	0x0000	Current C channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Current B channel offset adjustment register, complement
AE	IA_CHOS	16	0x0000	Current A channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Current N channel offset adjustment register, complement

B2	VA_CHOS	16	0x0000	Voltage A channel offset adjustment register, complement
B3	VB_CHOS	16	0x0000	Voltage B channel offset adjustment register, complement
B4	VC_CHOS	16	0x0000	Voltage C channel offset adjustment register, complement
B6	WATTGN_A	16	0x0000	A phase active gain adjustment register, complement
B7	WATTGN_B	16	0x0000	B-phase active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	C-phase active power gain adjustment register, complement
B9	VARGN_A	16	0x0000	A phase reactive power gain adjustment register, complement
BA	VARGN_B	16	0x0000	B-phase reactive power gain adjustment register, complement
BB	VARGN_C	16	0x0000	C-phase reactive power gain adjustment register, complement
BC	FVARGN_A	16	0x0000	A phase fundamental reactive power gain adjustment register, complement
BD	FVARGN_B	16	0x0000	B-phase fundamental reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	C-phase fundamental reactive power gain adjustment register, complement
BF	VAGN_A	16	0x0000	A phase apparent power gain adjustment register, complement
C0	VAGN_B	16	0x0000	B-phase apparent power gain adjustment register, complement
C1	VAGN_C	16	0x0000	C-phase apparent power gain adjustment register, complement
C2	WATTOS_A	16	0x0000	A phase active power offset adjustment register, complement
C3	WATTOS_B	16	0x0000	B-phase active power offset adjustment register, complement
C4	WATTOS_C	16	0x0000	C-phase active power offset adjustment register, complement
C5	VAROS_A	16	0x0000	A phase reactive power offset adjustment register, complement
C6	VAROS_B	16	0x0000	B-phase reactive power offset adjustment register, complement
C7	VAROS_C	16	0x0000	C-phase reactive power offset adjustment register, complement

C8	FVAROS_A	16	0x0000	A phase fundamental reactive power offset adjustment register, complement
C9	FVAROS_B	16	0x0000	B-phase fundamental reactive power offset adjustment register, complement
CA	FVAROS_C	16	0x0000	C-phase fundamental reactive power offset adjustment register, complement
CB	VAOS_A	16	0x0000	A phase apparent power offset adjustment register, complement
CC	VAOS_B	16	0x0000	B-phase apparent power offset adjustment register, complement
CD	VAOS_C	16	0x0000	C-phase apparent power offset adjustment register, complement
CE	CFDIV	12	0x010	Active CF scaling register
CF	AT_SEL	9	0x000	AT1~3 logic output pin configuration
D0	Reserved	16	0x0000	Reserved

4.4 Detailed description of calibration register

4.4.1 Channel PGA gain adjustment register

Address	Name	Bit width	Defaults	Description
60	GAIN1	24	0x000000	Channel PGA gain adjustment register
61	GAIN2	20	0x00000	Channel PGA gain adjustment register

It is used to set the PGA amplification parameters of the analog input channel, which can be set (0000=1 times; 0001=2 times; 0010=8 times; 0011=16 times); one channel is set for every 4bit.

GAIN1	Bit[23:20]	Bit[19:16]	Bit[15:12]	Bit[11:8]	Bit[7:4]	Bit[3:0]
	Neutral current	A phase current	B phase current	C phase current	Reserved	Reserved

GAIN2	Bit[23:20]	Bit[19:16]	Bit[15:12]	Bit[11:8]	Bit[7:4]	Bit[3:0]
	Reserved	C phase voltage	B phase voltage	A phase voltage	Reserved	Reserved

Note that, after setting the corresponding channel gain, the maximum allowable channel input signal also is reduced accordingly!

PGAgain	Channel maximum input differential signal
1	700mV pp（495mV rms）
2	350mV pp（247.5mV rms）

8	87.5mVpp（61.9mV rms）
16	43.75mVpp（30.9mV rms）

4.4.2 Phase correction related registers

Current channel angle differential segment definition register：

Address	Name	Bit width	Defaults	Description
62	IRMS_P1	24	0x010000	The angle difference segment point defines P1, which satisfies IRMSmin<P1<P2<IRMSmax
63	IRMS_P2	24	0x200000	The angle difference segment point defines P2, which satisfies IRMSmin<P1<P2<IRMSmax

Since the current transformer used for three-phase measurement may have different angular differences at different currents, BL6552 can be set to perform segmented phase compensation according to the effective value of the current

Address	Name	Bit width	Defaults	Description
64	IA_PHCAL	24	0x000000	A phase current channel angle difference correction register
65	IB_PHCAL	24	0x000000	B-phase current channel angle difference correction register (same as above)
66	IC_PHCAL	24	0x000000	C-phase current channel angle difference correction register (same as above)
67	VA_PHCAL	24	0x000000	A phase voltage channel angle difference correction register,
68	VB_PHCAL	24	0x000000	B-phase voltage channel angle difference correction register (same as above)
69	VC_PHCAL	24	0x000000	C-phase voltage channel angle difference correction register (same as above)
90	IN_PHCAL	24	0x000000	IN phase current channel angle difference correction register

Take the A-phase current channel angle difference correction register as an example to explain：

1） When IRMSmin<effective value of input current (IA_RMS)<P1, IA_PHCAL[7:0] is used to correct the current channel phase, the minimum adjustment delay time is 250ns, corresponding to 0.0045 degrees/1LSB, and the maximum adjustable is ±0.574 degrees).

2） When P1<effective value of input current (IA_RMS)<P2, IA_PHCAL [15:8] is used to correct the phase of the current channel, and the adjustment accuracy is the same as above.

3） When P2<The effective value of input current (IA_RMS)<IRMSmax, IA_PHCAL [23:16] is used to correct the phase of the current channel, and the adjustment accuracy is the same as above.

(The minimum adjustment delay time is 250nS, corresponding to 0.0045°/LSB, the corresponding error is ≈1.732*Sin(0.0045°)=0.0136%, the maximum adjustment is about 0.574°, and the maximum adjustment error is about 1.734%.)

Address	Name	Bit width	Defaults	Description
6A	VAR_PHCAL_I	15	0000H	Reactive power phase correction (fine tuning): [3:0] bits fine-tune the phase of the A-phase current channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase current channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase current channel in the reactive power calculation;
6B	VAR_PHCAL_V	15	0000H	Reactive power phase correction (fine adjustment): [3:0] bits fine-tune the phase of the A-phase voltage channel in the reactive power calculation; [7:4] bits fine-tune the phase of the B-phase voltage channel in the reactive power calculation; [11:8] Bit to fine-tune the phase of the C-phase voltage channel in the reactive power calculation;

Take the VAR_PHCAL_I register as an example,

the description is as follows Reactive power phase correction (fine adjustment):

[3:0] bit fine-tune the phase of the A-phase current channel in the reactive power calculation;

[7:4] Fine-tune the phase of the B-phase current channel in the reactive power calculation;

[11:8] Bit fine-tuning the phase of the C-phase current channel in the reactive power calculation;

[11], [7], [3] are enable bits, the minimum adjustment delay time is 560ns, corresponding to 0.009 degrees/1LSB, and the corresponding error is ≈0.0245%.

Reactive power phase correction (coarse adjustment):

[12] Corresponding to the phase of A-phase current channel, IA channel reactive power delay 64us when=1;

[13] Corresponding to the phase of the B-phase current channel, the reactive power delay of the IB channel is 64us when=1;

[14] Corresponding to the phase of the C-phase current channel, when =1, the reactive power delay of the IC channel is 64us;

4.4.3 RMS gain adjustment register

Address	Name	Bit width	Defaults	Description
6D	IC_RMSGN	16	0x0000	Phase C Current RMS gain adjust
6E	IB_RMSGN	16	0x0000	Phase B Current RMS gain adjust
6F	IA_RMSGN	16	0x0000	Phase A Current RMS gain adjust
70	IN_RMSGN	16	0x0000	Phase N Current RMS gain adjust
73	VA_RMSGN	16	0x0000	Phase A Voltage RMS gain adjust
74	VB_RMSGN	16	0x0000	Phase B Voltage RMS gain adjust
75	VC_RMSGN	16	0x0000	Phase C Voltage RMS gain adjust

Complement code, the highest bit is the sign bit, used for gain correction of the effective value, the adjustment range is ±50%

$$X\_RMS = X\_RMS0 * (1 + \frac{X\_RMSGN}{2^{16}})$$

Where X_RMS0 is the measured value of the effective value of the corresponding channel, X_RMSGN is the gain adjustment value of the corresponding

channel, and X_RMS is the corresponding output value of the effective value after calibration.

4.4.3 RMS offset correction register

Address	Name	Bit width	Defaults	Description
78	IC_RMSOS	24	0x000000	Phase C Current RMS offset
79	IB_RMSOS	24	0x000000	Phase B Current RMS offset
7A	IA_RMSOS	24	0x000000	Phase A Current RMS offset
7B	IN_RMSOS	24	0x000000	Phase N Current RMS offset
7E	VA_RMSOS	24	0x000000	Phase A Voltage RMS offset
7F	VB_RMSOS	24	0x000000	Phase B Voltage RMS offset
80	VC_RMSOS	24	0x000000	Phase C Voltage RMS offset

Complement, the sign bit of the most significant bit. It is used to eliminate the deviation caused by input noise in the effective value calculation, and the effective value register value can be close to 0 under no load.

$$X\_RMS = \sqrt{X\_RMS0^2 + X\_RMSOS * 256}$$

Where X_RMS0 is the measured value of the effective value of the corresponding channel, X_RMSOS is the offset correction value of the corresponding channel, and I[N]_RMS is the corresponding output value of the effective value after calibration.

4.4.4 Power small signal compensation register

Address	Name	Bit width	Defaults	Description
82	WA_LOS_A/ VAR_LOS_A	24	0x000000	[23:12] Corresponding to A phase active power small signal compensation value, complement. [11:0] Corresponding to A

				phase reactive power small signal compensation value, complement code.
83	WA_LOS_B/ VAR_LOS_B	24	0x000000	[23:12] Corresponding to B phase active power small signal compensation value, complement. [11:0] Corresponding to B phase reactive power small signal compensation value, complement.
84	WA_LOS_C/ VAR_LOS_C	24	0x000000	[23:12] Corresponding to C phase active power small signal compensation value, complement. [11:0] Corresponding to C phase reactive power small signal compensation value, complement code.
85	FVAR_LOS_A	24	0x000000	[23:12] reserved [11:0] Corresponding to A phase reactive power small signal compensation register, complement.
86	FVAR_LOS_B	24	0x000000	[23:12] reserved [11:0] Corresponding to B phase reactive power small signal compensation register, complement.
87	FVAR_LOS_C	24	0x000000	[23:12] reserved [11:0] Corresponding to C phase reactive power small signal compensation register, complement.

Used to compensate the small signal deviation of active power caused by DC offset,

$$WATT\_X = WATT\_X0 + WA\_LOS\_X * 2$$

Among them, WATT_X0 is the active power measurement value corresponding to a certain phase, WA_LOS_X is the corresponding small signal compensation correction value, and WATT_X is the active power calibration output value corresponding to a certain phase.

Note that WA_LOS_X is a signed number, complement code, and the correction range of the active power register is ±4094. Reactive small signal compensation is similar;

4.4.5 Anti-creep threshold register

Address	Name	Bit width	Defaults	Description
88	VAR_CREEP/ WA_CREEP	24	0x04C04C	[23:12] is the anti-creeping threshold of reactive power [11:0] is the anti-creeping threshold of active power

Active power/reactive power anti-creep setting for each split phase. When a certain phase is in the anti-submarine state, the power of the phase below the threshold does not participate in the energy accumulation.

When the absolute value of the input power signal is less than this value, the output power register value is set to zero. This can make the value of output to the active power register 0 under no-load conditions, even if there is a small noise signal.

$$对应CREEP值 = \frac{对应功率寄存器值}{2}$$

Address	Name	Bit width	Defaults	Description
89	VAR_CREEP2/ WA_CREEP2	24	0x000000	[23:12] is the anti-creeping threshold of the combined reactive power; [11:0] is the anti-creeping threshold of the combined active power

The anti-creep threshold setting of the combined active/reactive power, if the Reg88 register has been set, this register does not need to be set.

$$WA\_CREEP2 = \frac{WATT寄存器值}{2}$$

Address	Name	Bit width	Defaults	Description
8A	REVP_CREEP/ RMS_CREEP	12	0x04C200	[23:12] is the reverse indication threshold [11:0] is the effective value anti-creeping power threshold,

It is possible to make the value output to the effective value register 0 under no load, even if there is a small noise signal.

$$RMS\_CREEP = X\_RMS$$

4.4.6 Fast effective value related setting register

Address	Name	Bit width	Defaults	Description
8B	FAST_RMS_CTRL	24	0x20FFFF	[23:21] Channel fast effective value register refresh time, half cycle and N cycle can be selected, the default is cycle; [20:0] reserved

Choose cumulative time by FAST_RMS_CTRL[23:21], divided into six types: 10ms(000), 20ms(001), 40ms(010), 80ms(011), 160ms(100), 320ms(101), default (001) selection The cumulative response time of the cycle is 20ms, and the longer the cumulative time, the smaller the jitter.

FAST_RMS_CTRL[20:0] reserved;

4.4.7 Fault detection related registers

See the description in chapter 3.12 Fault Detection

4.4.8 ADC enable control

Address	Name	Bit width	Defaults	Description
93	ADC_PD	11	0x000	7 analog channels ADC enable control

Power consumption can be reduced by closing unused channels.

Bit	10	9	8	7：6	5	4	3	2	1：0
Channel	Voltage C	Voltage B	Voltage A	Reserved	Current N	Current A	Current B	Current C	Reserved

When the corresponding bit is set to 1, close the corresponding analog channel to achieve the purpose of reducing power consumption;

Note: The reserved bits Bit[7:6] and Bit[1:0] need to be set to 1 during power-on initialization!

4.4.9 Mode register 1

0x96	MODE1	Operating mode register

No.	name	default value	description
[10:0]		00	Reserved
[21:11]		00	Reserved
[22]	L_F_SEL	1'b0	The fast effective value is selected through the high-pass, the default is 0 to select no high-pass, and 1 to select high-pass
[23]	WAVE_REG_SEL	1'b0	Current WAVE waveform register output selection, default 0 to select the waveform of the normal effective value channel, and 1 to select the waveform output of the fast effective value channel

4.4.10 Mode register 2

0x97	MODE2	Operating mode register	
No.	name	default value	description
[21:0]	WAVE_RMS_SEL	11{2'b00}	RMS waveform selection, 00-high pass, 01-select fundamental wave, 11-select sinc output [3,2]: C-phase current; [5,4]: B-phase current [7,6]: A phase current; [8,9]: Neutral line current [15,14]: A phase voltage; [17,16]: B phase voltage [19,18]: C phase voltage
[22]	RMS_UPDATE_SEL	1'b0	Valid value register update speed selection, 1 is 1000ms, 0 is 500ms, 500ms is selected by default;
[23]	AC_FREQ_SEL	1'b0	AC frequency selection, 1 is 60Hz, 0 is 50Hz, 50Hz is selected by default

4.4.11 Mode register 3

0x98	MODE3	Operating mode register	
No.	name	default value	description
[4]	isumlvl_sel	1'b0	When it is 0, compare the rms value of isumlvl and NI_RMS output neutral current; when it is 1, isumlvl and the rms value of the sum of the instantaneous waveforms of the output three-phase current;
[6:5]	period_sel	2'00	Line voltage frequency cycle measurement channel selection 2'b00-A; 2'b01-B; 2'b10-C; 2'b11-A. Affect the PERIOD (0x20) register
[7]	va_sel	1'b0	va algorithm selection: 0-RMS_I*RMS_V; 1-(watt^2+var^2)^0.5

[8]	add_sel	1'b0	Combination of watt and var accumulate method: 0-absolute value addition, |a|+|b|+|c|; 1-algebraic sum addition, a+b+c
[9]	cf_enable	1'b0	0-Close CF1/CF2 pulse output; 1-Allow CF1/CF2 pulse output
[13:10]	CF_SEL	4'b0000	CF1, CF2 output function selection, Default 0000, turn off CF1, CF2; 1111, turn off CF; 0001,watt_a/var_a electric energy CF; 0010,watt_b/var_b electric energy CF; 0011, watt_c/var_c electric energy CF; 0100, watt/var electric energy CF; 0101,watt_p_a/var1 electric energy CF; 0110,watt_p_b/var2 electric energy CF; 0111,watt_p_c/var3 electric energy CF; 1000,watt_p/var4 electric energy CF; 1001,watt_n_a/va_a electric energy CF; 1010,watt_n_/va_b electric energy CF; 1011, watt_n_c/va_c electric energy CF; 1100, watt_n/va electric energy CF 1101, (same as 0100); 1110, apparent energy CF;
[14]			Reserved
[15]	cf_add_sel	1'b0	watt and var energy addition methods: 0-absolute value addition; 1-algebra and addition (phase separation and combination)
[16]	var_sel	1'b0	Var energy selection: 0-fundamental wave; 1-full wave
[17]	watt_sel	1'b0	Watt waveform selection: 0-full wave; 1-fundamental wave
[18]		1'b0	Reserved

4.4.12 Interrupt status register

Interrupt register 1 0x54

Bit	Interrupt flag	Defaults	Description
0	SAG_A	0	Indicate the interruption of phase A SAG, the SAG event is 1
1	SAG_B	0	Indicate the interruption of B phase SAG
2	SAG_C	0	Indicate the interruption of B phase SAG
3	ZXTO_A	0	Indicates the phase A zero-crossing timeout interrupt is generated, the timeout event is 1
4	ZXTO_B	0	Indicates the phase B zero-crossing timeout interrupt is generated
5	ZXTO_C	0	Indicates that the phase C zero-crossing timeout interrupt is generated

6	ZX_VA	0	Indicate the sign bit of the phase A voltage waveform
7	ZX_IA		Indicate the sign bit of the phase A current waveform
8	ZX_VB		Indicate the sign bit of the phase B voltage waveform
9	ZX_IB		Indicate the sign bit of the phase B current waveform
10	ZX_VC		Indicate the sign bit of the phase C voltage waveform
11	ZX_IC		Indicate the sign bit of the phase C current waveform
12	ZX_IN		Indicate the sign bit of the N-phase current waveform
13	PK_VA	0	Indicates that the peak value of the effective value of the phase A voltage channel exceeds the PKVLVL interrupt, which is 1
14	PK_IA	0	Indicates that the peak value of the effective value of the phase A current channel exceeds PKILVL interrupt, which is 1
15	PK_VB	0	Indicates that the peak value of the effective value of the phase B voltage channel exceeds the PKVLVL interrupt, which is 1
16	PK_IB	0	Indicates that the peak value of the effective value of the phase B current channel exceeds the PKILVL interrupt, which is 1
17	PK_VC	0	Indicates that the peak value of the effective value of the phase C voltage channel exceeds PKVLVL interrupt, which is 1
18	PK_IC	0	Indicates that the peak value of the effective value of the phase C current channel exceeds PKILVL interrupt, which is 1
19	PK_NI	0	Indicates that the peak value of the effective value of the N-phase current channel exceeds the PKILVL interrupt, which is 1
20	pk_isum	0	Indicate three-phase current and exceed the threshold
21	Reserved	0	Reserved
22	Reserved	0	Reserved

Interrupt register 2 0x55

Bit	Interrupt flag	Defaults	Description
0	REVP_WATT_A	0	Indicates that the sign of the A phase active power calculation has changed
1	REVP_WATT_B	0	Indicates that the sign of the B-phase active power calculation has changed
2	REVP_WATT_C	0	Indicates that the sign of the C phase active power calculation has changed
3	REVP_VAR	0	Indicates that the sign of the A phase reactive power calculation has changed

4	REVP_VAR	0	Indicates that the sign of the B-phase reactive power calculation has changed
5	REVP_VAR	0	Indicates that the sign of the C-phase reactive power calculation has changed
6	REVP_FVAR	0	Indicates that the sign of the A phase fundamental reactive power calculation has changed
7	REVP_FVAR	0	Indicates that the sign of the B-phase fundamental reactive power calculation has changed
8	REVP_FVAR	0	Indicates that the sign of the C-phase fundamental reactive power calculation has changed
9			Reserved
10			Reserved
11			Reserved
12			Reserved
13			Reserved
14			Reserved
15	REVP_WATT	0	Indicates the sign change of the total active power calculation of the combined phase
16			Reserved
17	REVP_WATT_OR	0	Indicate the active power of any one of the three phases
18	REVP_VAR_OR	0	Indicate the sign change of any phase of the reactive power calculation in the three phases
19	REVP_FAVR_OR	0	Indicates that the fundamental reactive power calculation of any one of the three phases has a sign change
20			Reserved
21	VREF_LOW	0	Indicates that the reference voltage value is low, when it is 1, VREF<1V; when it is 0, it is normal
22	SPI_INPUT_ERR	0	SPI input check, when it is 1, the checksum is wrong; when it is 0, it is normal
23	UART_INPUT_ERR	0	UART input check, when it is 1, the checksum is wrong; when it is 0, it is normal

4.4.13 Interrupt mask register

Reg9A (MASK1) corresponds to the Reg54 (STATUS1) register bit, which controls whether an effective interrupt output is generated at the IRQ1 pin; the corresponding bit of the interrupt mask register is set to 1, then the corresponding interrupt is masked, and no signal is output at the IRQ pin.

Reg9B (MASK2) corresponds to the Reg55 (STATUS2) register bit, which controls whether to generate a valid interrupt output on the IRQ2 pin

IRQ1 and IRQ2 pins are 1 when there is no interrupt signal, and 0 when there is an interrupt signal;

For example, if you want to output the SAG_C interrupt signal on the IRQ1 pin, then MASK1=0xFFFFFB, MASK1[3] is set to 0, and other bits are set to 1, when a SAG_C event is detected, the IRQ1 pin is pulled low;

4.4.14 Clear the setting register after energy read

Addr	Name	Bit width	Defaults	Description
9D	RST_ENG	24	0x000000	Clear setting after reading the energy pulse count register

When Bit[23:0] is set to 1, the energy-related registers Reg46~2F are set to be cleared after reading. It can be set separately, RST_ENG[23:0] corresponds to REG46~2F, each bit controls the reset setting after reading a register.

4.4.15 User write protection setting register

Address	Name	Bit width	Defaults	Description
9E	USR_WRPROT	16	0x0000	User write protection setting register, when writing 0x5555, it means that it can be written into the calibration register Reg60~Reg9D, RegA0~RegD0

BL6552 has a strict protection mechanism for register writing. You must write 0x5555 to the write protection setting register before writing to other registers. Write other values other than 0x5555, and the calibration register is not allowed to be written.

4.4.16 Soft reset command

Address	Name	Bit width	Defaults	Description
9F	SOFT_RESET	24	0x000000	When the input is 5A5A5A, reset the electrical parameter register; When the input is 55AA55, the calibration register is reset: Reg60~reg9F, RegA0~RegD0

After writing 0x5555 in the Reg9E (USR_WRPROT) register, the system can be reset by writing to Reg9F;

Two-level reset mechanism:

1) Write 0x5A5A5A in Reg9F, reset the electrical parameter register, and clear the energy accumulation register to 0;

2) Write 0x55AA55 to Ref9F, reset the calibration register, Reg60~reg9F, RegA0~RegD0 load the power-on default value.

4.4.17 Channel gain adjustment register

Address	Name	Bit width	Defaults	Description
A1	IC_CHGN	16	0x0000	Current C channel gain adjustment register, complement
A2	IB_CHGN	16	0x0000	Current B channel gain adjustment register, complement
A3	IA_CHGN	16	0x0000	Current A channel gain adjustment register, complement
A4	IN_CHGN	16	0x0000	Current N channel gain adjustment register, complement
A7	VA_CHGN	16	0x0000	Voltage A channel gain adjustment register, complement
A8	VB_CHGN	16	0x0000	Voltage B channel gain adjustment register, complement
A9	VC_CHGN	16	0x0000	Voltage C channel gain adjustment register, complement

16-bit signed number, adjust the gain of the AD sampling waveform of the corresponding channel in the form of 2's complement, the adjustable range is ±50%

$$X\_WAVE = X\_WAVE0 * (1 + \frac{X\_CHGN}{2^{16}})$$

Where X_WAVE0 is the measured value of the corresponding channel, X_CHGN is the gain adjustment value of the corresponding channel, and X_WAVE is the output value after calibration.

4.4.18 Channel offset adjustment register

Address	Name	Bit width	Defaults	Description
AC	IC_CHOS	16	0x0000	Current C channel offset adjustment register, complement
AD	IB_CHOS	16	0x0000	Current B channel offset adjustment register, complement

AE	IA_CHOS	16	0x0000	Current A channel offset adjustment register, complement
AF	IN_CHOS	16	0x0000	Current N channel offset adjustment register, complement
B2	VA_CHOS	16	0x0000	Voltage A channel offset adjustment register, complement
B3	VB_CHOS	16	0x0000	Voltage B channel offset adjustment register, complement
B4	VC_CHOS	16	0x0000	Voltage C channel offset adjustment register, complement

The data in the form of 2's complement is used to eliminate the deviation caused by the analog-to-digital conversion of the current channel and the voltage channel respectively. The deviation here may be due to the input and offset produced by the analog-to-digital conversion circuit itself. Deviation correction can make the waveform offset to 0 under no load.

$$WAVE[N] = WAVE0[N] + CHOS[N]$$

Among them, WAVE0[N] is the measured value of the corresponding channel, CHOS[N] is the offset calibration value of the corresponding channel, and WAVE[N] is the output value after calibration.

4.4.19 Power gain adjustment register

Address	Name	Bit width	Defaults	Description
B6	WATTGN_A	16	0x0000	A phase active gain adjustment register, complement
B7	WATTGN_B	16	0x0000	B-phase active power gain adjustment register, complement
B8	WATTGN_C	16	0x0000	C-phase active power gain adjustment register, complement
B9	VARGN_A	16	0x0000	A phase reactive power gain adjustment register, complement
BA	VARGN_B	16	0x0000	B-phase reactive power gain adjustment register, complement
BB	VARGN _C	16	0x0000	C-phase reactive power gain adjustment register, complement
BC	FVARGN_A	16	0x0000	A phase fundamental reactive power

				gain adjustment register, complement
BD	FVARGN_B	16	0x0000	B-phase fundamental reactive power gain adjustment register, complement
BE	FVARGN_C	16	0x0000	C-phase fundamental reactive power gain adjustment register, complement
BF	VAGN_A	16	0x0000	A phase apparent power gain adjustment register, complement
C0	VAGN_B	16	0x0000	B-phase apparent power gain adjustment register, complement
C1	VAGN_C	16	0x0000	C-phase apparent power gain adjustment register, complement

Take the active power gain adjustment as an example, the description is as follows:

$$\mathrm{WATT[N]} = \mathrm{WATT0[N]} * (1 + \frac{WATTGN[N]}{2^{16}})$$

Among them, WATT[N] is the active power after the Nth correction, and WATT0[N] is the active power before the Nth correction. The adjustment range is ±50%.

Reactive power and apparent power gain correction formulas are similar;

4.4.20 Power offset adjustment register

Address	Name	Bit width	Defaults	Description
C2	WATTOS_A	16	0x0000	A phase active offset adjustment register, complement
C3	WATTOS_B	16	0x0000	B-phase active power offset adjustment register, complement
C4	WATTOS_C	16	0x0000	C-phase active power offset adjustment register, complement
C5	VAROS_A	16	0x0000	A phase reactive power offset adjustment register, complement
C6	VAROS_B	16	0x0000	B-phase reactive power offset adjustment register, complement
C7	VAROS_C	16	0x0000	C-phase reactive power offset adjustment register, complement
C8	FVAROS_A	16	0x0000	A phase fundamental reactive power offset adjustment register, complement
C9	FVAROS_B	16	0x0000	B-phase fundamental reactive power offset adjustment register, complement
CA	FVAROS_C	16	0x0000	C-phase fundamental reactive power

				offset adjustment register, complement
CB	VAOS_A	16	0x0000	A Phase Apparent Power offset adjustment register, complement
CC	VAOS_B	16	0x0000	B-phase apparent power offset adjustment register, complement
CD	VAOS_C	16	0x0000	C-phase apparent power offset adjustment register, complement

Complement, the sign bit of the most significant bit. Used to eliminate power deviation caused by board-level noise.

Take the active power offset correction as an example, the description is as follows:

$$WATT[N] = WATT0[N] + \frac{WATTOS[N]}{2}$$

Among them, WATT0[N] is the measured value of a certain phase, WATTOS[N] is the corresponding offset correction value, and WATT[N] is the corresponding calibration output value.

The offset correction formulas for reactive power and apparent power are similar;

4.4.21 CF scaling register

Used to control the accumulation speed of electric energy pulse counting, the default setting of BL6552 is 0x10

Address	Name	Bit width	Defaults	Description
CE	CFDIV	12	0x010	CF scaling register [11:0]

Take the frequency of energy pulse counting when CFDIV=0x10 as the standard frequency, and the multiples of energy pulse counting in other settings are as follows:

CFDIV	Counting magnification	CFDIV	Counting magnification
0x00	0.03125	0x40	4
0x01	0.0625	0x80	8
0x02	0.125	0x100	16
0x04	0.25	0x200	32
0x08	0.5	0x400	64
0x10	1	0x800	256

0x20	2	其他值	1

4.4.22 AT1~3 logic output pin configuration register

Used to configure the function of AT1~AT3 logic output pins

Address	Name	Bit width	Defaults	Description
CF	AT_SEL	9	0x000	Bit[8:5] is AT1~AT3 logic output pin function configuration Bit[4:0] reserved

AT_SEL [8:5]	AT1 output	AT2 output	AT3 output
0000	SAG_A	SAG_B	SAG_C
0001	CFA_WA	CFB_WA	CFC_WA
0010	ZX_VA	ZX_VB	ZX_VC
0011	ZX_IA	ZX_IB	ZX_IC
0100	PK_IA	PK_IB	PK_IC
0101	PK_VA	PK_VB	PK_VC
0110	Reserved	SAG(Three-phase or)	Reserved
0111	REVPVAR	VREF_LOW	Reserved
1000	REVPAP_A	REVPAP_B	REVPAP_C
1001	REVPRP_A	REVPRP_B	REVPRP_C
1010	REVPRP	REVPVAR	REVPAP
1011	SPI_INPUT_ERR	UART_INPUT_ERR	REVPWATT

Function	Defaults	Description
REVPAP_A	0	Indicates that the sign of the A phase active power calculation has changed
REVPRP_A	0	Indicates that the sign of the A phase reactive power calculation has changed
REVPAP_B	0	Indicates that the sign of the B phase active power calculation has changed
REVPRP_B	0	Indicates that the sign of the B phase reactive power calculation has changed
REVPAP_C	0	Indicates that the sign of the C phase active power calculation has changed
REVPRP_C	0	Indicates that the sign of the C phase reactive power calculation has changed
REVPWATT	0	Indicate the sign change of the active power calculation of any one of the three phases
REVPVAR	0	Indicate the sign change of any phase of the reactive power calculation in the three phases

REVPAP	0	Indicates the sign change of the total active power calculation of the combined phase
REVPRP	0	Indicates that the sign of the total reactive power calculation of the combined phase has changed
SPI_INPUT_ERR	0	SPI input check, when it is 1, the checksum is wrong;
UART_INPUT_ERR	0	UART input check, when it is 1, checksum error;
VREF_LOW	0	Indicates that the reference voltage value is low, when it is 1, VREF<1V; when it is 0, it is normal
SAG_A	0	Indicate the interruption of A phase line voltage drop, the drop is 1
SAG_B	0	Indicate the interruption of B phase line voltage drop, the drop is 1
SAG_C	0	Indicate the interruption of the voltage drop of the C phase line, the drop is 1
ZXTO_A	0	Indicates the generation of A phase zero-crossing timeout interrupt, the timeout is 1
ZXTO_B	0	Indicates that B phase zero-crossing timeout interrupt is generated, and the timeout is 1
ZXTO_C	0	Indicates that the C phase zero-crossing timeout interrupt is generated, and the timeout is 1
ZX_VA	0	Indicate the sign bit of the A phase voltage waveform
ZX_IA	0	Indicate the sign bit of the A phase current waveform
ZX_VB	0	Indicate the sign bit of the B phase voltage waveform
ZX_IB	0	Indicate the sign bit of the B phase current waveform
ZX_VC	0	Indicate the sign bit of the C phase voltage waveform
ZX_IC	0	Indicate the sign bit of the C phase current waveform
ZX_IN	0	Indicate the sign bit of the N-phase current waveform
PK_VA	0	Indicates that the instantaneous peak value of the A phase voltage channel exceeds the PKVLVL interrupt, which is 1
PK_IA	0	Indicates that the instantaneous peak value of the A phase current channel exceeds the interruption of PKILVL, which is 1
PK_VB	0	Indicates that the instantaneous peak value of B phase voltage channel exceeds PKVLVL interrupt, which is 1
PK_IB	0	Indicates that the instantaneous peak value of the B phase current channel exceeds the interruption of PKILVL, which is 1
PK_VC	0	Indicates that the instantaneous peak value of the C phase voltage channel exceeds PKVLVL interrupt, which is 1
PK_IC	0	Indicates that the instantaneous peak value of the C-phase current channel exceeds the interruption of PKILVL, which is 1

PK_NI	0	Indicates that the instantaneous peak value of the N-phase current channel exceeds the interruption of PKILVL, which is 1
pk_isum	0	Indicate three-phase current and exceed the threshold

4.5 Detailed description of electrical parameter registers

4.5.1 Wave register

Address	Name	Bit width	Defaults	Description
2	IC_WAVE	24	0x000000	C-phase current waveform register
3	IB_WAVE	24	0x000000	B phase current waveform register
4	IA_WAVE	24	0x000000	A phase current waveform register
5	IN_WAVE	24	0x000000	Neutral current waveform register
8	VA_WAVE	24	0x000000	A phase voltage waveform register
9	VB_WAVE	24	0x000000	B phase voltage waveform register
A	VC_WAVE	24	0x000000	C phase voltage waveform register

Waveform data of real-time sampling points, sampling clock 4MHz, 4MHz/256/50=312.5, about 312 sampling points per cycle.

4.5.2 RMS register

Address	Name	Bit width	Defaults	Description
D	IC_RMS	24	0x000000	C-phase current RMS register, unsigned
E	IB_RMS	24	0x000000	B-phase current RMS register, unsigned
F	IA_RMS	24	0x000000	A phase current RMS register, unsigned
10	IN_RMS	24	0x000000	Neutral RMS current register, unsigned
13	VA_RMS	24	0x000000	A phase voltage RMS register, unsigned
14	VB_RMS	24	0x000000	B phase voltage RMS register, unsigned
15	VC_RMS	24	0x000000	C-phase voltage RMS register, unsigned

By setting the RMS_UPDATE_SEL of MODE2[22], the average refresh time of the effective value can be selected to be 525ms or 1.05s, and the default is 525ms.

The corresponding formula (typical value) of the register value and the input signal:

Current RMS register: $I\_RMS = \frac{12875*I(A)*Gain\_I}{Vref}$

Voltage RMS register: $V\_RMS = \frac{13162*V(V)*Gain\_V}{Vref}$

Vref is the reference voltage, and the typical value is 1.097V.

I(A), V(V) are the voltage signals of the current and voltage input pins (unit: mV); Gain_I, Gain_V are the corresponding channel gain multiples;

4.5.3 Fast RMS register

Address	Name	Bit width	Defaults	Description
18	IC_FAST_RMS	24	0x000000	C-phase current fast RMS register, unsigned
19	IB_FAST_RMS	24	0x000000	B-phase current fast RMS register, unsigned
1A	IA_FAST_RMS	24	0x000000	A phase current fast RMS register, unsigned
1B	IN_FAST_RMS	24	0x000000	Neutral Line current fast RMS register, unsigned
1E	VA_FAST_RMS	24	0x000000	A phase voltage fast RMS register, unsigned
1F	VB_FAST_RMS	24	0x000000	B-phase voltage fast RMS register, unsigned
20	VC_FAST_RMS	24	0x000000	C-phase voltage fast RMS register, unsigned

It can be used for fast current and voltage detection. The detection cycle and refresh time can be set by the FAST_RMS_CTRL register. It should be noted that the smaller the detection period, the greater the jump of the register value. Using arithmetic average algorithm, the measurement accuracy is lower than the effective value.

$$I[N]\_FAST\_RMS \approx I[N]\_RMS * 0.55$$

4.5.4 Active power register

Address	Name	Bit width	Defaults	Description

22	WATT_A	24	0x000000	A-phase active power register
23	WATT_B	24	0x000000	B-phase active power register
24	WATT_C	24	0x000000	C-phase active power register
25	WATT	24	0x000000	Combined phase active power register

The active power register is signed 24-bit data, complemented. The highest bit is the sign bit, Bit[23]=1, indicating that the current power is negative;

$$WATT = \frac{SUM(WATT[N])}{4}$$

The calculation formula of each split-phase active power register (typical value):

$$\text{WATT[x]}\boldsymbol{register\ value} = \frac{40.4125 * \text{I}_\text{N}(\text{A}) * \text{Gain\_I} * V_N(\text{V}) * \text{Gain\_V} * \text{Cos}(\emptyset)}{\text{Vref}^2}$$

Among them, I_N (A) and V_N (V) are the effective value (mV) of the channel pin input voltage, and Vref is the built-in reference voltage, with a typical value of 1.097V. The value 40.4125 is a typical value coefficient. Gain_I is the current channel gain multiple, and Gain_V is the voltage channel gain multiple.

4.5.5 Reactive power register

Address	Name	Bit width	Defaults	Description
5A	VAR_A	24	0x000000	A Phase (full wave) reactive power register
5B	VAR_B	24	0x000000	B Phase (full wave) reactive power register
5C	VAR_C	24	0x000000	C-phase (full wave) reactive power register
5D	VAR	24	0x000000	Combined phase (full wave) reactive power register
2A	FVAR_A	24	0x000000	A Phase (fundamental wave) reactive power register
2B	FVAR_B	24	0x000000	B Phase (fundamental wave) reactive power register
2C	FVAR_C	24	0x000000	C-phase (fundamental wave) reactive power register

2D	FVAR	24	0x000000	Combined phase (fundamental) reactive power register

Signed 24-bit data, complement. Bit[23] is the sign bit, =1, indicating that the current power is negative;

$$VAR = \frac{SUM(VAR[N])}{4}$$

Fundamental reactive power register is similar to reactive power register;

Calculation formula of each split-phase reactive power register (typical value):

$$\text{VAR[x]}\boldsymbol{register\ value} = \frac{40.4125 * \text{I}_\text{N}(\text{A}) * \text{Gain\_I} * V_N(\text{V}) * \text{Gain\_V} * \text{Sin}(\emptyset)}{\text{Vref}^2}$$

Among them, I_N (A) and V_N (V) are the effective value (mV) of the channel pin input voltage, and Vref is the built-in reference voltage, with a typical value of 1.097V. The value 40.4125 is a typical value coefficient. Gain_I is the current channel gain multiple, Gain_V is the voltage channel gain multiple.

4.5.6 Apparent power register

Address	Name	Bit width	Defaults	Description
26	VA_A	24	0x000000	A phase apparent power register
27	VA_B	24	0x000000	B phase apparent power register
28	VA_C	24	0x000000	C-phase apparent power register
29	VA	24	0x000000	Combined apparent power register

Unsigned 24-bit data

$$VA = \frac{SUM(VA[N])}{4}$$

The calculation formula of each split phase apparent power register (typical value):

$$\text{VA[x]}\boldsymbol{register\ value} = \frac{40.4125 * \text{I}_\text{N}(\text{A}) * \text{Gain\_I} * V_N(\text{V}) * \text{Gain\_V}}{\text{Vref}^2}$$

Among them, I_N (A) and V_N (V) are the effective value (mV) of the channel pin input voltage, and Vref is the built-in reference voltage, with a typical value of

1.097V. The value 40.4125 is a typical value coefficient. Gain_I is the current channel gain multiple, and Gain_V is the voltage channel gain multiple.

4.5.7 Energy pulse count register

Address	Name	Bit width	Defaults	Description
2F	CF_A_CNT	24	0x000000	A phase active pulse count, unsigned
30	CF_B_CNT	24	0x000000	B phase active pulse count, unsigned
31	CF_C_CNT	24	0x000000	C phase active pulse count, unsigned
32	CF_CNT	24	0x000000	Combined phase active pulse count, unsigned
33	CFP_A_CNT	24	0x000000	A positive active phase pulse count, unsigned
34	CFP_B_CNT	24	0x000000	B positive active phase pulse count, unsigned
35	CFP_C_CNT	24	0x000000	C positive active phase pulse count, unsigned
36	CFP_CNT	24	0x000000	Combined positive active phase pulse count, unsigned
37	CFN_A_CNT	24	0x000000	A negative active phase pulse count, unsigned
38	CFN_B_CNT	24	0x000000	B negative active phase pulse count, unsigned
39	CFN_C_CNT	24	0x000000	C negative active phase pulse count, unsigned
3A	CFN_CNT	24	0x000000	Combined negative active phase pulse count, unsigned
3B	CFQ_A_CNT	24	0x000000	A phase reactive pulse count, unsigned
3C	CFQ_B_CNT	24	0x000000	B phase reactive pulse count, unsigned
3D	CFQ_C_CNT	24	0x000000	C phase reactive pulse count, unsigned

3E	CFQ_CNT	24	0x000000	Combined phase reactive pulse count, unsigned
3F	CFQ1_CNT	24	0x000000	The first quadrant reactive pulse count, unsigned
40	CFQ2_CNT	24	0x000000	The second quadrant reactive pulse count, unsigned
41	CFQ3_CNT	24	0x000000	The third quadrant reactive pulse count, unsigned
42	CFQ4_CNT	24	0x000000	The fourth quadrant reactive pulse count, unsigned
43	CFS_A_CNT	24	0x000000	A phase apparent pulse count, unsigned
44	CFS_B_CNT	24	0x000000	B-phase apparent pulse count, unsigned
45	CFS_C_CNT	24	0x000000	C-phase apparent pulse count, unsigned
46	CFS_CNT	24	0x000000	Combined apparent pulse count, unsigned

The energy pulse count is related to the CFDIV register. The larger the CFDIV register setting value, the faster the pulse count.

Cumulative time of each split-phase CF pulse

$$t_{CF\_X} \approx \frac{4194304 * 0.032768 * 16}{CFDIV * WATT\_X寄存器值}$$

The typical value of the pulse frequency when the current and voltage are input at full amplitude is as follows:

Input 480mV rms according to current and voltage full scale

CFDIV			Split phase CF_X	Split phase CF_SUM
Hexadecimal	Decimal	Magnification	Full-scale frequency Hz	Full-scale frequency Hz
0	0	0.03125	1.85	1.39
1	1	0.0625	3.71	2.78
2	2	0.125	7.42	5.56
4	4	0.25	14.84	11.13
8	8	0.5	29.67	22.25
10	16	1	59.34	44.51
20	32	2	118.68	89.01
40	64	4	237.36	178.02
80	128	8	474.72	356.04

100	256	16	949.44	712.08
200	512	32	1898.88	1424.16
400	1024	64	3797.76	2848.32
800	2048	256	15191.04	11393.28

MODE3[15] is used to set the accumulation mode of electric energy pulse counting: algebraic and/absolute value mode;

RST_ENG register is used to set whether the energy pulse counting register is cleared after reading;

Take the active pulse count register as an example to illustrate as follows:

$$CF\_CNT = \frac{SUM(CF\_X\_CNT[N])}{4}$$

4.5.8 Waveform angle register

Address	Name	Bit width	Defaults	Description
4E	ANGLE_AB	16	0x000000	Waveform angle register of voltage A phase and voltage B phase
4F	ANGLE_BC	16	0x000000	Waveform angle register of voltage B phase and voltage C phase
50	ANGLE_AC	16	0x000000	Waveform angle register of voltage A phase and voltage C phase
51	ANGLE_A	16	0x000000	A phase voltage and current waveform angle register
52	ANGLE_B	16	0x000000	B phase voltage and current waveform angle register
53	ANGLE_C	16	0x000000	C phase voltage and current waveform angle register

It should be noted that when the current is less than a certain value, the angle register stops working

$$angle(^{\circ}) = \frac{360 * ANGLE[N] * f_c}{500000}$$

fc is the measurement frequency of the AC signal source, the default is 50Hz

4.5.9 Power factor register

Address	Name	Bit width	Defaults	Description
47	PF_A	24	0x000000	A phase power factor register
48	PF_B	24	0x000000	B phase power factor register
49	PF_C	24	0x000000	C phase power factor register
4A	PF	24	0x000000	Combined phase power factor register

24-bit signed number, complement. Bit[23] is the sign bit,

$$power\ factor = \frac{PF}{2^{23}}$$

4.5.10 Line voltage frequency register

Address	Name	Bit width	Defaults	Description
2E	PERIOD	20	0x000000	Line voltage frequency period register

Measure the frequency of the sine wave signal of the selected voltage channel

$$\boldsymbol{Line\ voltage\ frequency} = \frac{10000000}{PERIOD}\ \text{Hz}$$

The measurement channel of line voltage frequency can be set through MODE3[6:5], the default is phase A;

5、 Communication Interface

Register data is sent in 3 bytes (24bit). For register data less than 3 bytes, add 0 to the unused bits and send together 3 bytes.

It is selected by pin SEL, when SEL=1 it is SPI, when SEL=0 it is UART

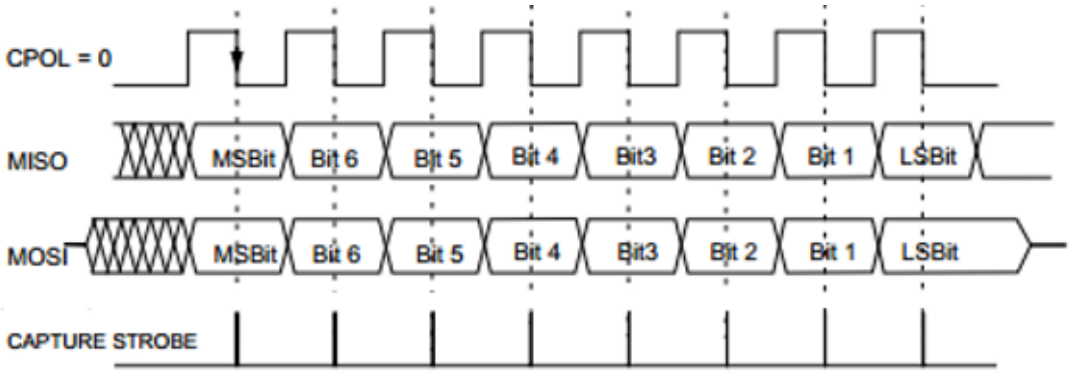
5.1 SPI

5.1.1 Overview

- ✓ Slave mode, half-duplex communication, maximum communication speed 1.5M
- ✓ 8-bit data transmission, MSB in the front, LSB in the back
- ✓ Fix a clock polarity/phase (CPOL=0, CPHA=1)

5.1.2 Operating mode

The master device works in Mode1: CPOL=0, CPHA=1, that is, in idle state, SCLK is at low level, and data transmission is on the first edge, that is, the transition of SCLK from low to high, so Data sampling is on the falling edge, and data transmission is on the rising edge.



5.1.3 Frame structure

In the communication mode, first send the 8bit identification byte (0x81) or (0x82), (0x82) is the read identification byte, (0x81) is the write identification byte, and then send the register address byte to determine the address of the access register (Please refer to the BL6552 register list). The following figure shows the data transfer sequence of read and write operations respectively. After one frame of data transmission is completed, BL6552 enters the communication mode again. The number of SCLK pulses required for each read/write operation is 48 bits.

There are two types of frame structures, which are explained as follows:

1） Write register

Cmd: {0x81}+ Addr+Data_H+Data_M+Data_L+SUM

{0x81} is the frame identification byte of the write operation;;

Addr is the internal register address of BL6552 corresponding to the write operation;

Where the checksum byte CHECKSUM is (((0x81)+ADDR+DATA_H+DATA_M+DATA_L)& 0xFF) and then inverted by bit.

写操作帧	0x81	ADDR[7:0]	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

2） Read register

Cmd:{0x82}+Addr

Returns: Data_H+Data_M+Data_L+SUM

{0x82} is the frame identification byte of the read operation;

Addr is the internal register address of BL6552 corresponding to the read operation (0x00-0xff);

Among them, the checksum byte CHECKSUM is （({0x82}+ADDR+DATA_H+DATA_M+DATA_L）& 0xFF）and then inverted by bit.

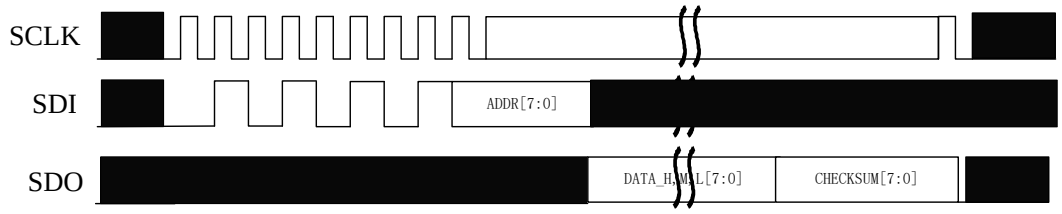
读命令帧	0x82	ADDR[7:0]

读数据帧	DATA_H[7:0]	DATA_M[7:0]	DATA_L[7:0]	CHECKSUM[7:0]

5.1.4 Read operation timing

During the data read operation of BL6552, at the rising edge of SCLK, BL6552 shifts the corresponding data out to the DOUT logic output pin. During the following time when SCLK is 1, the value of DOUT remains unchanged, that is, at the next At

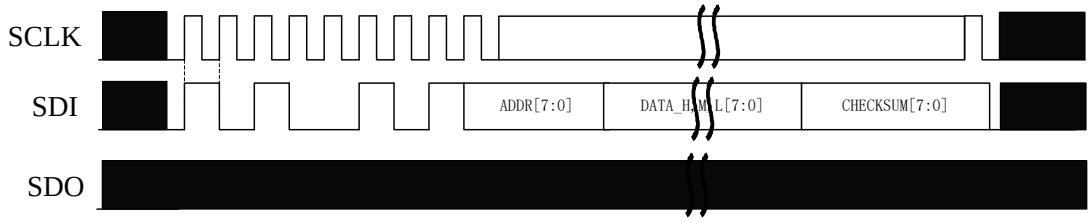
the falling edge, the external device can sample the DOUT value. As with the data write operation, the MCU must first send the identification byte and address byte before the data read operation.



When BL6552 is in communication mode, the frame identification byte {0x82} indicates that the next data transfer operation is read. Then the following byte is the address of the target register to be read. BL6552 starts to shift out the data in the register on the rising edge of SCLK. All remaining bits of the register data are shifted out on the subsequent rising edge of SCLK. Therefore, on the falling edge, the external device can sample the output data of the SPI. Once the read operation is over, the serial interface re-enters the communication mode. At this time, the DOUT logic output enters a high impedance state on the falling edge of the last SCLK signal.

5.1.5 Write operation timing

The serial writing sequence is performed as follows. The frame identification byte {0x81} indicates that it is written during a data transfer operation. MCU prepares the data bits that need to be written into BL6552 before the lower edge of SCLK, and starts to shift in register data at the lower edge of the clock of SCLK. All the remaining bits of the register data are also shifted to the left on the lower edge of the SCLK.



5.1.6 Fault tolerance mechanism of SPI interface

1）If the frame recognition byte is wrong or the SUM byte is wrong, the frame data is abandoned；

2）SPI module reset: send 6 bytes of 0xFF through the SPI interface, and the SPI interface can be reset separately；

3) CS pull high to reset;

5.2 UART

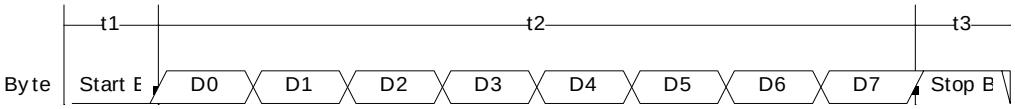
5.2.1 Overview

It is selected by pin UART_SEL, when SEL=1 it is SPI, when SEL=0 it is UART Communication baud rate is 4800bps/9600bps/19200bps/38400bps/, no parity, stop bit 1;

Baud rate setting	4800	9600	19200	38400
CS pin	0	0	1	1
SCLK pin	0	1	0	1

In UART mode, CS and SCLK pins are used as baud rate setting pins.

5.2.2 Format per byte

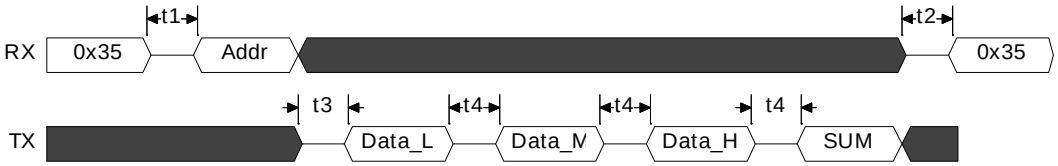


Start bit low level duration t1=208us (4800bps);

The valid data bit time lasts t2=208*8=1664us(4800bps);

Stop bit high level duration t3=2*208u(4800bps)s;

5.2.3 Read timing



The host UART read data sequence is shown in the figure below. The host first sends the command byte (0x35), then the address byte (ADDR) that needs to be read, then BL6552 sends the data byte in turn, and finally the checksum byte.

{0x35} is the frame identification byte of the read operation;

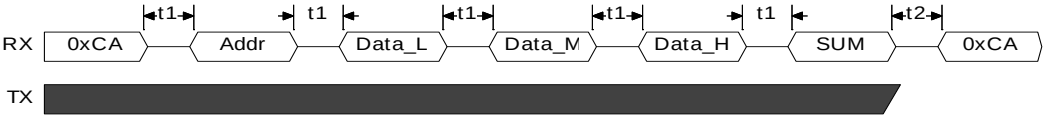
Addr is the internal register address of BL6552 corresponding to the read operation (0x00-0xff);

The SUM byte is (Addr+Data_L+Data_M+Data_H) & 0xFF reverse;

	Description	Min	Type	Max	Unit

t1	The interval between MCU sending bytes	0		20	mS
t2	Frame interval	0.5			uS
t3	The interval time from the end of MCU sending register address to BL050 sending byte during read operation		110		uS
t4	Interval time between BL6552 sending bytes		1		Bit

5.2.4 Write timing



The host UART write data sequence is shown in the figure below. The host first sends the command byte (0xCA), then the write address byte (ADDR), then sends the data byte in turn, and finally the checksum byte.

{0xCA} is the frame identification byte of the write operation;

Addr is the internal register address of BL6552 corresponding to the write operation;

The CHECKSUM byte is ((ADDR+Data_L+Data_M+Data_H) & 0xFF) and then inverted by bit.

5.2.5 Protection mechanism of UART interface

1) The UART communication of BL6552 provides a time-out protection mechanism. If the interval between bytes exceeds 18.5mS, the UART interface will automatically reset.
2) If the frame recognition byte is wrong or the checksum byte is wrong, the frame

data is abandoned.

3) UART module reset: The RX pin is pulled high after the low level exceeds 32bps (6.67ms at 4800 bps), and the UART module is reset.

6、 Package information

6.1 order information

BL6552 QFN36 PACKAGE

6.2 Package

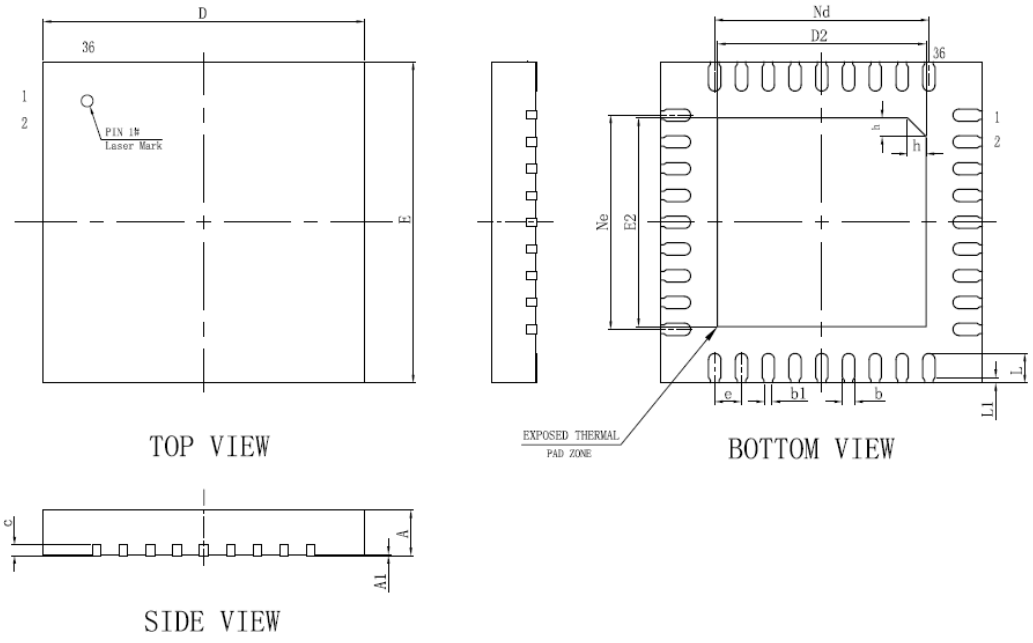
Moisture sensitivity level MSL 3

Warranty period: two years

Packing method Taping

Minimum packaging 4000/reel

6.3 Package appearance



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.23	0.30
b1	0.16REF		
c	0.18	0.20	0.23
D	5.90	6.00	6.10
D2	3.80	3.90	4.00
Nd	3.95	4.00	4.05
e	0.50BSC		
E	5.90	6.00	6.10
E2	3.80	3.90	4.00
Ne	3.95	4.00	4.05
L	0.50	0.55	0.60
L1	0.10REF		
h	0.30	0.35	0.40
L/F载体尺寸 (MIL)	181X181		