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BL6562 ACTIVE PFC CONTROLER

1 Features

- Transition-mode control
- Low start-up current (<70uA)
- Ultra-low quiescent current≤2mA
- Ultra-low operating current≤2.2mA
- Large IC supply voltage operating range
- Supply current≤1mA after disable
- 1%(@T_j=25°C) internal reference voltage
- System operation protection:
  Dynamic and static over voltage protection
  Under-voltage lockout function
  Peak current limited
  Supply voltage upper clamped
  Output voltage upper clamped
- -400mA/+600mA totem pole output driver with UVLO pull-down

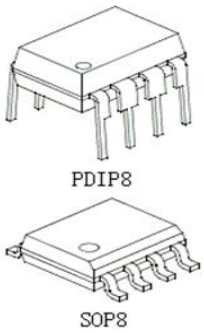


Figure1 PACKAGES

Applications

- LED Light Driver
- Electronic Ballast
- AC/DC Adapter

2 General descriptions

BL6562 is an active power factor correct controller operating in transition mode, which is mainly used in small power electronic ballast, LED light driver and AC/DC adapter.

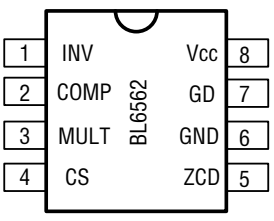
Realised in advanced BCD technology, BL6562 features ultra-low start-up current and operating current (≤ 2.2mA @12V). Remote IC DISALBE function can make it work at power saving mode.

BL6562 includes an internal highly linear multiplier, able to provide a high power factor in wide-range-mains operation and over a large range load change. The max current of the MOSFET is limited to the upper clamp output voltage of the multiplier.

Dynamic and static over-voltage protection, internal supply voltage upper clamp、under voltage lockout and output upper clamp functions can make the system work safely.

-400mA/+600mA totem pole output driver is capable of driving large power MOSFET and IGBT.

Figure 2 Pin connection



8 LEAD SOP or DIP

Table 1 Pin description

Pin	Symbol	Function description
1	INV	Inverting input of the error amplifier.
2	COMP	Output of the error amplifier and one input of the multiplier.
3	MULT	One input of the multiplier.
4	CS	One input of Current sense comparator. An internal low pass filter is placed to reduce high frequency interface.
5	ZCD	Zero current detection input and disable function pin. When the voltage is smaller than 130mV, the device is disabled.
6	GND	Ground.
7	GD	Gate driver output. The typical upper output clamp voltage is 12V.
8	Vcc	Supply input. Supply voltage of UVLO block, voltage regulator and output driver. The upper limit is extended to 24V min.

Figure 3 Block diagram

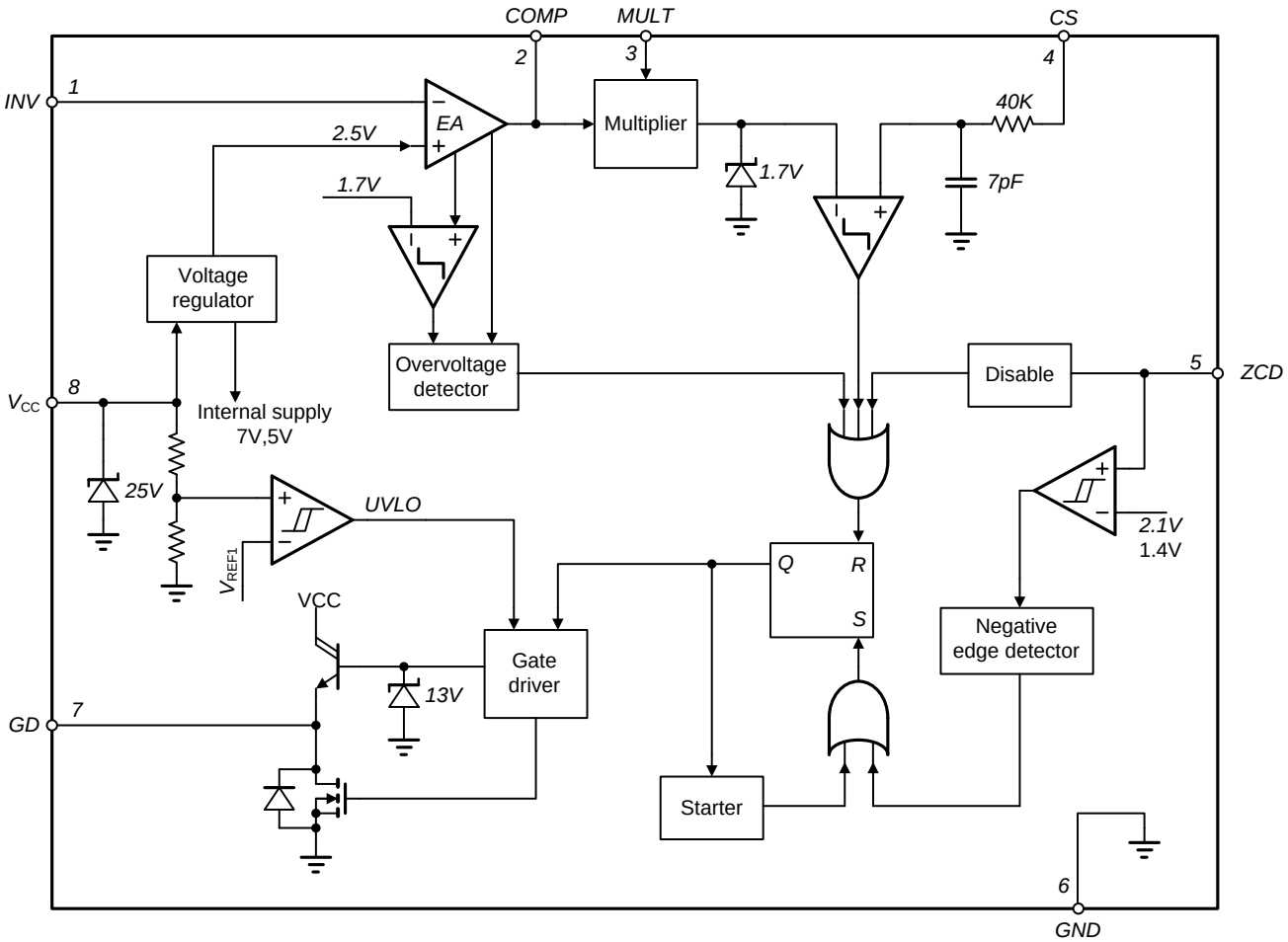


Table 2 Absolute maximum ratings

Parameter	symbol	Value	Unit
Supply voltage	V_{CC}	24.5	V
inputs and outputs voltages(Pin1~4)		-0.3~8	V
Zero current detector current	I_{ZCD}	+/-10	mA
Gate driver output voltage	V_{GD}	-0.3~self-limited	
Power dissipation@50°C(DIP-8)	P_{total}	1	W
Power dissipation@50°C(SO-8)	P_{total}	0.65	W
Junction temperature operating range	T_j	-40~150	°C
Storage temperature	T_{stg}	-55~150	°C
ESD(HBM) voltage	V_{ESD}	>4000	V
Latch up current	$I_{Latchup}$	>200	mA

Table3 Electrical characteristics

（T=25°C，V_{cc}=12V，C_O=1nF；unless otherwise specifed）

symbol	parameter	Test condition	min	typ	max	unit
Supply block						
V_{cc-on}	Turn-on threshold		11	12	13	V
V_{cc-off}	Turn-off threshold		9	9.5	10.2	V
V_{cc}	Operating rang	After turn-on	10.3		24	V
$V_{cc,clamp}$	Upper clamp voltage	I_{CC}=20mA	24.5	25.8	28	V
V_{R25}	2.5V reference voltage	T=25°C	2.475	2.5	2.525	V
		10.3V<V_{CC}<24	2.45		2.55	
Supply current						
I_{st}	Start-up current	V_{CC}=11V before turn on		40	70	uA
I_q	Quiescent current			1.3	2	mA
I_{cc}	Operating current	@70kHz		1.5	2.2	mA
I_{qsdis}	Quiescent current when DISABLE	V_{zcd}=120mV		0.67	1	mA
I_{qsovp}	Quiescent current when OVP	OVP		1.3	2	mA
Multiplier block						
I_{mul}	Input bias current	V_{mult}= 4V			-1	uA
L_{mul}	Linear operating range		0~3			V
k_{max}	Max slope	V_{mult}=0~0.5V, V_{comp}=5.2V	1.6	1.9		V/V
K	Gain(1)	V_{mult}=1V,Vcomp=4V	0.5	0.6	0.7	1/V
$V_{multoffset}$	Multiplier offset	$V_{mult=}$0V		27		mV
		$V_{mult=}$2.5V		5		mV
$V_{multclamp}$	Output clamp voltage	V_{comp}=5.2V	1.6	1.7	1.8	V

Table 3 Electrical characteristics (continued)

（T=25°C，Vcc=12V，C_O=1nF；unless otherwise specified）

Error amplifier block						
I_{inv}	Input bias current	V_{inv}= 3V			-1	uA
Av	Open loop voltage gain		60	80		dB
GBW	Gain Bandwidth			1		MHz
I_{comp}	Source current	V_{comp}=4V, V_{inv}=2.4V	-2	-3.5	-5	mA
	Sink current	V_{comp}=4V, V_{inv}=2.6V	4	6		mA
V_{comp}	upper clamp voltage	I_{source}=-0.5mA	5.2	5.35	5.8	V
	Lower clamp voltage	I_{sink}=0.5mA	0.8	1	1.2	V
Over voltage protector						
I_{ovp}	Dynamic OVP threshold current		24	39	45	uA
Hys		(2)		20		uA
V_{ovp}	Static OVP threshold voltage	(2)	1.6	1.7	1.8	V
Current sense block						
I_{cs}	Input bias current	V_{cs}=0			-1	uA
$t_{d(H-L)}$	Delay to output			250	350	ns
Zero current detector block						
$V_{zcd(H)}$	Upper clamp voltage	I_{zcd}=2.5mA	5	5.8	6.5	V
$V_{zcd(L)}$	Lower clamp voltage	I_{zcd}=-2.5mA	0.3	0.55	0.8	V
I_{zcdb}	Input bias current	V_{zcd}=1 to 4.5V		2		uA
V_{ZCDA}	Positive triggering voltage	(2)		2.1		V
V_{ZCDT}	Negative triggering voltage	(2)		1.4		V
I_{zcdsor}	Source current capability		-2.5		-5.5	mA
$I_{zcdsink}$	Sink current capability		2.5			mA
V_{zcddis}	Disable threshold		130	160	190	mV
V_{zcden}	Enable threshold		250	280	310	mV
Izcdres	Restart current		40	80		uA
Starter block						
f_{start}	Starter frequency		5	9	16	KHz
Output gate driver block						
V_{oh}	Output voltage	$I_{GDsource}$=20mA	9.8	10.3		V
		$I_{GDsource}$=200mA	8	8.3		V
V_{ol}		I_{GDsink}=200mA		1	1.9	V
tf	Fall time			32	70	ns
tr	Rise time			45	85	ns
V_{oclamp}	Output clamp voltage	V_{cc}=20V, $I_{GDsource}$=5mA	11	12	13	V
V_{o-uvlo}	Output voltage before turn on	V_{cc}=0~V_{CCon}, I_{GDsink}=10mA			1	V

(1) K= V_{CS}/ [V_{mult}*(V_{comp}-2.5)]

(2)Parameters guaranteed by design.

3 Application information

Figure 4 Wide-range mains demo board BL6562-80W: schematic

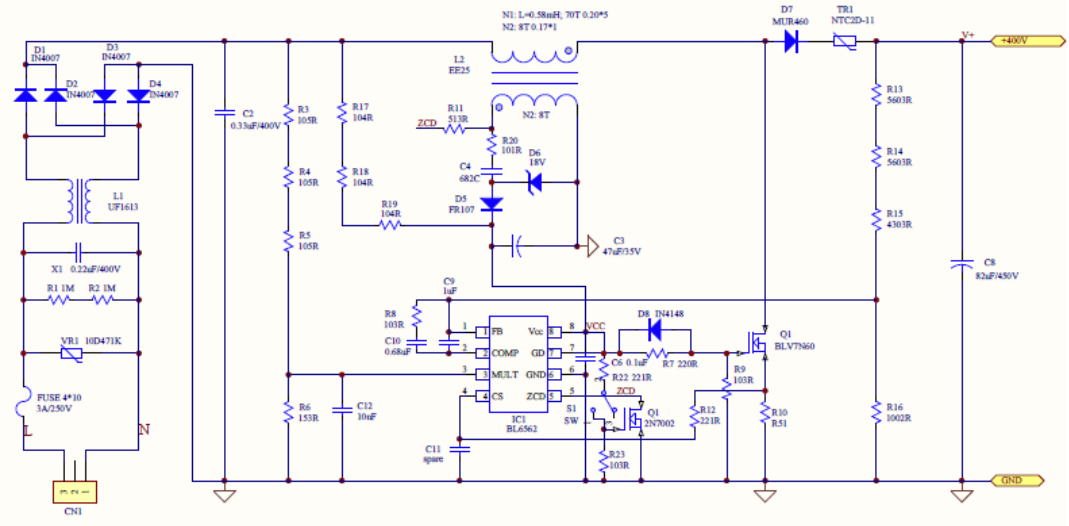


Figure 5 Wide-range mains demo board BL6562-80W: PCB layout

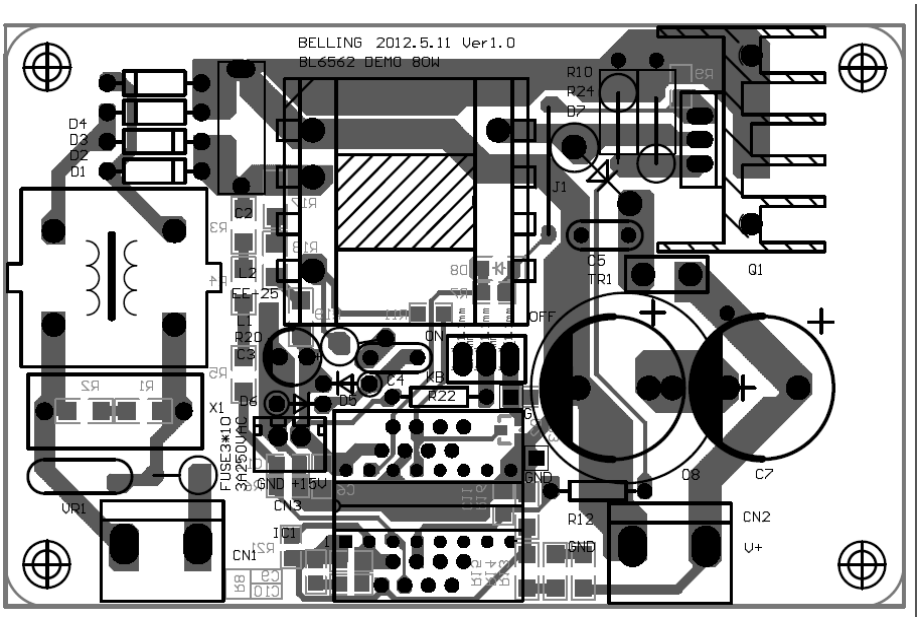
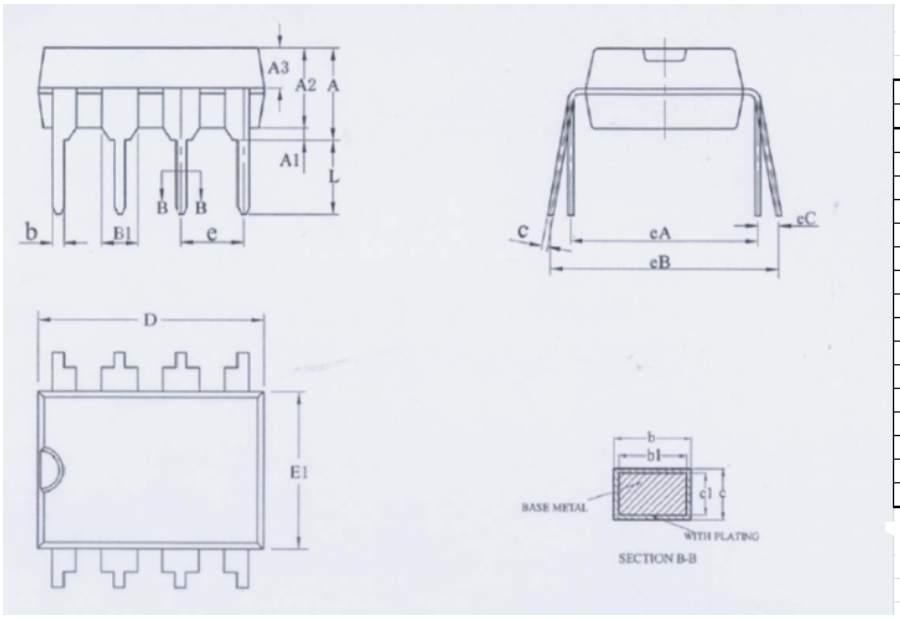


Table 4 BL6562-80W test results

Vin (V_{AC})	P_{in} (W)	V_o (V_{DC})	ΔV_o(V_{pp})	P_o (W)	η (%)	PF	THD(%)
85	86.6	391.75	15	80.19	92.6	0.998	3.4
110	84.7	391.83	15	80.21	94.7	0.998	4.6
135	83.8	391.83	15	80.21	95.7	0.997	5.4
175	83.2	391.85	15	80.21	96.4	0.997	5.8
220	82.9	391.87	15	80.21	96.8	0.991	6.7
265	82.7	391.87	15	80.21	97.0	0.978	8.2

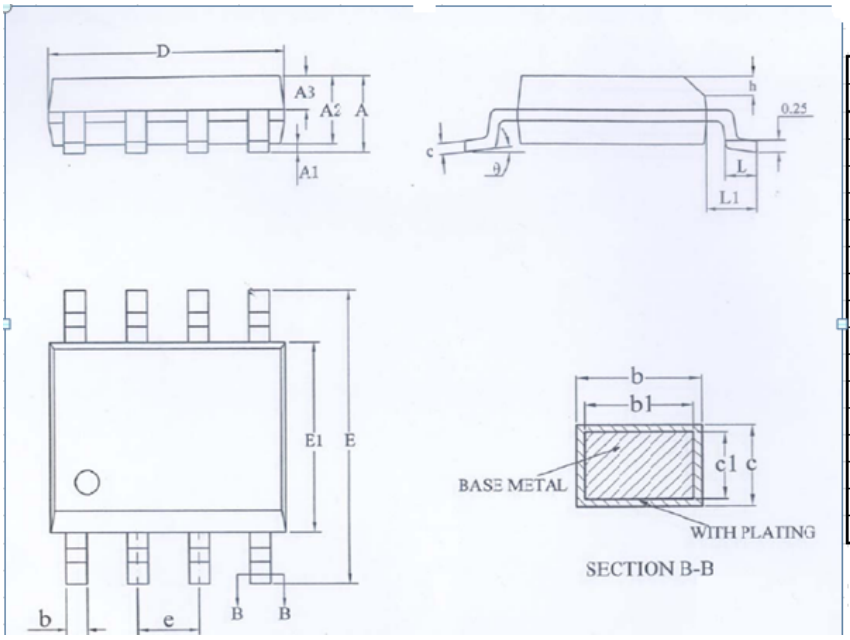
4 Package information

Figure 6 DIP8 package dimensions



SYMBOL	MILLIMETER		MILLIMETER
	MIN.	NOM	MAX.
A	3.60	3.80	4.00
A1	0.51	-	-
A2	3.20	3.30	3.40
A3	1.55	1.60	1.65
b	0.44	-	0.53
b1	0.43	0.46	0.48
B1	1.52BSC		1.52BSC
c	0.24	-	0.32
c1	0.23	0.25	0.27
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54BSC		2.54BSC
eA	7.62BSC		7.62BSC
eB	7.62	-	9.30
eC	0	-	0.84
L	3. 00	-	-

Figure 7 SOP8 package dimensions



SYMBOL	MILLIMETER		MILLIMETER
	MIN.	NOM	MAX.
A	-	-	1.75
A1	0.10	-	0.23
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
b1	0.38	0.41	0.44
c	0.21	-	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		1.27BSC
h	0.25	-	0.50
L	0.50	-	0.80
L1	1.05BSC		1.05BSC
θ	0°	-	8°

Notice： Sample tested during initial release and after any redesign or process change that may affect parameter. Specification subject to change without notice. Please ask for the newest product specification at any moment.