Description

BL7448SM is an IC Card chip (module) made by 0.35um CMOS EERPOM process. It has 1024 byte EEPROM with logical encryption and function.

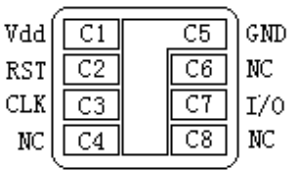

Figure 1

Features

- 1024 x 8 bit EEPROM organization
- Byte-wise addressing
  Irreversible byte-wise write protection of every Byte
- 1024 x1 bit organization of protection memory
- Serial three-wire link
- End of processing indicated at data output
- Minimum of 100,000 write/erase cycles
- Data retention time :>10 years
- Contacts configuration and serial interface according to ISO 7816 standard (synchronous transmission)
- Data can only be changed after entry of the correct 2-byte Programmable security code

Pin Description

Pin No.	Parameter	Symbol	Function Description
1	C1	V_{dd}	Supply Voltage
2	C2	RST	Reset signal
3	C3	CLK	Clock input
4	C4	N.C.	Not connected
5	C5	GND	Ground
6	C6	NC	Not connected
7	C7	I/O	Bidirectional data line (open drain)
8	C8	NC	Not connected

Function Description

- **Block Diagram**

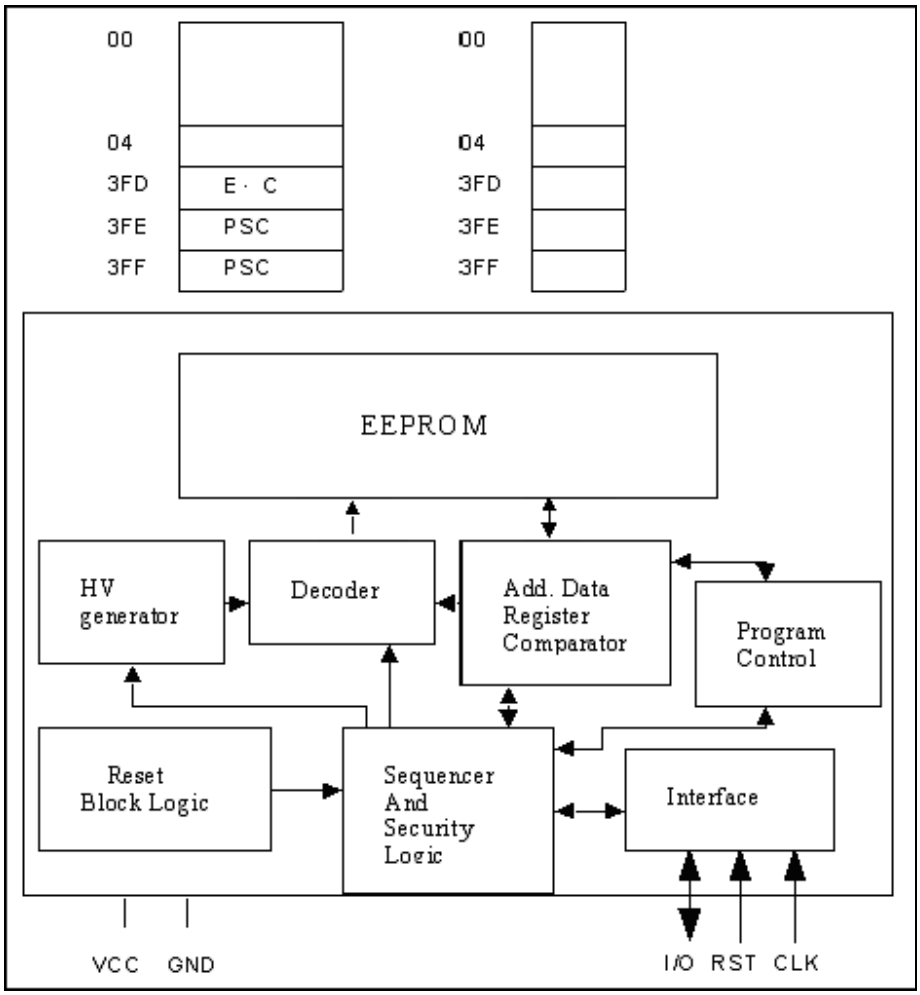

Figure 2

The BL7448SM consists of 1024 x 8 bit EEPROM main memory and a 1024-bit protection-memory With PROM functionality .The main memory can be irreversibly protected against data change by writing the corresponding bit in the protection memory. Once written the protection bit cannot be erased. The main memory is erased and written byte by byte. Normally a data change consists of an erase and write procedure. It depends on the contents of the data byte in the main memory and the new data byte whether the EEPROM is really erased and/or written. If none of the 8 bits in the addressed byte requires a zero-to-one transition the erase access will be suppressed. Vice versa the write access will be suppressed if no one-to-zero transition is necessary.

Additionally to the above functions the BL7448SM provides a security code logic, which controls the write/erase access to the memory. For this purpose, the BL7448SM contains a 3-byte security memory with an error counter EC and 2 bytes reference data. These 2 bytes as a whole are called programmable security code (PSC). After power on the whole memory, except for the reference data, the memory can only be read. (The value of PSC is “00”)Writing and erasing is only possible after a successful comparison of verification data with the internal reference data.

After eight successive unsuccessful comparisons the error counter blocks any subsequent attempt, and hence any possibility to write and erase.

- **Reset and Answer-to-Reset**

*Reset

After connecting the operating voltage to Vcc, the chip will hold and wait the operation of reset. The operation of reset begins with RST from L to H, and ends with CLK from L to H. During the operation of reset, all commands will be ignored.

After power on reset, the operation of reading must be execute before data can be altered.

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*Answer-to-Reset

Answer-to-Reset set the address counter to zero and output the first data. The other data can be read with CLK signal.

- **Command**

RST

RST	I/O
1	Command Input
0	Data Output

Command

Byte1								Byte2 Address	Byte3 Data	Operation	Mode
S0	S1	S2	S3	S4	S5	A8	A9	A0~A7	D0~D7		
1	0	0	0	1	1				Data	Updata main memory & protection memory	Processing
1	1	0	0	1	1				Data	Updata main memory	Processing
0	0	0	0	1	1				Comp. data	Write protection memory	Processing
0	0	1	1	0	0				No effect	Read main memory & protection memory	Data Output
0	1	1	1	0	0				No effect	Read main memory	Data Output

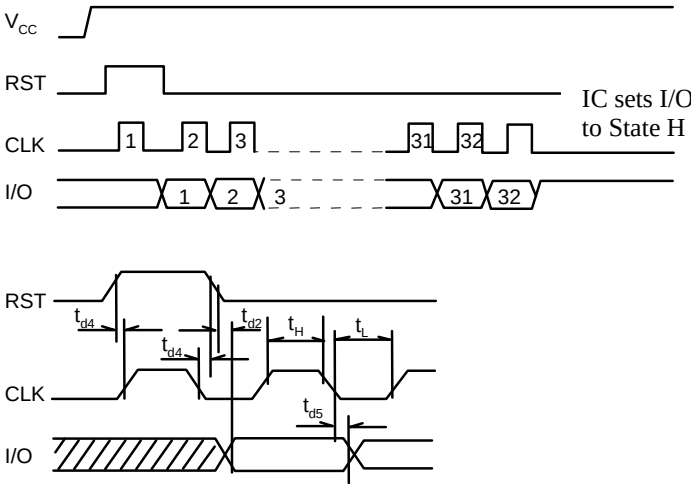

Figure 3 Reset and Answer-to-Reset

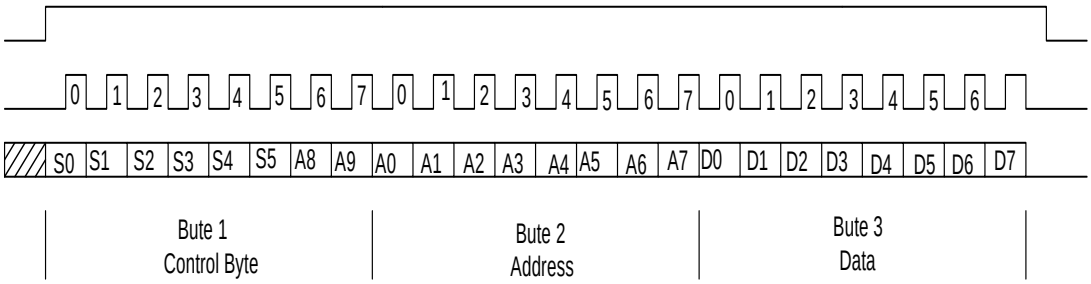

Figure 4 Command Input

Command Mode

Write/Erase Operation

Write/Erase, except for protection-memory

Note: Write means from H to L, Erase means from L to H

There are three kinds of Write/Erase operations:

Erase and Write (The number of clock pulses=203, frequency <=20KHZ)

Write only: means the 8 bits in the addressed byte from H to L(The number of clock pulses =103, frequency <=20KHZ)

Erase only(=FF; The number of clock pulses =103, frequency <= 20KHZ)

Write/Erase, include protection-memory

As shipped, the protection-memory has been erased, it can be written only once.

Write protection-memory and compare data

When comparison of the entered data byte is same as the assigned byte in the EEPROM. the protection-memory is written.

After sent a certain CLK, the command of Write/Erase will be over. After operation, the state of I/O pin will be changed from H to L.

The I/O state can be changed when RST change from L to H.

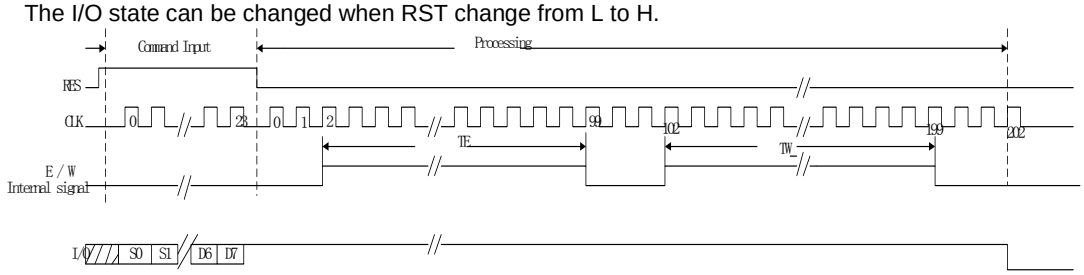

Figure 5 Erase and Write timing

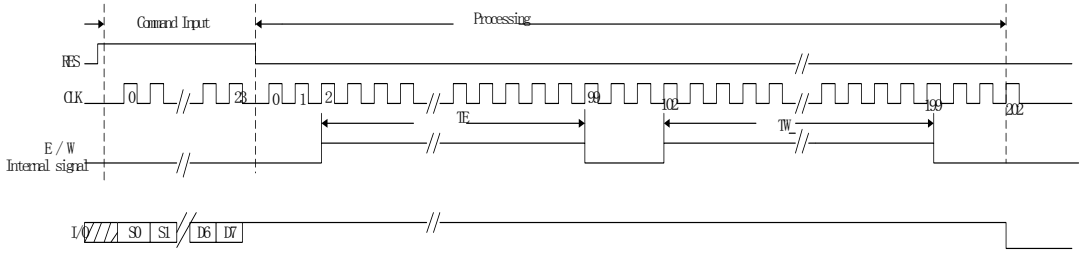

Figure 6 Only Write or Erase

Read operation

Read main memory (See Figure 7)

This operation don't read the protection-memory. After 8 CLK, the address of memory will be increased by additional pulse .

Read main memory and protection-memory (See Figure 8)
After input this command, the next 8 CLK will read out 8 bits data; the ninth CLK will read out the content of protection-memory. After 9 CLK, the address of memory will be increased by additional pulse.

Security code verification

Byte1								Byte2 Address	Byte3 Address	Operation	Mode
0	1	0	0	1	1	1	1	253	Bit mask	Write error counter	Processing
1	0	1	1	0	0	1	1	254	PSC byte1	Verification 1st PSC byte	Processing
1	0	1	1	0	0	1	1	255	PSC byte2	Verification 2nd PSC byte	Processing

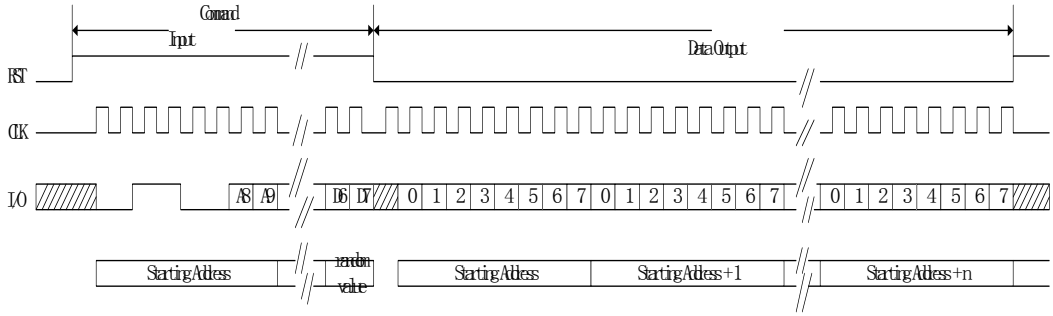

Figure 7 Read main memory

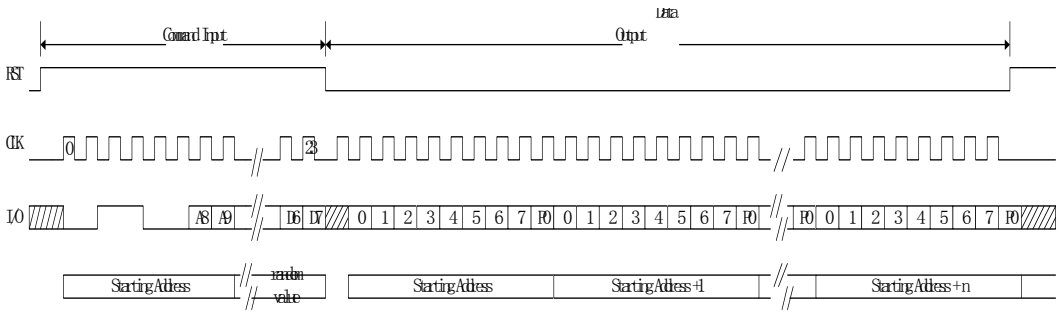

Figure 8 read main memory and protection-memory

- **Security code verification**

User verification operation

BL7448SM only can read when the security code verification is unsuccessful. The content of security code cannot be read out. If you try to read security code, you only can get “00”

The processing is:
*Write a bit of EC(the bit is not written before), the address of EC is “1021”
*Input the first byte of PSC, the address is “1022”
*Input the second byte of PSC, the address is “1023”
*If the security verification is successful , the EC can be erased.

After security code identification , I/O will be changed from H to L. I/O will return to H when RST change from L to H. EC cannot be erased automatically.

Write Error Counter (EC)

Before security code identification, only Error Counter (EC) can be written. A number of erased bit of EC means what times EC can be written. After security code verification is successful, EC should be erased before power off. After security code verification is unsuccessful, if it is verified again, EC must be written.

Input PSC

PSC input start from lowest bit of low byte to high byte. If comparison of data is right, EEPROM can be written or erased before power-off and the corresponding protection bit of PSC is H, PSC can be changed.

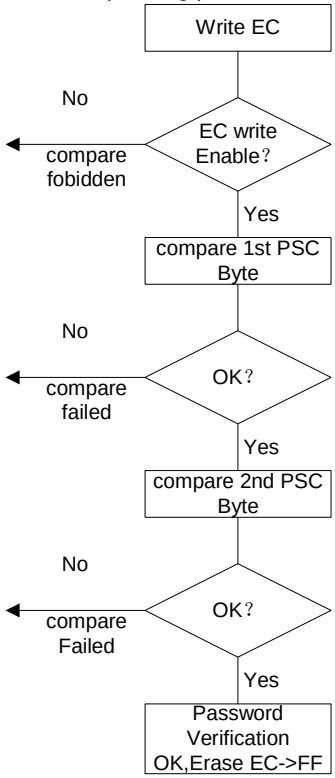

Figure 9 Verification Procedure

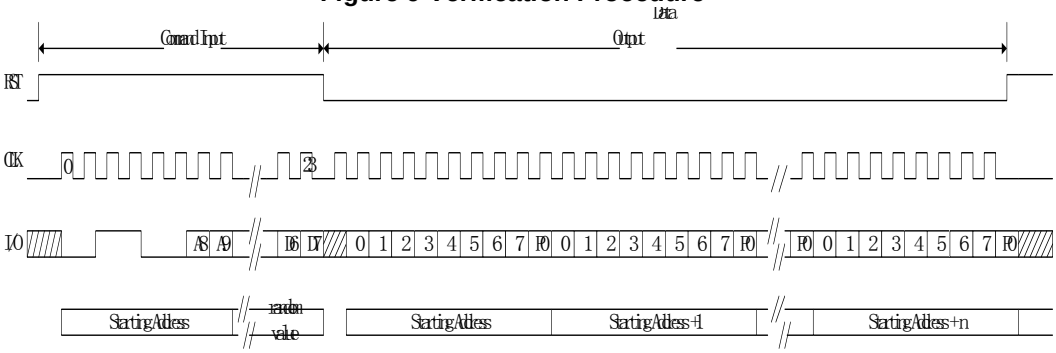

Figure 10. PSC Verification timing

Electrical Parameter

- **Absolute Maximum Ratings**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	Max	
Supply voltage	V_{CC}	-0.3		6.0	V
Input voltage (any pin)	V_I	-0.3		6.0	V
Storage temperature	T_S	-40		125	℃
Power comsumption	PT	0		60	mw
Operation temperature	Ta	-35		70	℃

- **DC Characteristics**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	Max	
Supply voltage	V_{CC}	3.0	5.0	5.5	V
Supply current	I_{CC}		3	10	mA
High-level input voltage (I/O,CLK,RST)	V_{IH}	$0.7V_{CC}$	-	V_{CC} +0.3	V
Low-level input voltage (I/O,CLK,RST)	V_{IL}	V_{GND}-0.2	-	$0.15V_{GND}$	V
High-level input current (I/O,CLK,RST)	I_H	-	-	50	uA
Low-level output current V_{OL} =0.4V,open drain	I_{OL}	0.5	-	-	mA
High-level leakage current $V_{OH} = V_{CC}$,open drain	I_{OH}	-	-	50	A
Input capacitance	C_I	-	-	10	pF

- **AC Characteristics**

Parameter	Symbol	Limit Values			Unit
		min.	typ.	Max	
Clock frequency	CLK		20		kHz
Clock high period	t_H	10			μs
Clock low period	t_L	10			μs
Setup time data	t_{d1}	4			μs
Delay time	t_{d2}	6			μs
Clock setup time for RST	t_{d3}	4			μs
RST setup time for clock	t_{d4}	4			μs
Hold time data	t_{d5}	4			μs
Eraser time	T_{ER}	5			ms
Write time	t_{WR}	5			ms