上海贝岭 SHANGHAI BELLING

# BL8087

***PMU with a Synchronous 1A Buck and a CMOS 500mA LDO***

## DESCRIPTION

The BL8087 is a power management unit (PMU), with 1 synchronous Buck and 1 CMOS low-dropout regulators that delivers a maximum current of 1A for Buck's output and a maximum current of 0.5A for LDO's output.

The synchronous buck is a high-efficiency, DC-to-DC step-down switching regulator, capable of delivering up to 1A of output current. The device operates from an input voltage range of 2.6V to 6V and provides an output voltage from 0.6V to VDD, making the buck ideal for low voltage power conversions. Running at a fixed frequency of 1.5MHz allows the use of small external components, such as ceramic input and output caps, as well as small inductors, while still providing low output ripples. This low noise output along with its excellent efficiency achieved by the internal synchronous rectifier, making the buck an ideal green replacement for large power consuming linear regulator. Internal soft-start control circuitry reduces inrush current. Short-circuit and thermal-overload protection improves design reliability.

The LDO is a low-dropout regulator that delivers a maximum current of 0.5A output. Typical dropout voltage at 0.5A load current is 0.8V. It has excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The output accuracy is set within 2% by trimming.

Typical LDO output voltage: VOUT=1.8V. Other fixed voltage can be provided in the range of 1.2V~4.5V every 0.1V step. It also can be customized on command. LDO can also work under a wide input voltage ranging from 2V to 6V. They can provide foldback short-circuit protection and output current limit function.

BL8087 is available in lead (Pb)-free DFN2X2-8 (with exposed pad for heat dissipation) package.

## FEATURES

BUCK

- High Efficiency : Up to 97%
- Capable of Delivering 1A
- 1.5MHz Switching Frequency
- No External Schottky Diode Needed
- Low dropout 100% Duty operation
- Internal Compensation and Soft-Start
- Current Mode control
- 0.6V Reference for Low Output voltages
- Logic Control Shutdown (IQ<1uA)
- Thermal shutdown, UVLO and OVP

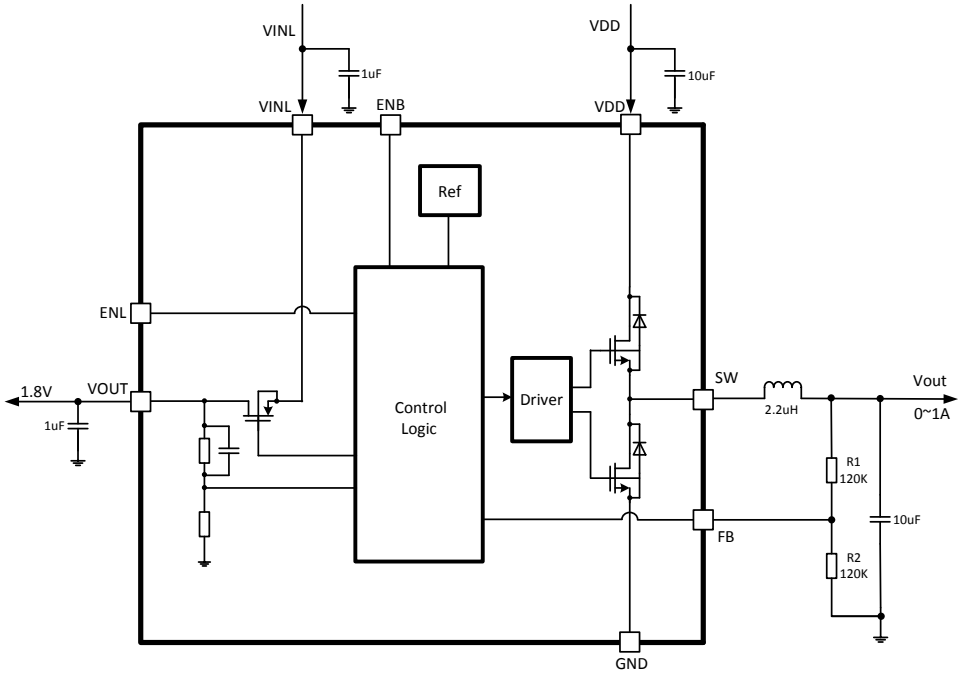
LDO

- Max output current is 0.5A
- Input voltage range: 2 – 6V
- Output voltage range: 1.2V~4.5V (customized on command every 0.1V step)
- Low power consumption: 40uA (Typ.)
- Low output noise (47uVRMS)
- Shutdown mode: 0.1uA
- Low dropout voltage: 800mV@IOUT=500mA, VOUT=1.8V
- High PSRR: 65dB@1KHz (Typ.)
- Low temperature coefficient: ±100ppm/°C
- Excellent line regulation: 0.05%/V
- Highly accurate: ±2%
- Output current limit
- Fold-back short circuit current

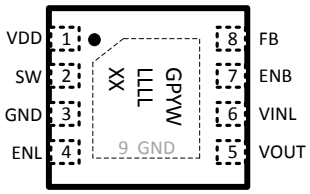
## APPLICATIONS

- Distributed Power Systems
- Digital Set Top Boxes
- Flat Panel Television and Monitors
- Wireless and DSL Modems
- Power source for cellular phones and various kind of PCSs
- Battery Powered equipment

## TYPICAL APPLICATION




## ORDERING INFORMATION

| Mark Explanation | | Ordering Information | |
|---|---|---|---|
| GP: Product Code<br>YW: Date code<br>LLLL: Lot No.<br>XX: Output Voltage |  DFN2x2-8 | DFN2x2-8<br>3000pcs/reel | BL8087CKBTR□□ |

## ABSOLUTE MAXIMUM RATING

| Parameter | | Value |
|---|---|---|
| Max Input Voltage (VDD) | | 8V |
| Max Input Voltage (VINL) | | 8V |
| Max Operating Junction Temperature(Tj) | | 125°C |
| Ambient Temperature(Ta) | | -40°C – 85°C |
| Maximum Power Dissipation | DFN2X2-8 | 1.6W |
| Package Thermal Resistance (θjc) | | 18°C / W |
| Package Thermal Resistance (θjA) | | 80°C / W |
| Storage Temperature(Ts) | | -40°C - 150°C |
| Lead Temperature & Time | | 260°C, 10S |

***Note:*** *Exceed these limits to damage to the device. Exposure to absolute maximum rating conditions may affect device reliability.*

## RECOMMENDED WORK CONDITIONS

| Parameter | Value |
|---|---|
| Input Voltage Range (VDD) | Max. 6V |
| Input Voltage Range (VIN) | Max. 6V |
| Operating Junction Temperature(Tj) | Max. 125°C |

## PIN DESCRIPTION

| PIN # | NAME | DESCRIPTION | PIN # | NAME | DESCRIPTION |
|---|---|---|---|---|---|
| 1 | VDD | Supply Voltage Input Pin | 6 | VINL | LDO Input Pin |
| 2 | SW | Switch Pin | 7 | ENB | Buck Enable Pin |
| 3 | GND | Ground Pin | 8 | FB | Feedback Pin |
| 4 | ENL | LDO Enable Pin | 9 | GND | Ground Pin (Thermal PAD) |
| 5 | VOUT | Output Pin | | | |

## ELECTRICAL CHARACTERISTICS

(VDD=5V, TA=25°C)
BL8087CKBTR18

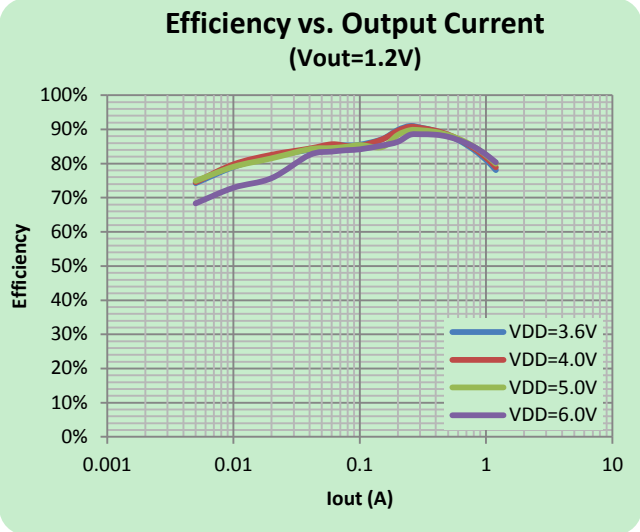
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BUCK** | | | | | | |
| VDD | Input Voltage Range | | 2.6 | | 6 | V |
| Vref | Feedback Voltage | VDD=5V | 0.588 | 0.6 | 0.612 | V |
| Ifb | Feedback Leakage current | | | 0.1 | 1 | uA |
| Iq | Quiescent Current | Active, Vfb=0.65, No Switching | | 50 | | uA |
| | | Shutdown | | | 1 | uA |
| LnReg | Line Regulation | VDD=2.7V to 5.5V | | 0.1 | 0.2 | %/V |
| LdReg | Load Regulation | Iout=0.01 to 1A | | 0.1 | 0.2 | %/A |
| Fsoc | Switching Frequency | | | 1.5 | | MHz |
| OVP | Input over voltage lockout | | | 6.5 | | V |
| RdsonP | PMOS Rdson | | | 250 | 350 | mohm |
| RdsonN | NMOS Rdson | | | 150 | 250 | mohm |
| Ilimit | Peak Current Limit | | 1.1 | 1.5 | 2 | A |
| Inoload* | | VDD=5V, Vout=3.3V, Iout=0 | | 75 | | uA |
| Iswlk | SW Leakage Current | Vout=6V, $V_{SW}$=0 or 6V, ENB=0V | | | 1 | uA |
| Ienlk | ENB Leakage Current | | | | 1 | uA |
| Vh_ENB | ENB Input High Voltage | | 1 | | | V |
| Vl_ENB | ENB Input Low Voltage | | | | 0.5 | V |
| **LDO** | | | | | | |
| VINL | Input Voltage Range | | VOUT | | 6 | V |
| IOUT (Max.) | Maximun Output Current | VINL-VOUT=1V | 500 | | | mA |
| VOUT | Output Voltage | 1mA≤IOUT≤30mA , VINL=3.3V | 1.774 | 1.8 | 1.836 | V |
| LNR | Line Regulation | IOUT=40mA, 3V≤VINL≤6V | | 0.05 | 0.2 | %/V |
| ΔVOUT | Load Regulation | VINL=VOUT+1V, 1mA≤IOUT≤0.5A | | 30 | 100 | mV |
| Vdrop | Dropout Voltage | IOUT=0.5A (VOUT=1.8V) | | 0.75 | 0.95 | V |
| Ilimit | Current Limit | | | 0.8 | | A |
| Iss | Supply Current | VINL=VOUT+1V | | 40 | 80 | uA |
| Vh_ENL | ENL Input Voltage “H” | | 1.5 | | VINL | V |
| Vl_ENL | ENL Input Voltage “L” | | 0 | | 0.25 | V |
| PSRR | Ripple Rejection | F=1KHz, Ripple=0.5Vp-p<br>VINL=VOUT+1V | | 65 | | dB |
| ΔV/ΔT | Temperature coefficient | | | ±100 | | ppm |

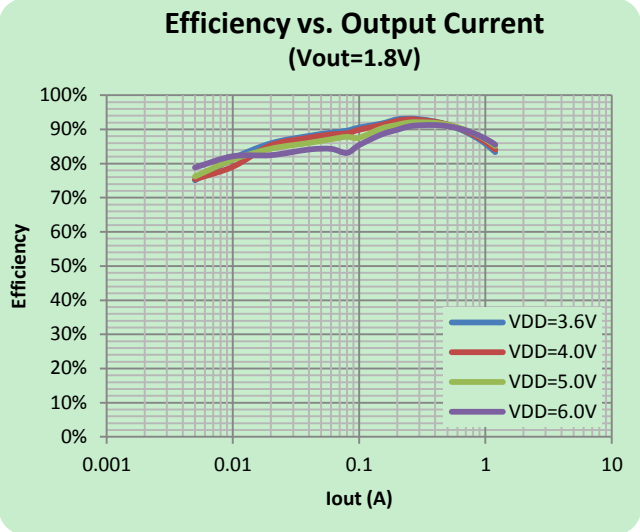
***Note:*** **When Buck Dutycycle >80%, Inoload will increase. e.g. VDD=3.6V/Vout=3.3V, Inoload=1mA.*

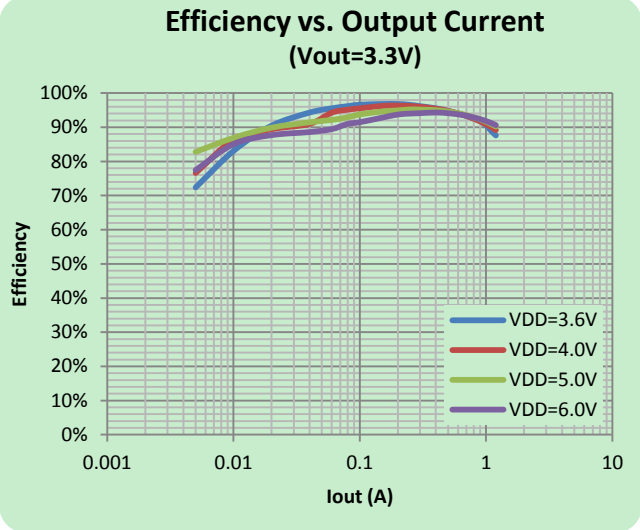
## ELECTRICAL PERFORMANCE

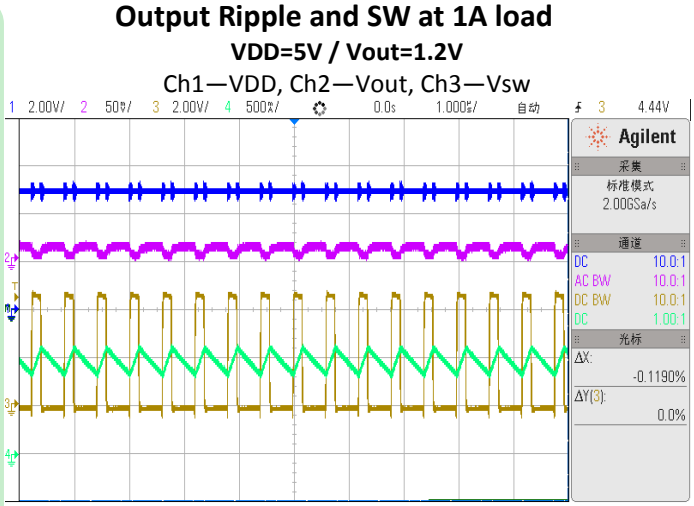
*Tested under TA=25°C, unless otherwise specified*

***BUCK***

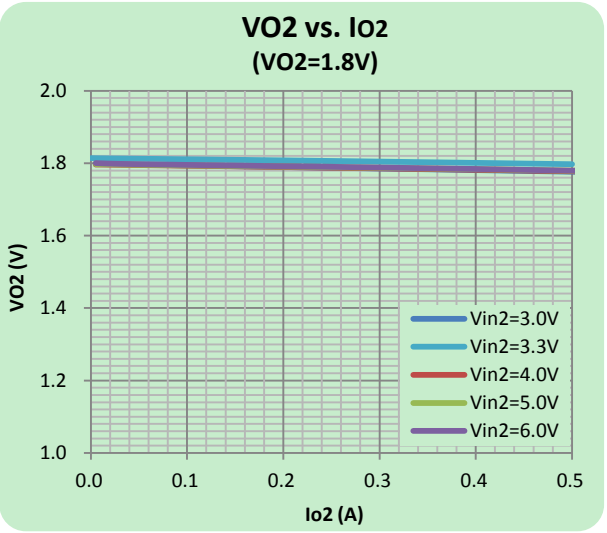


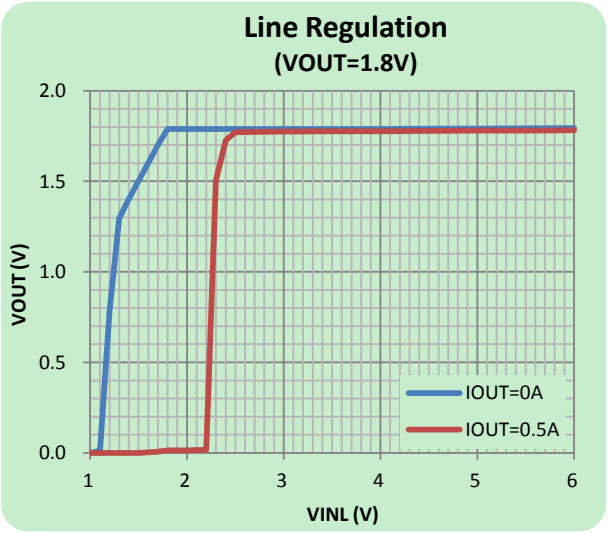




***LDO***



## DETAILED DESCRIPTION

### *BUCK*

#### *Current Limit*

There is a cycle-by-cycle current limit on the high-side MOSFET of 1.5A(typ). When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. The buck utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to 1.5A (typ) and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

#### *Soft-start*

The buck has an internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

#### *UVLO and Thermal Shutdown*

If VDD drops below 2.5V, the UVLO circuit inhibits switching. Once VDD rises above 2.6V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds TJ= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

#### *Setting Output Voltages*

Output voltages are set by external resistors. The FB_ threshold is 0.6V.
R1 = R2[(Vout/0.6) - 1]

#### *Input Capacitor Selection*

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

VRIPPLE = IL(PEAK)[1 / (2π x fOSC x COUT)]

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:
VRIPPLE(ESR) = IL(PEAK) x ESR

### *LDO*

The device has built-in modules including high accuracy voltage reference, error amplifier, current limit, power transistors and driver circuit. Current limit functions ensure reliability of device and power system.

The bandgap module provides stable reference voltage whose temperature coefficient is compensated by careful design considerations. The temperature coefficient is under 100 ppm/°C. It has excellent load and line transient response and good temperature characteristics, which can assure the stability of chip and power system. The accuracy of output voltage is guaranteed by trimming technique.

## THERMAL CONSIDERATIONS

Thermal consideration has to be taken account into to ensure proper function of the device. Power dissipation of BL8087 can be calculated as

LDO Power Dissipation (PL) = (VINL-VOUT)×IOUT

BUCK Power Dissipation (PB) = VDD×IDD×10%

Total Power Dissipation (PT) = PL + PB

For proper function and safe operation of the device, total power dissipation is recommended to be limited within 1.6W.

## APPLICATION INFORMATION

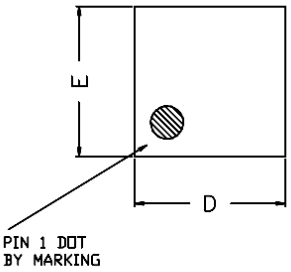
Layout is critical to achieve clean and stable operation. The switching power stage and heat dissipation requires particular attention. Follow these guidelines for good PC board layout:

1) Place decoupling capacitors as close to the IC as possible
2) Connect input and output capacitors to the same power ground node with a star ground configuration then to IC ground.
3) Keep the high-current paths as short and wide as possible. Keep the path of switching current (CIN to VDD and CIN to GND) short. Avoid vias in the switching paths.
4) If possible, connect VINL, VOUT, VDD, SW, and GND separately to a large copper area to help cool the IC to further improve efficiency and long-term reliability.
5) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the IC as possible.
6) Route high-speed switching nodes away from sensitive analog areas.

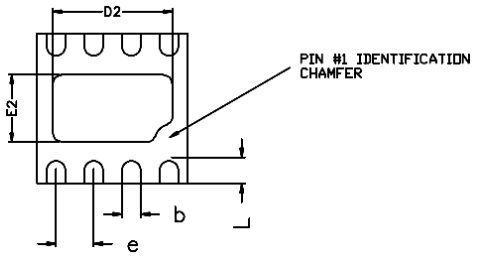
## PACKAGE OUTLINE

| Package | DFN2x2-8 | Devices per reel | 3000 | Unit | mm |
|---|---|---|---|---|---|

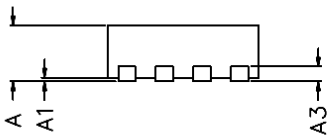
Package specification：




TOP VIEW




BOTTOM VIEW




SIDE VIEW

| COMMON DIMENSIONS(MM) | | | |
|---|---|---|---|
| PKG. | W1VERY VERY THIN | | |
| REF. | MIN. | NOM. | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.2 REF. | | |
| D | 1.95 | 2.00 | 2.05 |
| E | 1.95 | 2.00 | 2.05 |
| b | 0.20 | 0.25 | 0.30 |
| L | 0.20 | 0.30 | 0.40 |
| D2 | 1.45 | 1.60 | 1.70 |
| E2 | 0.75 | 0.90 | 1.00 |
| e | 0.50 BSC | | |