Ultra-small package High-precision Voltage Detector with delay circuit, BL8509B Series

General Description

BL8509B Series is a series of high-precision voltage detectors with a built-in delay time generator of fixed time developed using CMOS process. Internal oscillator and counter timer can delay the release signal without external parts. Detect voltage is extremely accurate with minimal temperature drift. CMOS output configurations are available.

Selection Guide

BL8509B- ***XXX X X XX***

Package type：
RM：SOT-23-3
RN：SOT-23-5
RO：SOT-23

Output type：
N：Nch
C：CMOS

Delay time：
A：50mS
B：100mS
C：150mS
D：200mS
E：250mS
F：300mS
G：400mS

Detector voltage：
090……0.9V
100……1.0V
263……2.63V
300……3.0V
465……4.65V
……
600……6.0V

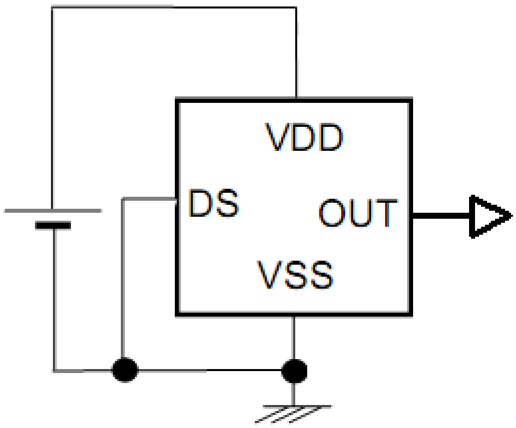
Features

- Highly accuracy：　±2%
- Low power consumption：TYP 0.9uA　(V_{DD}=3V)
- Detect voltage range：1.0V~6.5V in 0.1V increments
- Operating voltage range：0.7V~7V
- Detect voltage temperature characteristics：TYP±100ppm/℃
- Output configuration：　CMOS
- Package：　SOT-23，SOT-23-3，SOT-23-5

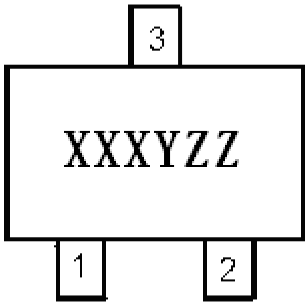
Typical Application

- Power monitor for portable equipment such as notebook computers, digital still cameras, PDA, and cellular phones
- Constant voltage power monitor for cameras, video equipment and communication devices.
- Power monitor for microcomputers and reset for CPUs.
- System battery life and charge voltage monitors

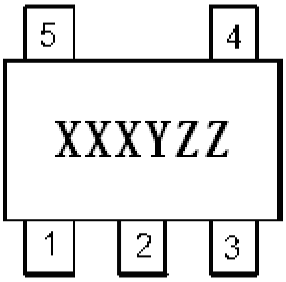
Typical Application Circuit



Pin Configuration



SOT-23
SOT-23-3



SOT-23-5

Marking definition：

Symbol	Define
XXX	Voltage
Y	Delay Time
ZZ	Data Code

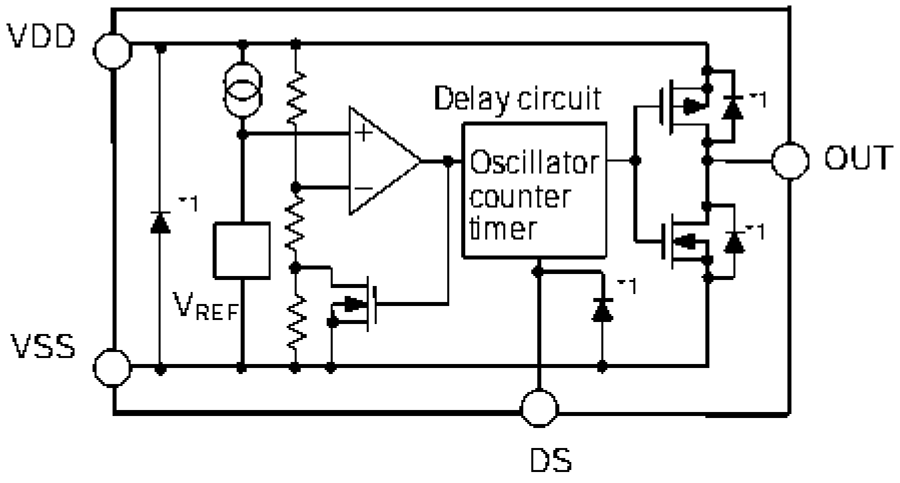
Ex. 293DKL：
293：Detection voltage 2.93v
D：Delay time 200ms
KL：Date in produced

Pin Assignment

PIN Number	Pin Name	Function
SOT-23/SOT23-3		
1	VSS	Ground
2	VOUT	Output Voltage
3	VDD	Input Voltage

PIN Number	Pin Name	Function
SOT23-5		
1	DS	ON/OFF switch for delay time
2	VSS	Ground
3	NC	No Connection
4	VOUT	Output Voltage
5	VDD	Input Voltage

Block Diagram



*1. Parasitic diode

Absolute Maximum Ratings

PARAMETER		SYMBAL	RATINGS	UNITS
V_{DD} Input Voltage		V_{DD}	8	V
Output Current		I_{OUT}	50	mA
Output Voltage	CMOS	V_{OUT}	Vss-0.3~ V_{DD} +0.3	V
Continuous Total Power Dissipation	SOT-23-3	Pd	300	mW
	SOT-23-5			
Operating Ambient Temperature		T_{Opr}	-40~+85	℃
Storage Temperature		T_{stg}	-40~+125	℃
Soldering temperature and time		T_{solder}	260℃, 10s	

Electrical Characteristics：

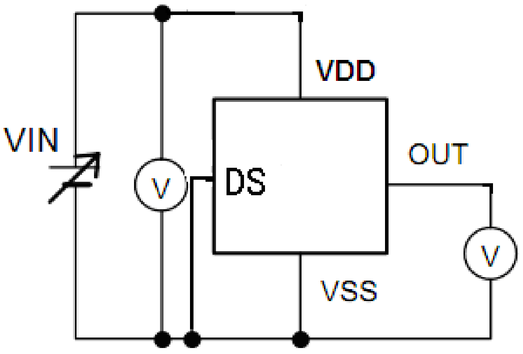
(-V_{DET}(S)=1.0V to 6.5V±2% ,Ta=25^{O}C , unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Units	Test circuit
Detect Voltage	-VDET	-	-VDET（S） ×0.98	-VDET(S)	-VDET(S) ×1.02	V	1
Hysteresis Range	VHYS	-	0.03	0.06	0.1	V	
Supply Current	ISS	VDD=3V (below 2.5V)	-	0.9	1.5	uA	2
		VDD=5V (2.5V-4.5V)	-	1.4	2.8		
		VDD=7V (4.5V-6.5V)	-	1.8	3.6		
Output Current	Iout N-ch	VDS=0.5V VDD=0.7V	0.01	0.19	--	mA	3
	Iout P-ch	VDS=0.5V VDD=7V	1.7	3.4	--	mA	4
Operating voltage	VDD	-	0.7	-	7	V	1
Delay time	Td1	VDD=-VDET+1V DS low	130	200	290	ms	1
	Td2	VDD=-VDET+1V DS high	110	220	330	us	5
Temperature characteristics	$\frac{\Delta -VDET}{\Delta Ta \bullet -VDET}$	ΔTa =-40℃ ~ 85℃	-	±100	±350	ppm/℃	1

Note： 1、-VDET(S) ：Specified Detection Voltage value
2、-VDET ：Actual Detection Voltage value
3、Release Voltage：+VDET=-VDET+VHYS

Test Circuits:

1.



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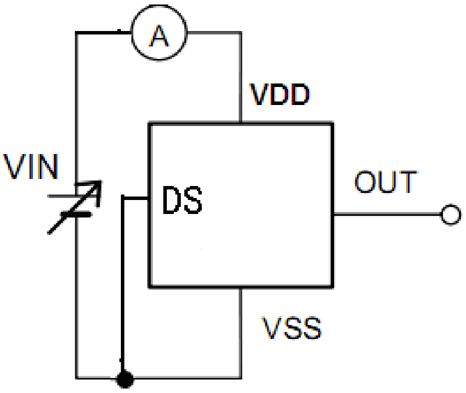

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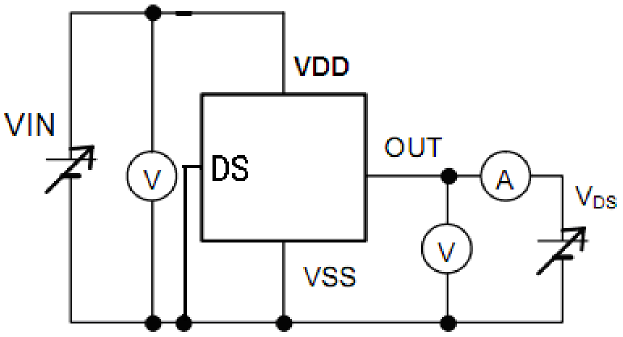

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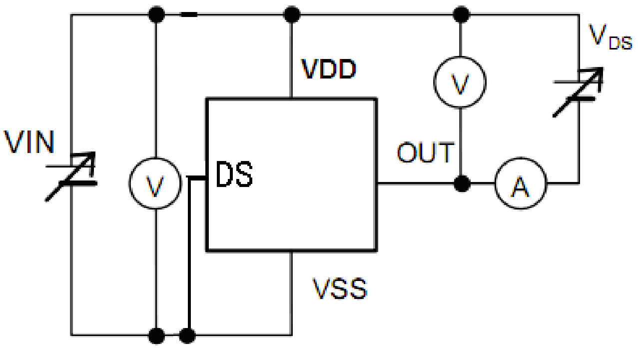

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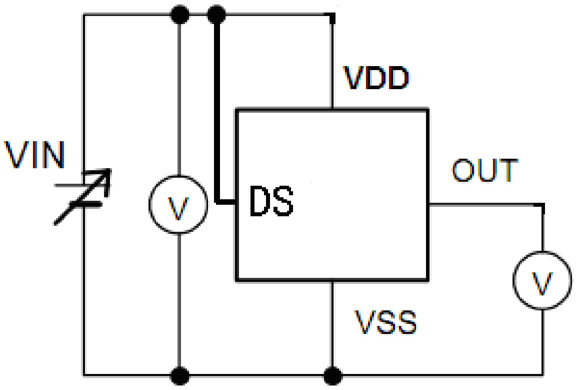


Functional Description：

1. Basic Operation: CMOS Output (Active Low)

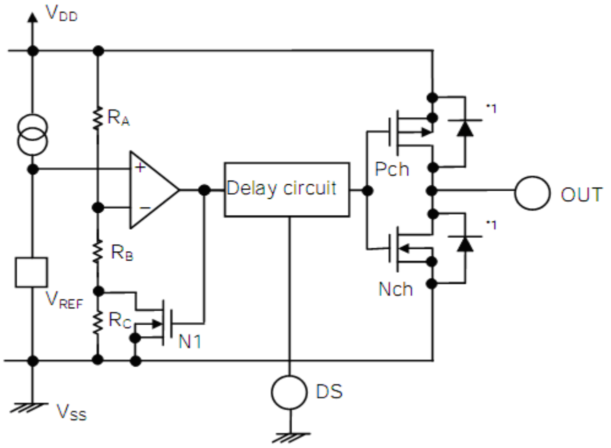
1-1. When the power supply voltage (VDD) is higher than the release voltage (+VDET), the Nch transistor is OFF and the Pch transistor is ON to provide VDD (high) at the output. Since the Nch transistor N1 in Figure 1 is OFF, the comparator input voltage is $\frac{(R_B + R_C) \bullet VDD}{R_A + R_B + R_C}$.

1-2. When the VDD goes below +VDET, the output provides the VDD level, as long as VDD remains above the detection voltage (–VDET). When the VDD falls below –VDET (point A in Figure 2), the Nch transistor becomes ON, the Pch transistor becomes OFF, and the VSS level appears at the output. At this time the Nch transistor N1 in Figure 1 becomes ON, the comparator input voltage is changed to $\frac{R_B \bullet VDD}{R_A + R_B}$.

1-3. When the VDD falls below the minimum operating voltage, the output becomes undefined, or goes to VDD when the output is pulled up to VDD.

1-4. The VSS level appears when VDD rises above the minimum operating voltage. The VSS level still appears even when VDD surpasses the –VDET, as long as it does not exceed the release voltage +VDET.

1-5. When VDD rises above +VDET (point B in Figure 2), the Nch transistor becomes OFF and the Pch transistor becomes ON to provide VDD at the output. The VDD at the OUT pin is delayed for Td due to the delay circuit.



*1. Paracitic diode

Figure 1 Operation 1

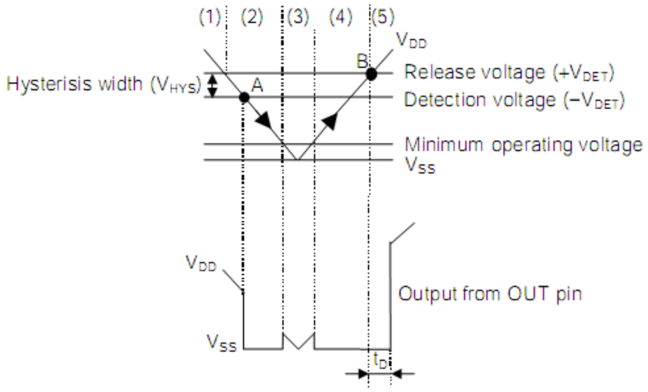


Figure 2 Operation 2

2. Delay Circuit

2-1. Delay Time

The delay circuit delays the output signal from the time at which the power voltage (VDD) exceeds the release voltage (+VDET) when VDD is turned on. The output signal is not delayed when the VDD goes below the detection voltage (–VDET). (Refer to Figure 2.) The delay time (t_D) is a fixed value that is determined by a built-in oscillation circuit and counter.

2-2. DS Pin (ON/OFF Switch Pin for Delay Time)

The DS pin should be connected to Low or High. When the DS pin is High, the output delay time becomes short since the output signal is taken from the middle of counter circuit (Refer to Figure 3).

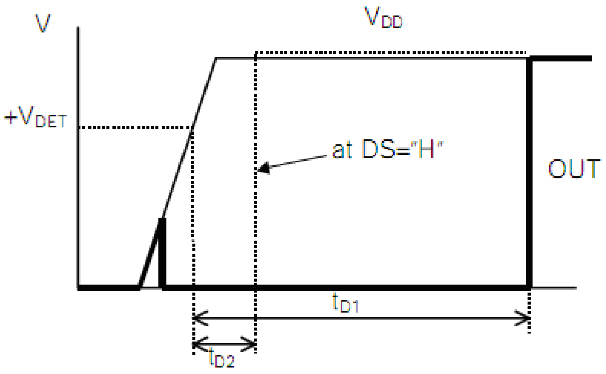


Figure 3

Directions for use：

1、 Please use this IC within the stated maximum ratings. Operation beyond these limits may cause degrading or permanent damage to the device.

2、When a resistor is connected between the V_{DD} pin and the input with CMOS output configurations, oscillation may occur as a result of voltage drops at R_{IN} if load current(I_{OUT}) exists.(refer to the Oscillation Description(1) below)

3、When a resistor is connected between the V_{DD} pin and the input with CMOS output configurations, oscillation may occur as a result of through current at the time of voltage release even if load current(I_{OUT}) does not exist. (refer to the Oscillation Description(2) below)

4、With a resistor connected between the V_{DD} and the input, detect and release voltage will rise as a result of the IC's supply current flowing through the V_{DD} pin.

5、In order to stabilize the IC's operations, please ensure that V_{DD} pin's input frequency's rise and fall times are more than several u Sec/V.

Oscillation Description：

1、 Output current oscillation with the CMOS output configuration

When the voltage applied at IN rises, release operations commence and the detector's output voltage increase. Load current(I_{OUT}) will flow at R_L. Because a voltage drop(R_{IN}*I_{OUT}) is produces at the R_{IN} resistor, located between the input(IN) and the V_{DD} pin. The load current will flow via the IC's pin. The voltage drop will also lead to a fall in the voltage level at the V_{DD} pin. When the V_{DD} pin voltage level falls below the detect voltage level, detect operations will commence. Fllowing detect operations, load current flow will cease and since voltage drop at R_{IN} will disapper, the voltage level at the V_{DD} pin will rise and release operations will begin over again. Oscillation may occur with this "release-detect-release" repetition. Further, this condition will also appear via means of a similar mechanism during detect operations.

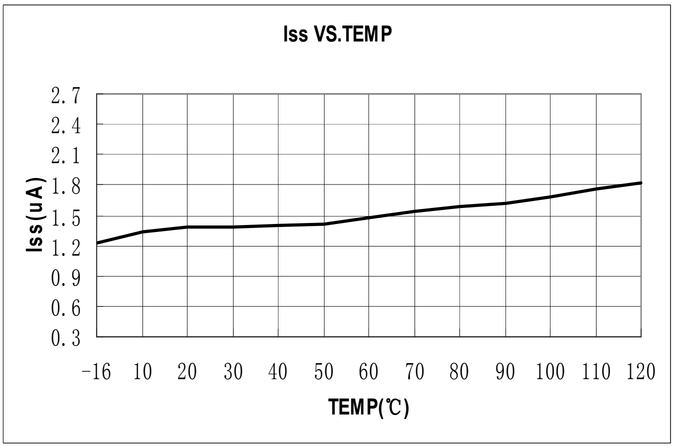
2、 Oscillation as a result of through current

Since the BL8509B series are CMOS IC's, through current will flow when the IC's internal circuit switching operates(during release and detect operations). Consequently, oscillation is liable to occur as a result of drops in voltage at the through current's resistor(R_{IN}) during release voltage operations.(refer to diagram 2) since hysteresis exists during detect operations, oscillation is unlikely to occur.

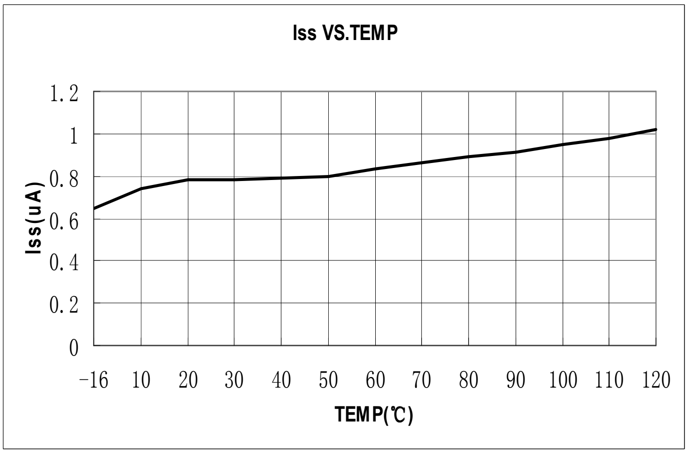
Type Characteristics

1、SUPPLY CURRENT VS. AMBIENT TEMPERATURE

VDD=5V,-VDET=2.63V

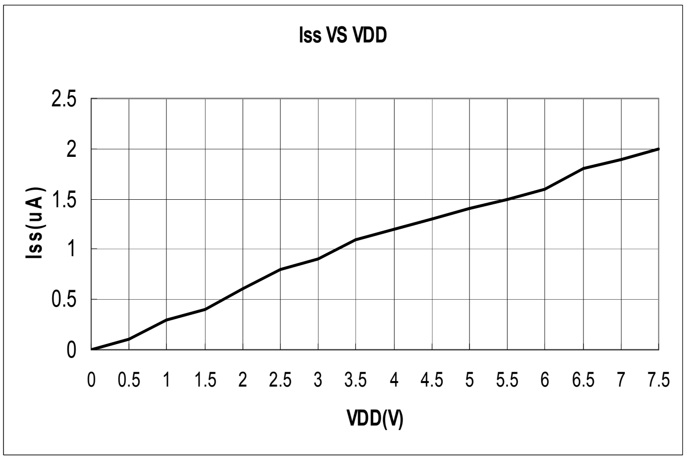


VDD=2.5V,-VDET=2.63V



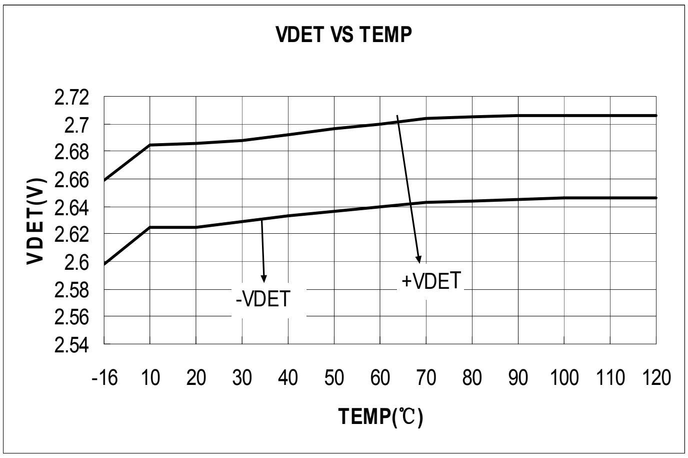
2、 SUPPLY CURRENT VS. INPUT VOLTAGE

-VDET=2.63V （T=25℃）



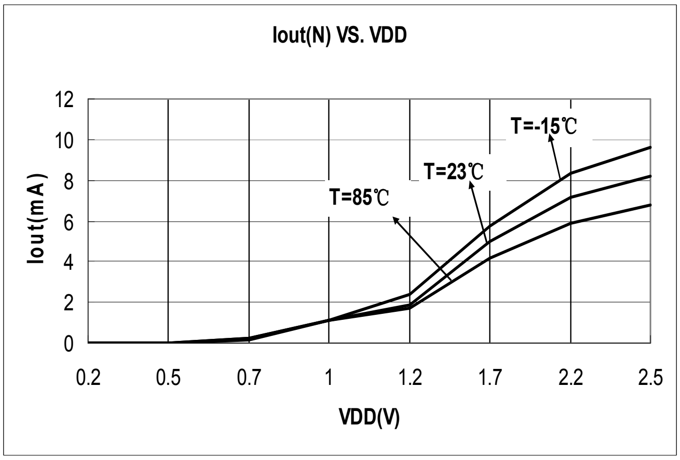
3、 DETECT,RELEASE VOLTAGE VS. AMBIENT TEMPERATURE

-VDET=2.63V

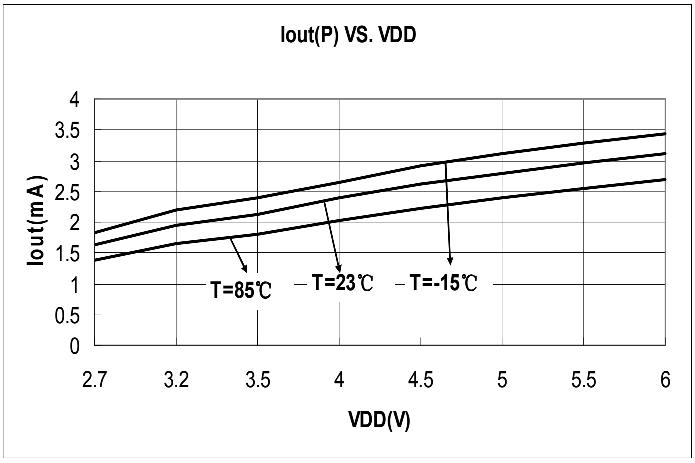


4、 OUTPUT CURRENT VS. INPUT VOLTAGE

N-ch VDS=0.5V,-VDET=2.63V

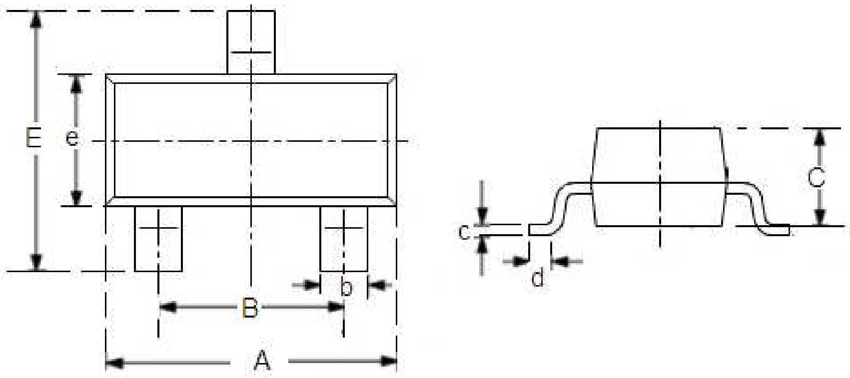


P-ch VDS=0.5V,-VDET=2.63V



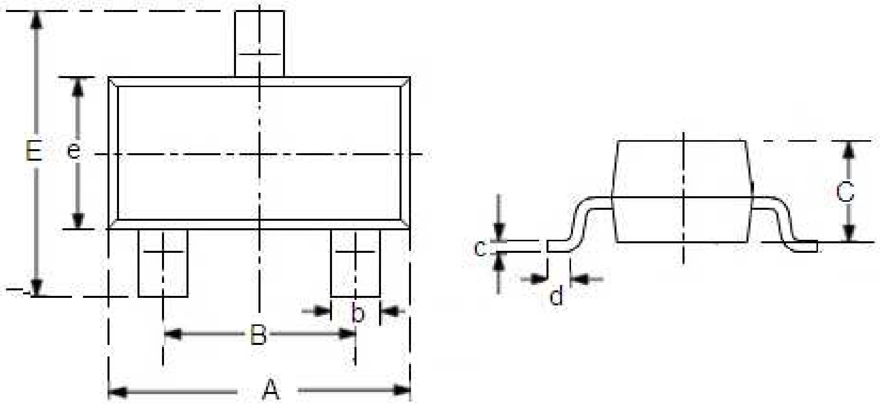
Package Information

SOT-23



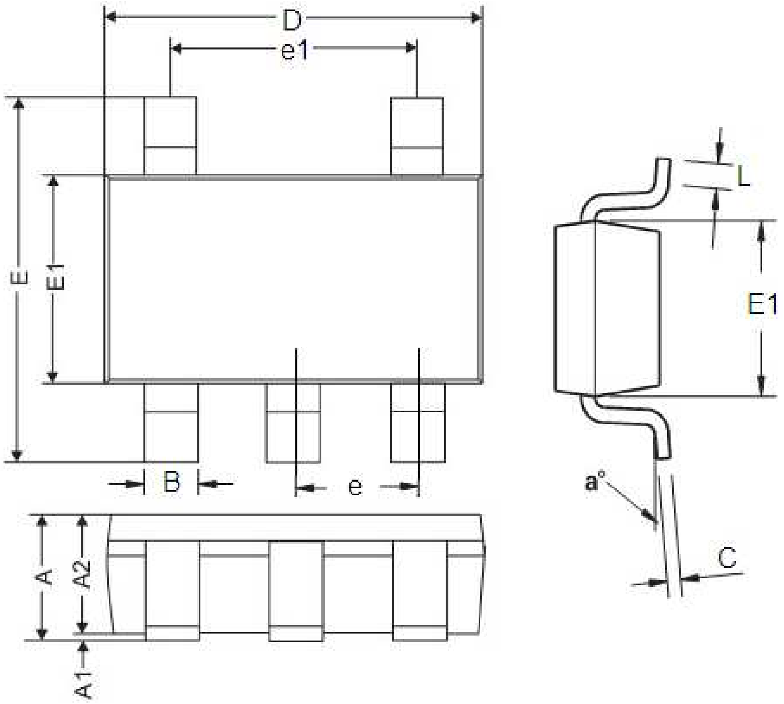
DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	2.7	3.1	0.1063	0.122
B	1.7	2.1	0.0669	0.0827
b	0.35	0.5	0.0138	0.0197
C	1	1.2	0.0394	0.0472
c	0.1	0.25	0.0039	0.0098
d	0.2	-	0.0079	-
E	2.1	2.64	0.0827	0.1039
e	1.2	1.4	0.0472	0.0551

SOT23-3



DIM	Millimeters		Inches	
	Min	Max	Min	Max
A	2.7	3.1	0.1063	0.122
B	1.7	2.1	0.0669	0.0827
b	0.35	0.5	0.0138	0.0197
C	1	1.2	0.0394	0.0472
c	0.1	0.25	0.0039	0.0098
d	0.2	-	0.0079	-
E	2.6	3	0.1023	0.1181
e	1.5	1.8	0.059	0.0708

SOT23-5



DIM	Millimeters		Inches	
	Min	**Max**	**Min**	**Max**
A	0.9	1.45	0.0354	0.057
A1	0	0.15	0	0.0059
A2	0.9	1.3	0.0354	0.0511
B	0.2	0.5	0.0078	0.0196
C	0.09	0.26	0.0035	0.0102
D	2.7	3.1	0.1062	0.122
E	2.2	3.2	0.0866	0.1181
E1	1.3	1.8	0.0511	0.0708
e	0.95REF		0.0374REF	
e1	1.90REF		0.0748REF	
L	0.1	0.6	0.0039	0.0236
a0	0	300	0	300