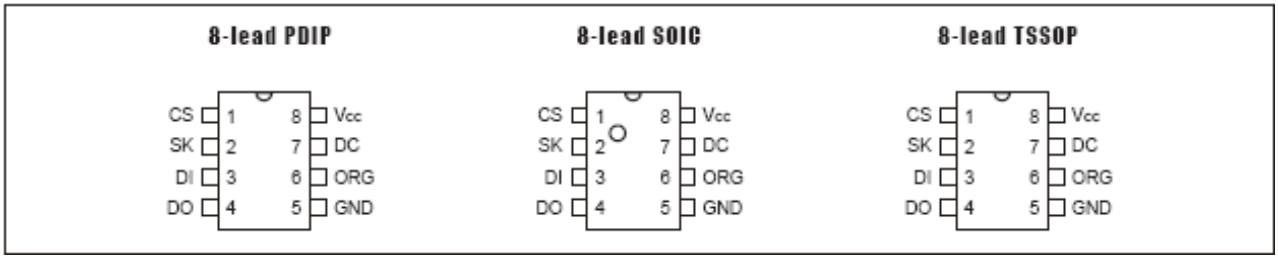
BL93C46

1K bits (128 X 8 or 64 X 16) Three-wire Serial EEPROM

■ Features

- Three-wire Serial Interface
- Vcc = 1.8V to 5.5V
- 2 MHz Rate (5V) Compatibility
- Self-timed Write Cycle (5 ms max)
- 1 Million Write Cycles guaranteed
- Data Retention > 100 Years
- 8-lead PDIP, 8-lead JEDEC SOIC and 8-lead TSSOP Packages



■ Description

The BL93C46 provides 1024 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 64 words of 16 bits each, when the ORG pin is connected to VCC and 128 words of 8 bits each when it is tied to ground. TheBL93C46 is available in space-saving 8-lead PDIP, 8-lead TSSOP and 8-lead JEDEC SOIC packages. The BL93C46 is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought “high” following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

Order information

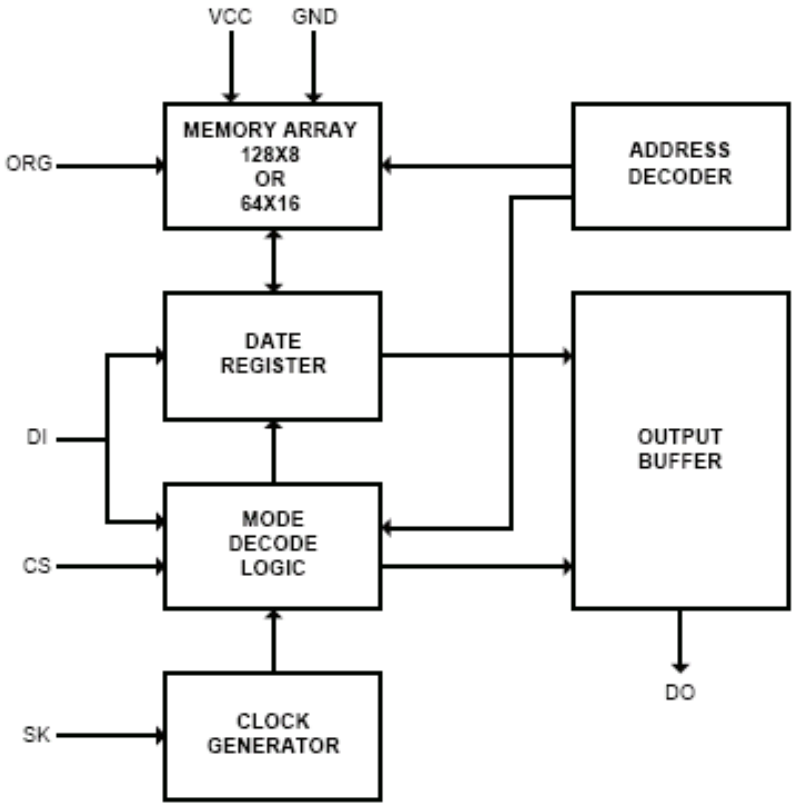
Part Number	Package	shipping
BL93C46-DIP	PDIP8	tube
BL93C46-SOP	SOP8	tube；2500 pcs / Tape & Reel
BL93C46-TSSOP	TSSOP8	tube；3000 pcs / Tape & Reel

■ Pin Descriptions

➤Table 1: Pin Configuration

Pin Name	Function
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

Block Diagram



Notes: When the ORG pin is connected to VCC, the "x 16" organization is selected. When it is connected to ground, the "x 8" organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the "x 16" organization is selected.

■ Electrical Characteristics

➤Absolute Maximum Ratings*

DC Supply Voltage . . . . . .-0.3V to +6.5V

Input / Output Voltage . . . . . GND-0.3V to Vcc+0.3V

Operating Ambient Temperature . . . . . -40°C to +85°C

Storage Temperature . . . . . -65°C to +150°C

➤*NOTICE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

■ Table 2.Pin Capacitance (1)

➤Applicable over recommended operating range from TA = 25°C, f = 1.0 MHz, VCC = +1.8V (unless otherwise noted)

Symbol	Test Conditions	Max	Unit	Conditions
COUT	Output Capacitance (DO)	5	pF	VOUT = 0V
CIN	Input Capacitance (CS, SK, DI)	5	pF	VIN = 0V

■ Table 3 . DC Characteristics

➤Applicable over recommended operating range from: TA = −40°C to +85°C, VCC = +1.8V to +5.5V, (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage	-		1.8	-	5.5	V
V_{CC2}	Supply Voltage	-		2.7	-	5.5	V
V_{CC3}	Supply Voltage	-		4.5	-	5.5	V
I_{CC}	Supply Current	V_{CC} = 5.0V	Read at 1.0 MHz	-	0.2	2.0	mA
			Write at 1.0 MHz	-	0.9	3.0	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V	CS = 0V	-	-	1.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V	CS = 0V	-	-	1.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V	CS = 0V	-	-	1.0	µA
$I_{IL(1)}$	Input Leakage	V_{IN} = 0V to V_{CC}		-	0.1	1.0	µA
$I_{IL(2)}$	Input Leakage	V_{IN} = 0V to V_{CC}		-	2.0	3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}		-	0.1	1.0	µA
$V_{IL1(3)}$	Input Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V		-0.3	-	0.8	
$V_{IH1(3)}$	Input High Voltage			2.0	-	V_{CC} + 0.3	V
$V_{IL2(3)}$	Input Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V		-0.3	-	V_{CC} + 0.3	
$V_{IH2(3)}$	Input High Voltage			V_{CC} x 0.7	-	V_{CC} + 0.3	V
V_{OL1}	Output Low Voltage	2.7V ≤ V_{CC} ≤ 5.5V	IOL = 2.1mA	-	-	0.4	V
V_{OH1}	Output High Voltage		IOH = -0.4mA	2.4	-		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} ≤ 2.7V	IOL = 0.15mA	-	-	0.2	V
V_{OH2}	Output High Voltage		IOH = -100µA	V_{CC}-0.2	-	-	V

Notes: 1. DI、CS、SK input pin
2. ORG input pin
3. VIL min and VIH max are reference only and are not tested.

■ AC Electrical Characteristics

➤Applicable over recommended operating range from TA = −40°C to + 85°C, VCC = +1.8V to + 5.5V,
CL = 1 TTL Gate and 100pF (unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
f_{SK}	SK Clock Frequency	4.5V ≤ Vcc ≤ ≤5.5V		0	-	2	MHz
		2.7V ≤ Vcc ≤ ≤5.5V		0		1	
		1.8V ≤ Vcc ≤ 5.5V		0		0.25	
t_{SKH}	SK High Time	4.5V ≤ Vcc ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ Vcc ≤ ≤5.5V		250			
		1.8V ≤ Vcc ≤ 5.5V		1000			
t_{SKL}	SK Low Time	4.5V ≤ Vcc ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ Vcc ≤ ≤5.5V		250			
		1.8V ≤ Vcc ≤ 5.5V		1000			
t_{CS}	Minimum CS Low Time	4.5V ≤ Vcc ≤ ≤5.5V		250	-	-	ns
		2.7V ≤ Vcc ≤ ≤5.5V		250			
		1.8V ≤ Vcc ≤ 5.5V		1000			
t_{CSS}	CS Setup Time	Relative to SK	4.5V ≤ Vcc ≤ ≤5.5V	50	-	-	ns
			2.7V ≤ Vcc ≤ ≤5.5V	50			
			1.8V ≤ Vcc ≤ 5.5V	200			
t_{DIS}	DI Setup Time	Relative to SK	4.5V ≤ Vcc ≤ ≤5.5V	100	-	-	ns
			2.7V ≤ Vcc ≤ ≤5.5V	100			
			1.8V ≤ Vcc ≤ 5.5V	400			
t_{CSH}	CS Hold Time	Relative to SK		0	-	-	ns
t_{DIH}	DI Hold Time	Relative to SK	4.5V ≤ Vcc ≤ ≤5.5V	100	-	-	ns
			2.7V ≤ Vcc ≤ ≤5.5V	100			
			1.8V ≤ Vcc ≤ 5.5V	400			
t_{PD1}	Output Delay to "1"	AC Test	4.5V ≤ Vcc ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ Vcc ≤ ≤5.5V			250	
			1.8V ≤ Vcc ≤ 5.5V			1000	
t_{PD0}	Output Delay to "0"	AC Test	4.5V ≤ Vcc ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ Vcc ≤ ≤5.5V			250	
			1.8V ≤ Vcc ≤ 5.5V			1000	
t_{SV}	CS to Status Valid	AC Test	4.5V ≤ Vcc ≤ ≤5.5V	-	-	250	ns
			2.7V ≤ Vcc ≤ ≤5.5V			250	
			1.8V ≤ Vcc ≤ 5.5V			1000	
t_{DF}	CS to DO in High Impedance	AC Test CS = VIL	4.5V ≤ Vcc ≤ ≤5.5V	-	-	100	ns
			2.7V ≤ Vcc ≤ ≤5.5V			100	
			1.8V ≤ Vcc ≤ 5.5V			400	
t_{WP}	Write Cycle Time	-	-	-	1.5	5	ms
Endurance(1)	5.0V, 25°C	-		1M	-	-	Write Cycle

Notes: 1. This parameter is characterized and is not 100% tested.

■ Functional Description

The BL93C46 is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic"1") followed by the appropriate op code and the desired memory address location.

Table5. Instruction Set for the **BL93C46**

Instruction	SB	OP Code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A_6 - A_0	A_5 - A_0			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXX	11XXXX			Write enable must precede all programming modes
ERASE	1	11	A_6 - A_0	A_5 - A_0			Erase memory location An - A0
WRITE	1	01	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Writes memory location An - A0
ERAL	1	00	10XXXXX	10XXXX			Erases all memory locations. Valid only at VCC = 4.5V to 5.5V
WRAL	1	00	01XXXXX	01XXXX	D_7 - D_0	D_{15} - D_0	Writes all memory locations. Valid only at VCC = 4.5V to 5.5V
EWDS	1	00	00XXXXX	00XXXX			Disables all programming instructions

Notes: The X's in the address field represent don't care values and must be clocked.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic "0") precedes the 8- or 16-bit data output string.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable(EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical "1" state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "1" at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, tWP, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic "0" at DO indicates that programming is still in progress. A logic "1" indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the selftimed programming cycle, TWP.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic "1" state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is

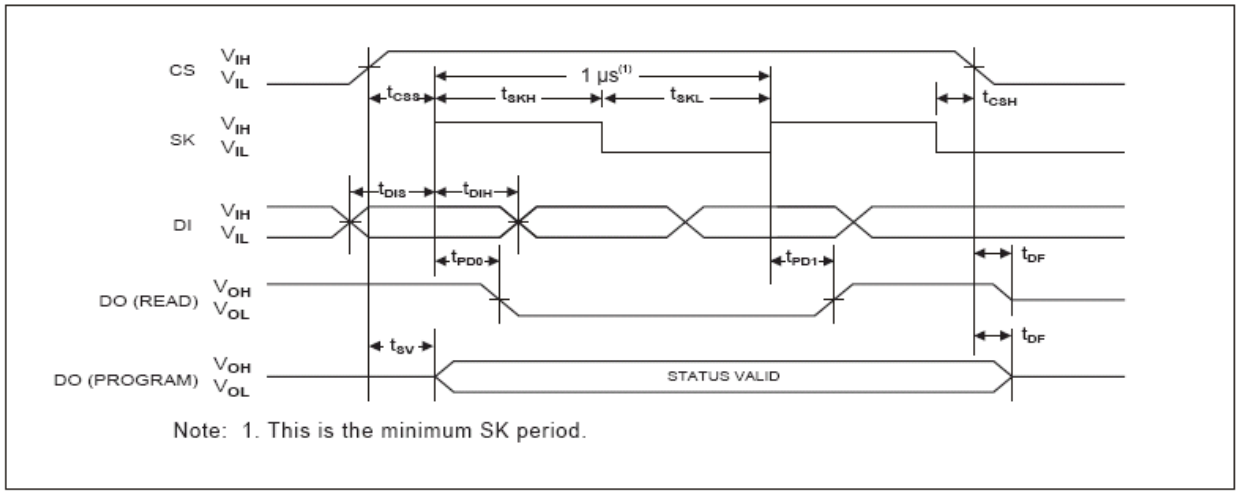
brought high after being kept low for a minimum of 250 ns (TCS). The ERAL instruction is valid only at VCC = 5.0V ± 10%.

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The WRAL instruction is valid only at VCC = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

■ Timing Diagrams

➤Figure 2: Synchronous Data Timing

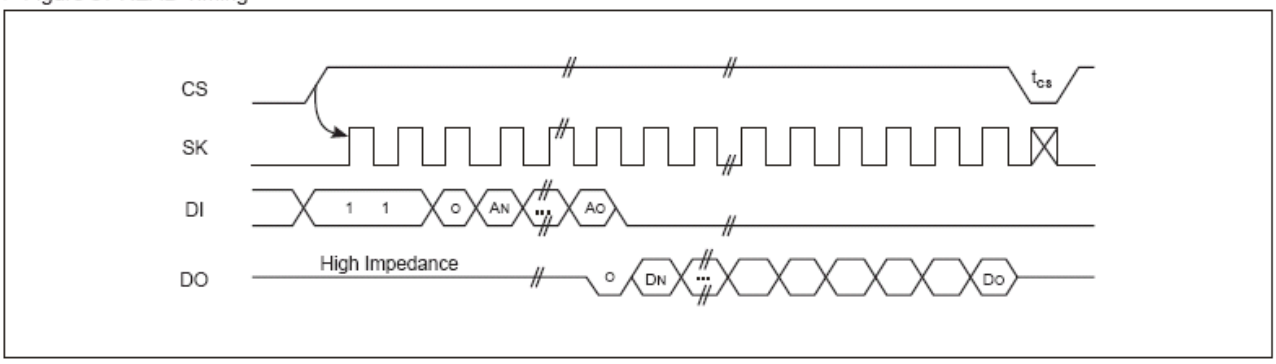


Note: 1. This is the minimum SK period.

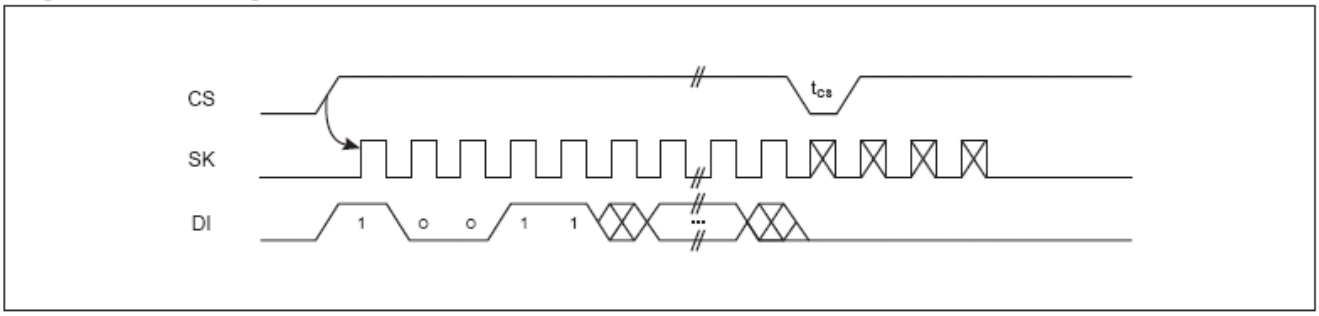
Table 6. Organization Key for Timing Diagrams

I/O	BL93C46	
	X 16	X 8
AN	A5	A6
DN	D15	D7

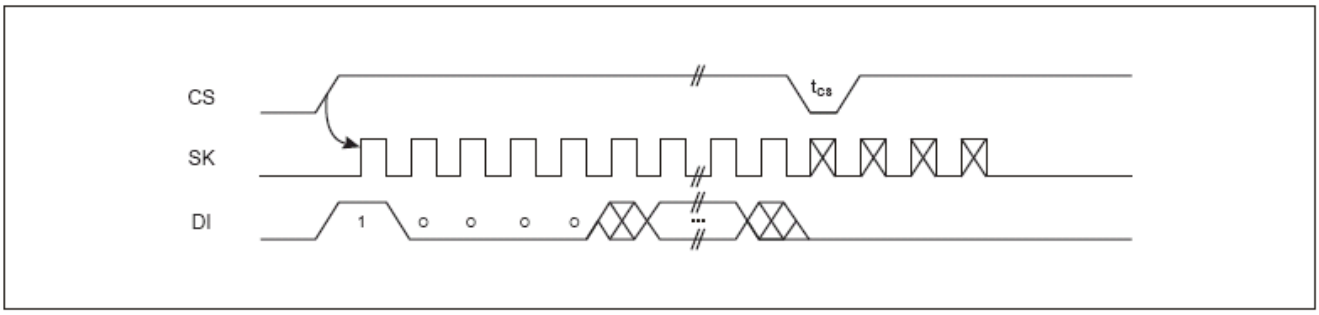
➤Figure 3: READ Timing



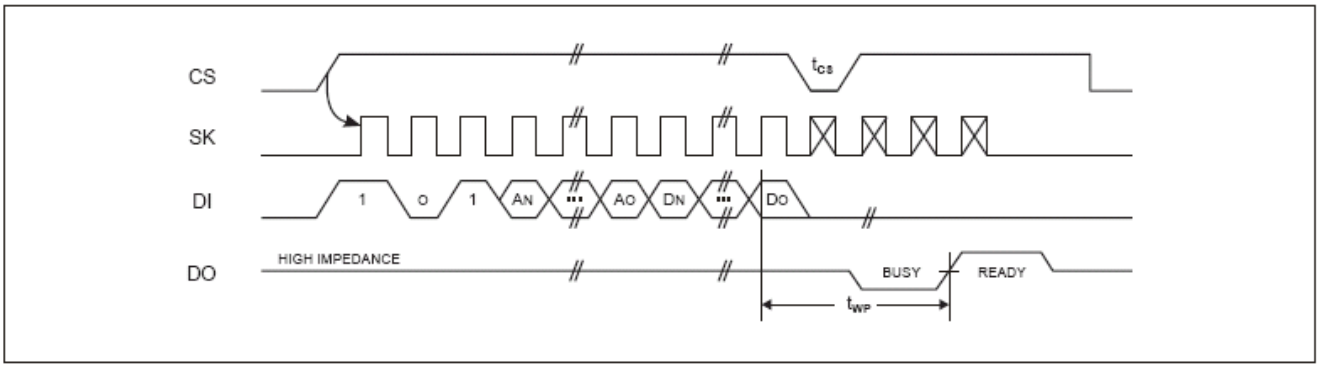
➤Figure 4: EWEN Timing



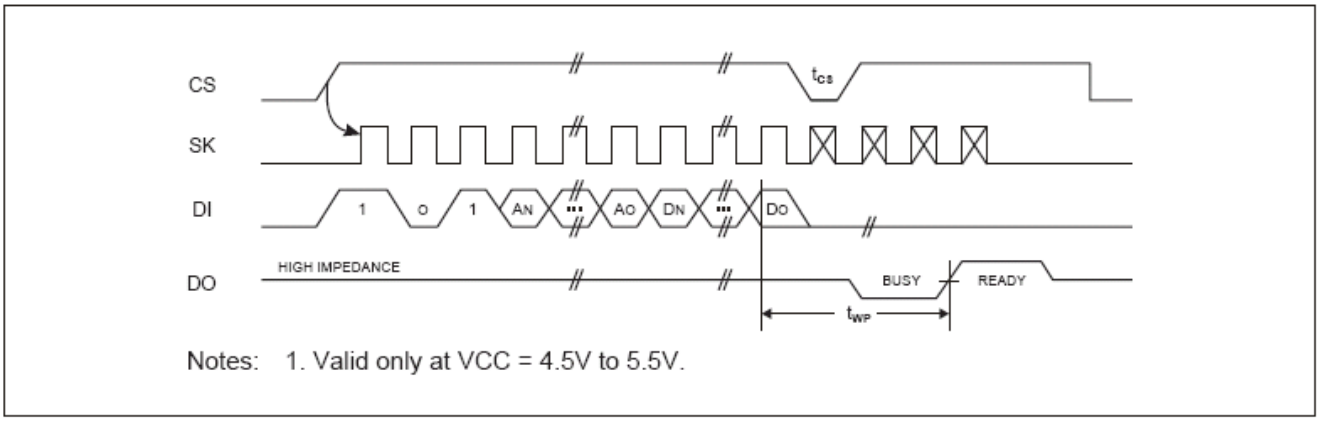
➤Figure 5: EWDS Timing



➤Figure 6: WRITE Timing

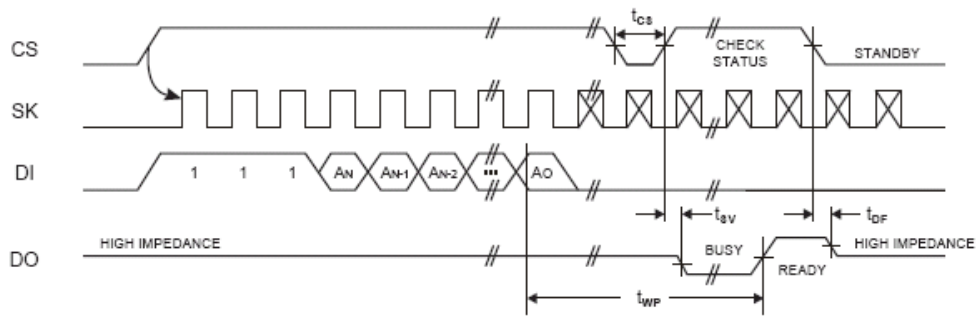


➤Figure 7: WRAL Timing(1)

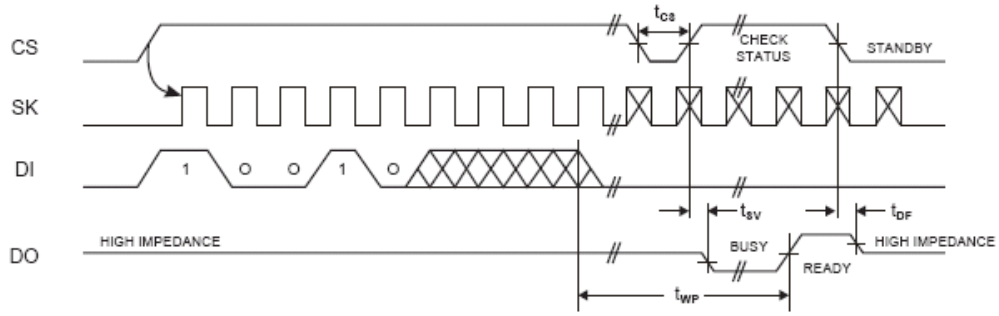


Notes: 1. Valid only at VCC = 4.5V to 5.5V.

➤Figure 8: ERASE Timing



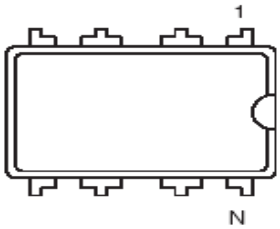
➤Figure 9: ERAL Timing(1)



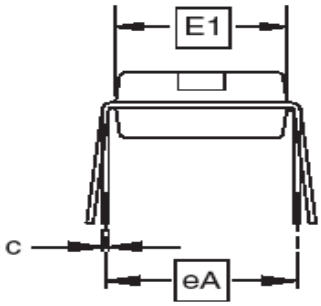
Notes: 1. Valid only at VCC = 4.5V to 5.5V.

Package Information

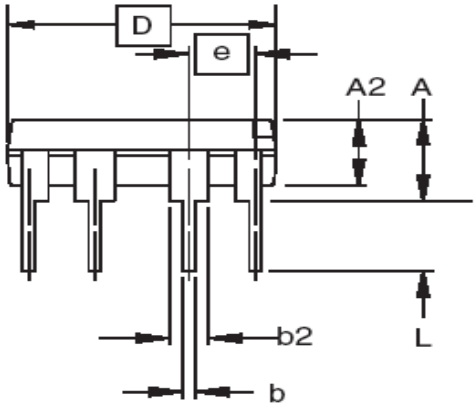
8-lead PDIP Outline Dimensions



Top View



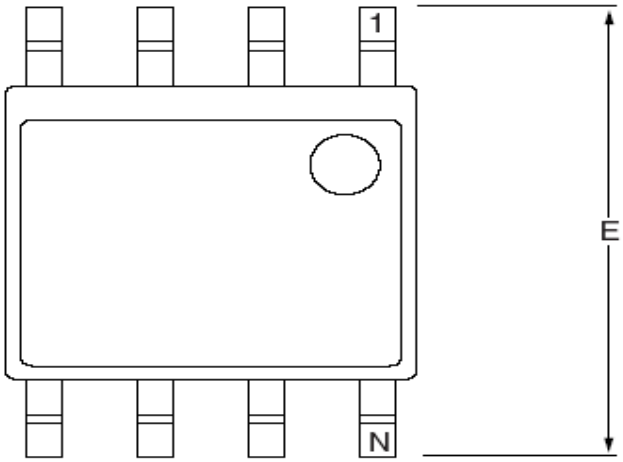
End View



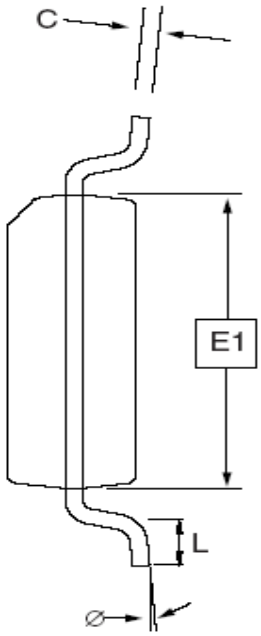
Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	3.60	3.80	4.00
A2	3.10	3.30	3.50
b	0.44	-	0.53
B1	1.52BSC		
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	9.05	9.25	9.45
E1	6.15	6.35	6.55
e	2.54BSC		
eA	7.62BSC		
L	3.00	-	-

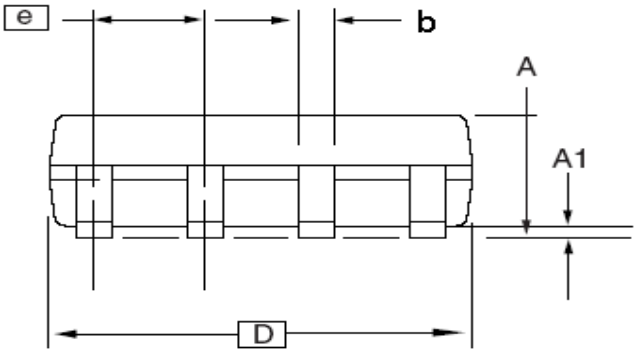
8-lead SOIC Outline Dimensions



Top View



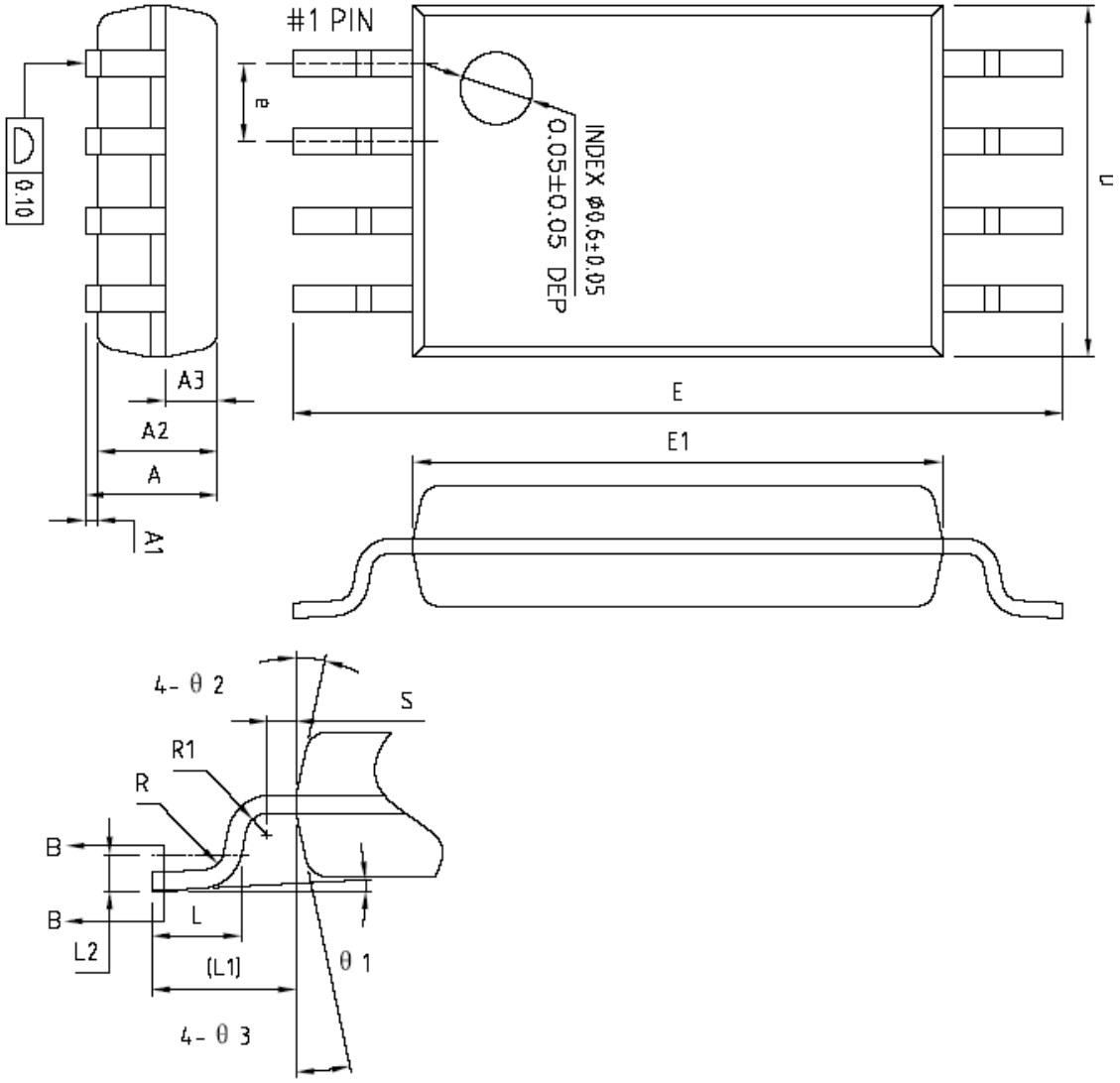
End View



Side View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.77
A1	0.08	0.18	0.28
b	0.44	-	0.53
c	0.21	-	0.26
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
Θ	0	-	8°

8-lead TSSOP Outline Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	-	0.28
b1	0.20	0.22	0.24
c	0.10	-	0.19
c1	0.10	0.13	0.15
D	2.83	2.93	3.03
E	6.20	6.40	6.60

E1	4.30	4.40	4.50
e	0.65BSC		
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
Θ1	0°	-	8°
Θ2	10°	12°	14°
Θ3	10°	12°	14°