# BLA6H0912L-1000; BLA6H0912LS-1000 LDMOS avionics power transistor

**AMPLEON** 

Rev. 5 — 1 September 2015

Product data sheet

### **Product profile**

### 1.1 General description

1000W LDMOS pulsed power transistor intended for avionics transmitter applications in the 960 MHz to 1215 MHz frequency range such as Mode-S, TCAS, JTIDS, DME and TACAN.

#### Table 1. **Application information**

Typical RF performance at  $T_{case} = 25$  °C;  $t_p = 50 \mu s$ ;  $\delta = 2$  %;  $I_{Dq} = 200$  mA; in a class-AB application circuit.

Test signal	f	V <sub>DS</sub>	$P_{L}$	G <sub>p</sub>	$\eta_{D}$	t <sub>r</sub>	t <sub>f</sub>
	(MHz)	(V)	(W)	(dB)	(%)	(ns)	(ns)
pulsed RF	1030	50	1000	16	52	11	5

#### 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (960 MHz to 1215 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

1000 W LDMOS pulsed power transistor intended for Mode-S, TCAS, JTIDS, DME and TACAN applications in the 960 MHz to 1215 MHz frequency range

### 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA6H0912	2L-1000 (SOT539A)		
1	drain1		
2	drain2	1 2	
3	gate1	5	3
4	gate2	3 4	5
5	source [1	Ī	4 7
			' <u></u>
			2 sym117
BLA6H0912	2LS-1000 (SOT539B)		
1	drain1		
2	drain2	1 2	1
3	gate1	5	
4	gate2	3 4	3 - 5
5	source [1	Ī	4
			' <del> </del>
			2 sym117
			, ,

<sup>[1]</sup> Connected to flange.

### 3. Ordering information

Table 3. Ordering information

Type number	Packaç	nckage		
	Name	ne Description		
BLA6H0912L-1000	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A	
BLA6H0912LS-1000	-	earless flanged balanced ceramic package; 4 leads	SOT539B	

### 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	100	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
T <sub>stg</sub>	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

### 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
Z <sub>th(j-c)</sub>	transient thermal impedance from	T <sub>case</sub> = 80 °C; P <sub>L</sub> = 1000 W		
	junction to case	t <sub>p</sub> = 50 μs; δ = 2 %	0.011	K/W
		$t_p$ = 100 $\mu$ s; $\delta$ = 10 %	0.021	K/W
		$t_p$ = 200 $\mu$ s; $\delta$ = 10 %	0.025	K/W
		$t_p$ = 300 $\mu$ s; $\delta$ = 10 %	0.027	K/W
		$t_p$ = 2.4 ms; $\delta$ = 6.4 %	0.041	K/W

### 6. Characteristics

Table 6. DC characteristics

 $T_i = 25$  °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 4 \text{ mA}$	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 400 mA	1.25	1.8	2.25	V
I <sub>DSS</sub>	drain leakage current	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 50 V	-	-	2.8	μΑ
I <sub>DSX</sub>	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	62	-	Α
$I_{GSS}$	gate leakage current	$V_{GS} = 11 \text{ V}; V_{DS} = 0 \text{ V}$	-	-	280	nA
9 <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 10 V; I <sub>D</sub> = 20 A	-	34	-	S
R <sub>DS(on)</sub>	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 14 \text{ A}$	_	75	-	mΩ

Table 7. RF characteristics

Test signal: pulsed RF;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %; RF performance at  $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $T_{case}$  = 25 °C; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DS}$	drain-source voltage	P <sub>L</sub> = 1000 W	-	-	50	V
G <sub>p</sub>	power gain	P <sub>L</sub> = 1000 W	14	15.5	-	dB
RLin	input return loss	P <sub>L</sub> = 1000 W	-	-19	-11	dB
$\eta_{D}$	drain efficiency	P <sub>L</sub> = 1000 W	47	51	-	%
P <sub>droop(pulse)</sub>	pulse droop power	P <sub>L</sub> = 1000 W	-	0	0.3	dB
t <sub>r</sub>	rise time	P <sub>L</sub> = 1000 W	-	11	30	ns
t <sub>f</sub>	fall time	P <sub>L</sub> = 1000 W	-	5	30	ns

### 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLA6H0912L-1000 and the BLA6H0912LS-1000 are capable of withstanding a load mismatch corresponding to VSWR = 3 : 1 through all phases under the following conditions:  $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA;  $P_{L}$  = 1000 W;  $I_{p}$  = 50  $\mu$ s;  $\delta$  = 2 %; f = 1030 MHz.

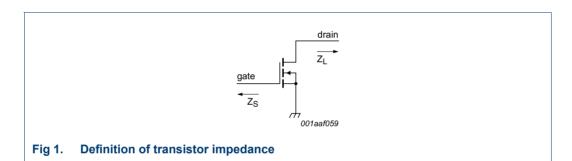
### 7.2 Impedance information

Table 8. Typical impedance

Typical values per section unless otherwise specified.

f	Z <sub>S</sub>	Z <sub>L</sub> [1]	<b>Z</b> <sub>L</sub> [2]
(MHz)	(Ω)	(Ω)	(Ω)
950	1.12 – j2.27	0.60 + j0.21	0.62 - j0.02
1000	1.39 – j2.69	0.54 + j0.08	0.66 - j0.06
1050	1.79 – j2.79	0.40 + j0.03	0.52 - j0.28
1100	2.44 – j2.72	0.41 – j0.12	0.67 – j0.29
1150	1.68 – j2.52	0.49 – j0.21	0.53 – j0.35
1200	4.68 – j2.97	0.36 - j0.30	0.57 – j0.40

- [1] Optimized for drain efficiency.
- [2] Optimized for power gain.



### 7.3 Circuit information

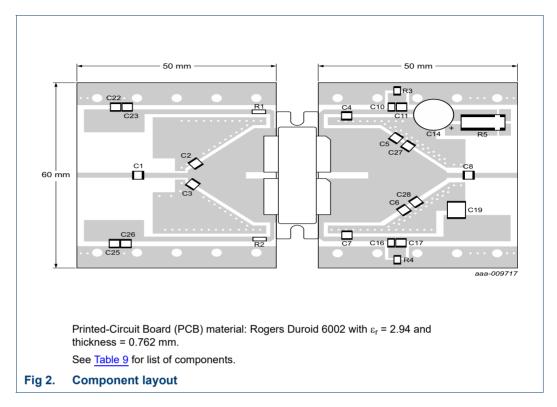


Table 9. List of components

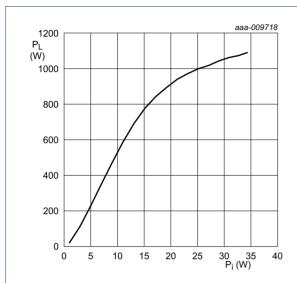
See <u>Figure 2</u> for component layout.

Component	Description	Value	Remarks
C1, C4, C7, C8, C22, C25	multilayer ceramic chip capacitor	33 pF [1]	
C2, C3, C27, C28	multilayer ceramic chip capacitor	6.2 pF [1]	
C5, C6	multilayer ceramic chip capacitor	3.9 pF [1]	
C23, C26	multilayer ceramic chip capacitor	1 nF [1]	
C10, C16	multilayer ceramic chip capacitor	10 nF	Murata
C11, C17	multilayer ceramic chip capacitor	100 nF	TDK
C14	electrolytic capacitor	220 μF, 63 V	
C19	multilayer ceramic chip capacitor	10 μF, 100 V	
R1	SMD resistor	1 kΩ	SMD 0603
R2	SMD resistor	20 Ω	SMD 0603
R3, R4	SMD resistor	2.4 Ω	SMD 0603
R5	current sense resistor	0.005 Ω	

[1] American Technical Ceramics type 100B or capacitor of same quality.

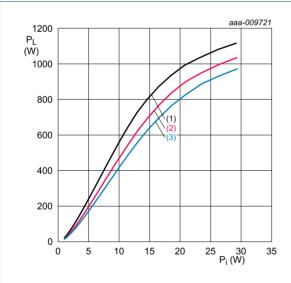
### 7.4 Graphical data

#### 7.4.1 Pulsed CW



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $t_p$  = 50  $\mu s$ ;

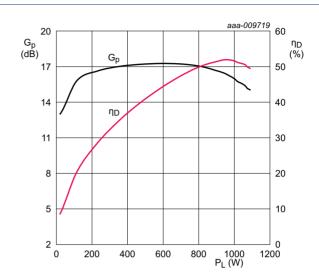
Fig 3. Output power as a function of input power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $t_p$  = 50  $\mu s$ ;  $\delta = 2 \%$ 

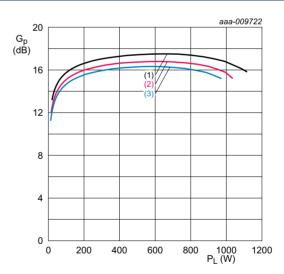
- (1) T<sub>case</sub> = 20 °C
- (2)  $T_{case} = 50 \, ^{\circ}C$
- (3)  $T_{case} = 70 \, ^{\circ}C$

Output power as a function of input power; Fig 5. typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $t_p$  = 50  $\mu s$ ;

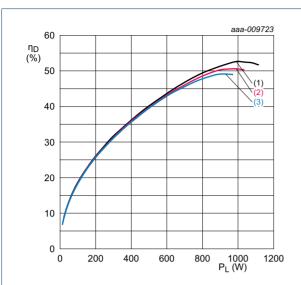
Fig 4. Power gain and drain efficiency as function of output power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $t_p$  = 50  $\mu s$ ;  $\delta$  = 2 %.

- (1)  $T_{case} = 20 \, ^{\circ}C$
- (2)  $T_{case} = 50 \, ^{\circ}C$
- (3)  $T_{case} = 70 \, ^{\circ}C$

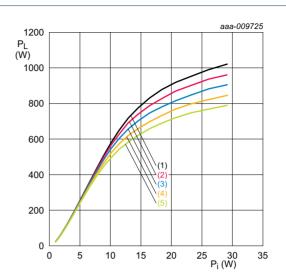
Fig 6. Power gain as a function of output power; typical values



 $V_{DS}$  = 50 V;  $I_{Dq}$  = 200 mA; f = 1030 MHz;  $t_p$  = 50  $\mu s;$   $\delta$  = 2 %.

- (1) T<sub>case</sub> = 20 °C
- (2)  $T_{case} = 50 \, ^{\circ}C$
- (3)  $T_{case} = 70 \, ^{\circ}C$

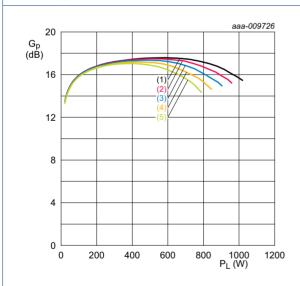
Fig 7. Drain efficiency as a function of output power; typical values



 $I_{Dq} = 200 \text{ mA}$ ;  $t_p = 50 \text{ } \mu\text{s}$ ;  $\delta = 2 \text{ } \%$ .

- (1)  $V_{DS} = 50 \text{ V}$
- (2)  $V_{DS} = 48 \text{ V}$
- (3)  $V_{DS} = 46 \text{ V}$
- (4)  $V_{DS} = 44 V$
- (5)  $V_{DS} = 42 \text{ V}$

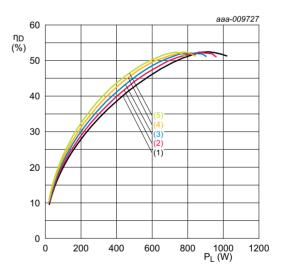




 $I_{Dq}$  = 200 mA;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %.

- (1)  $V_{DS} = 50 \text{ V}$
- (2)  $V_{DS} = 48 \text{ V}$
- (3)  $V_{DS} = 46 \text{ V}$
- (4)  $V_{DS} = 44 V$
- (5)  $V_{DS} = 42 V$

Fig 9. Power gain as a function of output power; typical values



 $I_{Dq}$  = 200 mA;  $t_p$  = 50  $\mu$ s;  $\delta$  = 2 %.

- (1)  $V_{DS} = 50 \text{ V}$
- (2)  $V_{DS} = 48 \text{ V}$
- (3)  $V_{DS} = 46 \text{ V}$
- (4)  $V_{DS} = 44 V$
- (5)  $V_{DS} = 42 V$

Fig 10. Drain efficiency as a function of output power; typical values

#### Package outline 8.

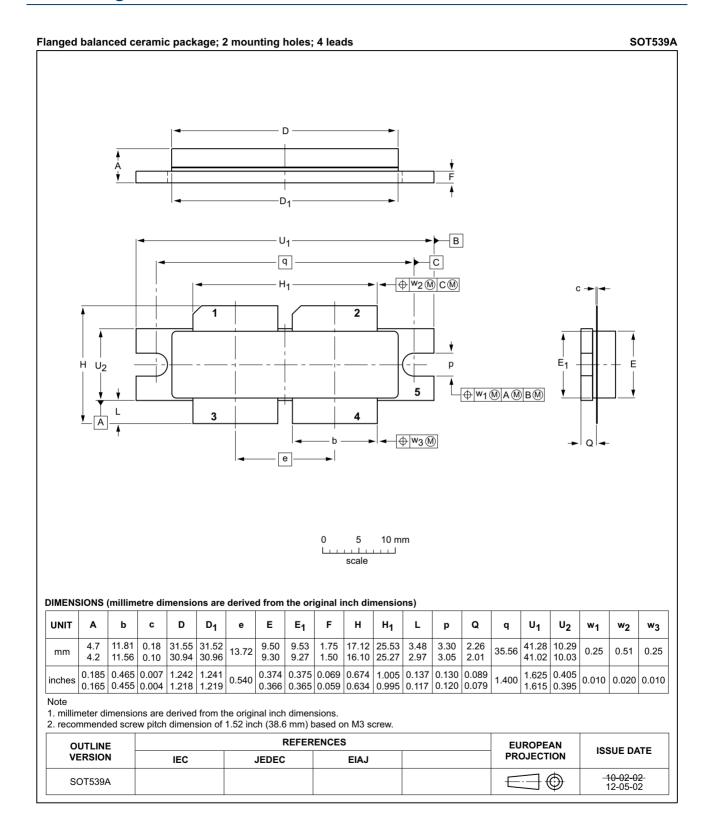


Fig 11. Package outline SOT539A

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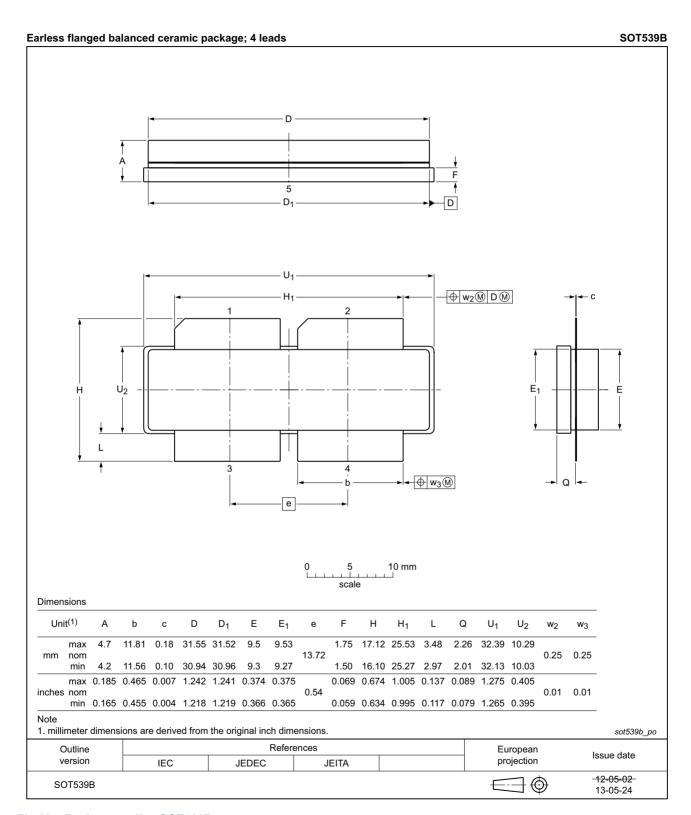


Fig 12. Package outline SOT539B

### 9. Handling information

#### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

### 10. Abbreviations

Table 10. Abbreviations

Acronym	Description	
CW	Continuous Wave	
DME	Distance Measuring Equipment	
ESD	ElectroStatic Discharge	
JTIDS	oint Tactical Information Distribution System	
LDMOS	Laterally Diffused Metal-Oxide Semiconductor	
Mode-S	Mode Select	
MTF	Median Time to Failure	
SMD	Surface Mounted Device	
TACAN	TACtical Air Navigation	
TCAS	raffic Collision Avoidance System	
VSWR	Voltage Standing-Wave Ratio	

### 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6H0912L-1000_0912LS-1000#5	20150901	Product data sheet	-	BLA6H0912L-1000_ 0912LS-1000 v.4
Modifications	<ul> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> </ul>			
	<ul> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLA6H0912L-1000_0912LS-1000 v.4	20150702	Product data sheet	-	BLA6H0912L-1000_ 0912LS-1000 v.3
BLA6H0912L-1000_0912LS-1000 v.3	20150615	Product data sheet	-	BLA6H0912L-1000_ 0912LS-1000 v.2
BLA6H0912L-1000_0912LS-1000 v.2	20140210	Objective data sheet	-	BLA6H0912L-1000_ 0912LS-1000 v.1
BLA6H0912L-1000_0912LS-1000 v.1	20131104	Objective data sheet	-	-

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Document status[1][2]	Product status[3]	Definition	
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## BLA6H0912L(S)-1000

#### LDMOS avionics power transistor

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### **AMPLEON**

# BLA6H0912L(S)-1000

### **LDMOS** avionics power transistor

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