# BLC2425M8LS300P

**Power LDMOS transistor**

AMPLEON

**Rev. 3 — 17 June 2016** **Poduct data sheet**

## 1. Product profile

### 1.1 General description

300 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLC2425M8LS300P is designed for high-power CW applications and is assembled in a high performance plastic package.

**Table 1. Typical performance**

*RF performance at $V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA; $T_{case}$ = 25 °C in a class-AB application circuit.*

| Test signal | f | $V_{DS}$ | $P_{L(AV)}$ | $G_p$ | $\eta_D$ |
|---|---|---|---|---|---|
| | (MHz) | (V) | (W) | (dB) | (%) |
| CW | 2450 | 32 | 300 | 17.0 | 58.0 |
| CW pulsed [1] | 2450 | 32 | 300 | 17.5 | 61.0 |

[1] $t_p$ = 100 μs; δ = 10 %

### 1.2 Features and benefits

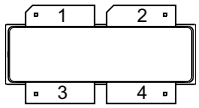
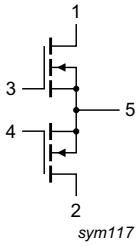
- High efficiency
- Easy power control
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM applications and heating

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| 1 | drain1 |  |  |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| flange | source | | |



## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BLC2425M8LS300P | - | air cavity plastic earless flanged package; 4 leads | SOT1250-1 |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | - | 65 | V |
| $V_{GS}$ | gate-source voltage | | –0.5 | +13 | V |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | [1] | - | 225 | °C |

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j\text{-}case)}$ | thermal resistance from junction to case | $T_{case}$ = 80 °C; $P_L$ = 300 W | 0.2 | K/W |

# 6. Characteristics

**Table 6. DC characteristics**

*$T_j$ = 25 °C, per section; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 2.2 mA | 65 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS}$ = 10 V; $I_D$ = 220 mA | 1.5 | 1.9 | 2.3 | V |
| $I_{DSS}$ | drain leakage current | $V_{GS}$ = 0 V; $V_{DS}$ = 28 V | - | - | 2.8 | μA |
| $I_{DSX}$ | drain cut-off current | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $V_{DS}$ = 10 V | - | 39 | - | A |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 11 V; $V_{DS}$ = 0 V | - | - | 280 | nA |
| $g_{fs}$ | forward transconductance | $V_{DS}$ = 10 V; $I_D$ = 11 A | - | 16 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $I_D$ = 7.7 A | - | 0.08 | - | Ω |

**Table 7. RF characteristics**

*Test signal: CW at 2450 MHz; RF performance at $V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA; $T_{case}$ = 25 °C; unless otherwise specified; in a class-AB production test circuit.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_p$ | power gain | $P_L$ = 300 W | 16.3 | 17.5 | - | dB |
| $RL_{in}$ | input return loss | $P_L$ = 300 W | - | –14 | –7 | dB |
| $\eta_D$ | drain efficiency | $P_L$ = 300 W | 49 | 54.5 | - | % |

# 7. Test information

## 7.1 Ruggedness in class-AB operation

The BLC2425M8LS300P is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA; $P_L$ = 300 W (CW); f = 2450 MHz.

## 7.2 Impedance information

**Table 8. Typical impedance**

*Measured load-pull data half device. Typical values unless otherwise specified. $I_{Dq}$ = 20 mA; $V_{DS}$ = 32 V.*

| f | $Z_S$ [1] | $Z_L$ [1] |
|---|---|---|
| (MHz) | (Ω) | (Ω) |
| 2400 | 1.2 – 5.9j | 3.7 – 2.8j |
| 2450 | 1.3 – 5.0j | 3.2 – 2.5j |
| 2500 | 3.3 – 7.0j | 3.1 – 2.3j |

[1] $Z_S$ and $Z_L$ defined in Figure 1.

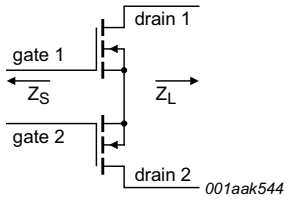
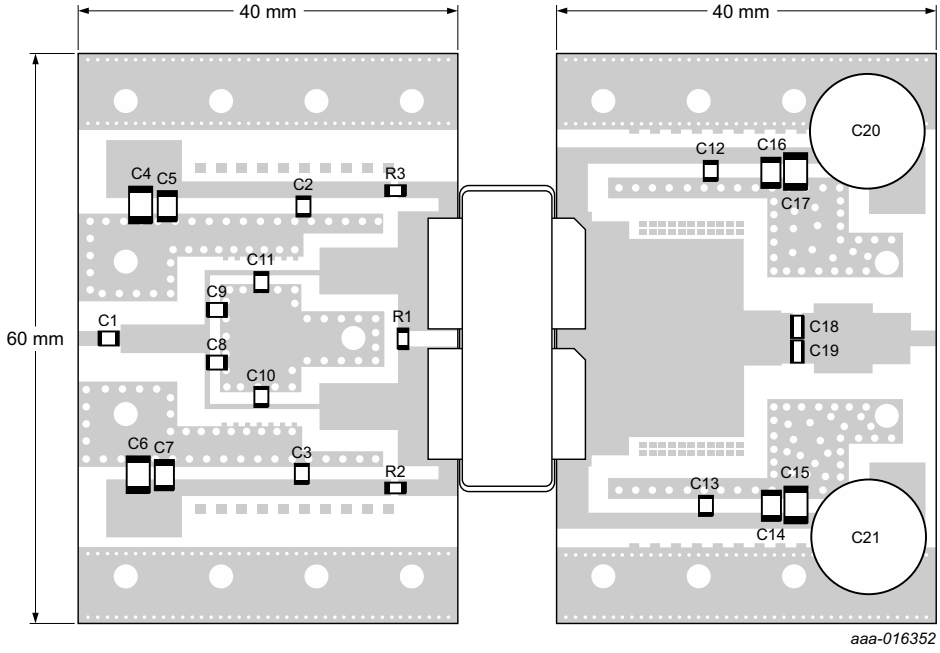



**Fig 1. Definition of transistor impedance**

## 7.3 Test circuit




Printed-Circuit Board (PCB): Rogers RT/Duroid 6035HTC; thickness = 0.762 mm; thickness copper plating = 35 μm.

See Table 9 for a list of components.

**Fig 2. Component layout for production test circuit**

**Table 9. List of components**

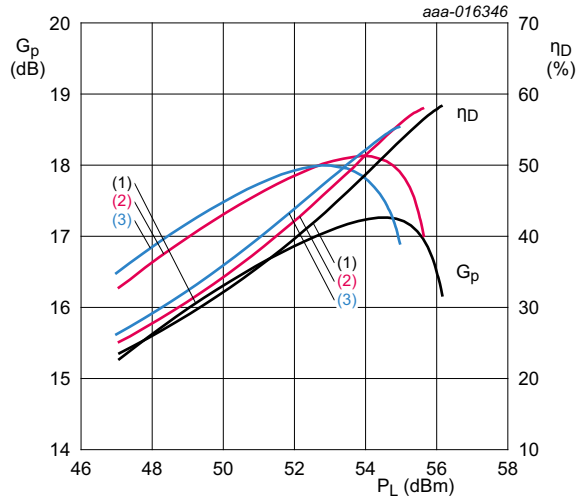
*See Figure 2 for component layout.*

| Component | Description | Value | Remarks |
|---|---|---|---|
| C1, C2, C3, C12, C13 | multilayer ceramic chip capacitor | 36 pF | ATC 800B |
| C4, C6, C15, C17 | multilayer ceramic chip capacitor | 10 μF, 50 V | |
| C5, C7, C14, C16 | multilayer ceramic chip capacitor | 470 nF, 50 V | |
| C8, C9 | multilayer ceramic chip capacitor | 1.4 pF | ATC 100B |
| C10, C11 | multilayer ceramic chip capacitor | 1.8 pF | ATC 100B |
| C18, C19 | multilayer ceramic chip capacitor | 24 pF | ATC 800R |

**Table 9. List of components** *...continued*
*See Figure 2 for component layout.*

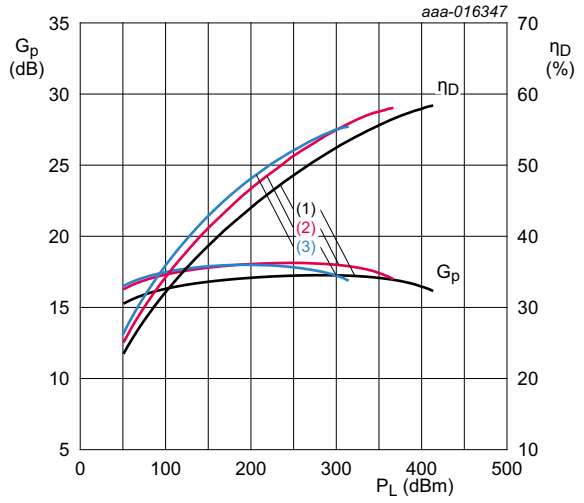
| Component | Description | Value | Remarks |
|---|---|---|---|
| C20, C21 | electrolytic capacitor | 470 μF, 63 V | |
| R1 | resistor | 9.1 Ω | SMD 0805 |
| R2, R3 | resistor | 5.1 Ω | SMD 0805 |

## 7.4 Graphical data



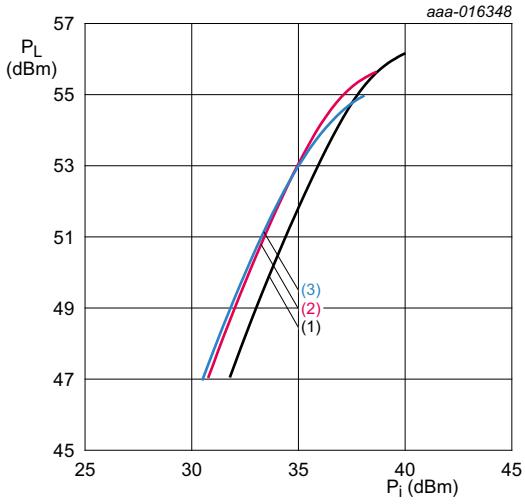

$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.
(1) f = 2400 MHz
(2) f = 2450 MHz
(3) f = 2500 MHz

**Fig 3. Power gain and drain efficiency as function of output power; typical values**




$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.
(1) f = 2400 MHz
(2) f = 2450 MHz
(3) f = 2500 MHz

**Fig 4. Power gain and drain efficiency as function of output power; typical values**



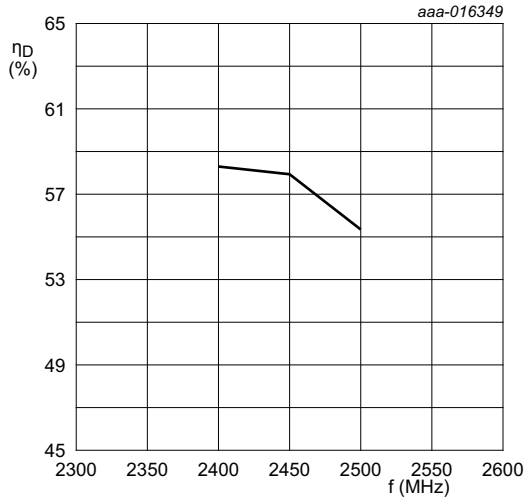

$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.

(1) f = 2400 MHz

(2) f = 2450 MHz

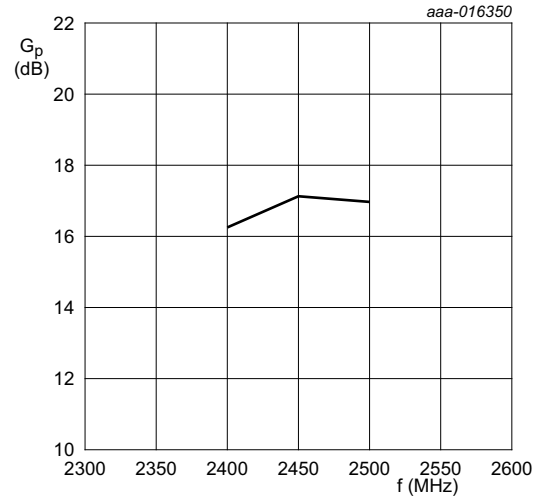
(3) f = 2500 MHz

**Fig 5. Output power as a function of input power; typical values**



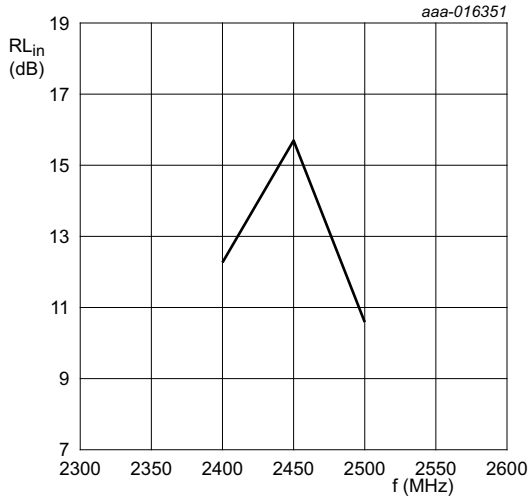

$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.

**Fig 6. Drain efficiency as a function of frequency; typical values**



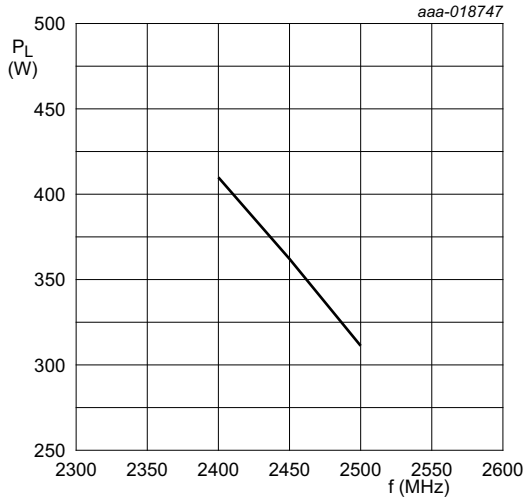

$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.

**Fig 7. Power gain as a function of frequency; typical values**




$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.

**Fig 8. Input return loss as a function of frequency; typical values**

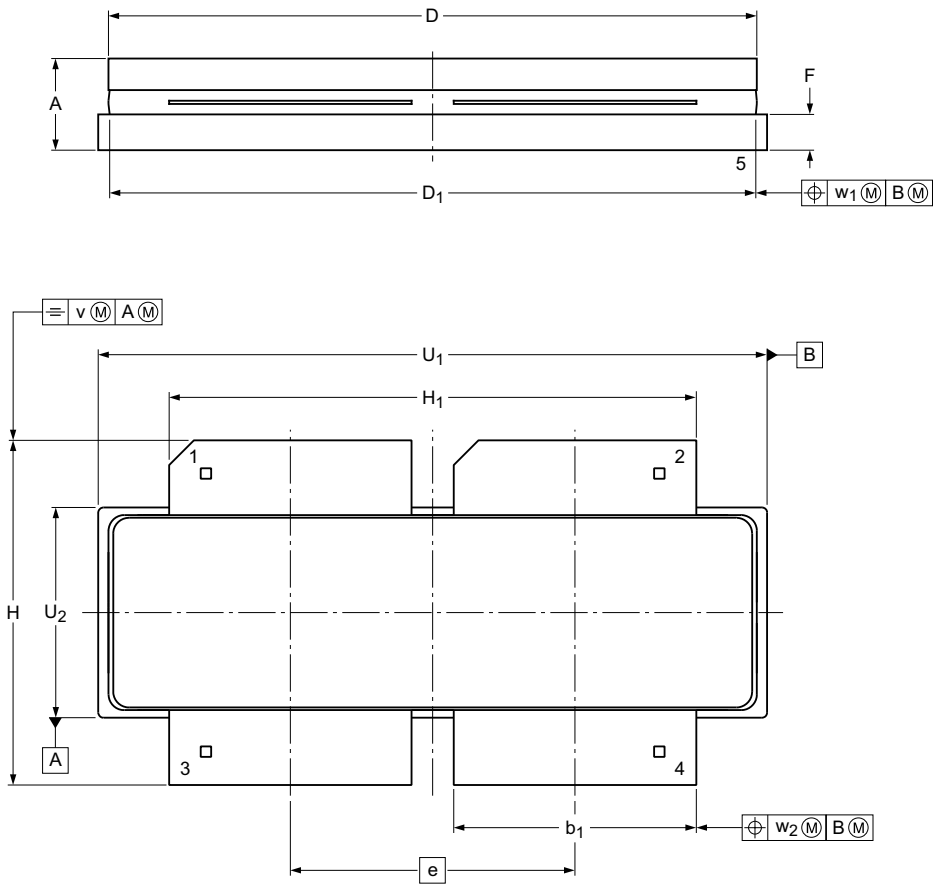



$V_{DS}$ = 32 V; $I_{Dq}$ = 20 mA.

**Fig 9. Output power as a function of frequency; typical values**

# 8. Package outline

**Plastic earless flanged cavity package; 4 leads** **SOT1250-1**




Dimensions (mm dimensions are derived from the original inch dimension)

| Unit | | A | $b_1$ | c | D | $D_1$ | E | $E_1$ | e | F | H | $H_1$ | Q(1) | $U_1$ | $U_2$ | v | $w_1$ | $w_2$ | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 4.65 | 11.79 | 0.18 | 31.44 | 31.34 | 9.60 | 9.50 | | 1.83 | 16.71 | 25.50 | 2.33 | 32.33 | 10.23 | 0.50 | 0.50 | 0.50 | 0.10 |
| | nom | | | | | | | | 13.72 | | | | | | | | | | |
| | min | 4.18 | 11.58 | 0.13 | 31.04 | 31.14 | 9.20 | 9.30 | | 1.63 | 16.51 | 25.30 | 2.13 | 32.13 | 10.03 | | | | |

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

*sot1250-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1250-1 | | | | | | ~~13-09-03~~ 16-05-20 |

**Fig 10. Package outline SOT1250-1**

## 9. Handling information

| CAUTION | |
|---|---|
|  | This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.<br>Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards. |

## 10. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CW | Continuous Wave |
| ESD | ElectroStatic Discharge |
| LDMOS | Laterally Diffused Metal-Oxide Semiconductor |
| MTF | Median Time to Failure |
| SMD | Surface Mounted Device |
| VSWR | Voltage Standing-Wave Ratio |

## 11. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BLC2425M8LS300P v.3 | 20160617 | Product data sheet | - | BLC2425M8LS300P#2 |
| Modifications | • Table 7 on page 3: table updated<br>• Figure 10 on page 8: figure updated | | | |
| BLC2425M8LS300P#2 | 20150901 | Objective data sheet | - | BLC2425M8LS300P v.1 |
| BLC2425M8LS300P v.1 | 20150703 | Objective data sheet | - | - |

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| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 14. Contents





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