BLC9G20LS-240PV

Power LDMOS transistor

Rev. 4 — 24 May 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

240 W LDMOS power transistor with enhanced video bandwidth for base station applications at frequencies from 1805 MHz to 1995 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Test signal	f	I_{Dq}	V_{DS}	$P_{L(AV)}$	G_p	η_D	$ACPR_{5M}$
	(MHz)	(mA)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	1805 to 1880	1600	28	60	18.0	30	–30 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 8.4 dB at 0.01 % probability on CCDF per carrier; 5 MHz carrier spacing.

1.2 Features and benefits

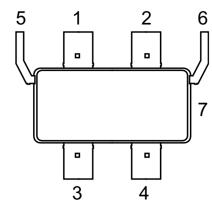
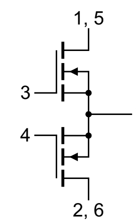
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable enhanced video bandwidth performance (70 MHz typical)
- Designed for broadband operation (1805 MHz to 1995 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1995 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 aaa-007731
2	drain2		
3	gate1		
4	gate2		
5	video decoupling		
6	video decoupling		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20LS-240PV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 60 W	0.4	K/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.6 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 150 mA	1.5	1.9	-	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 800 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	25.4	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 20 V; I_D = 7.5 A	-	10	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.3 A	-	0.1	-	Ω

Table 7. RF characteristics
Test signal: 2-carrier W-CDMA; 3GPP test model 1 with 64 DPCH; PAR = 8.4 dB at 0.01 % probability on the CCDF; f_1 = 1807.5 MHz; f_2 = 1812.5 MHz; f_3 = 1872.5 MHz; f_4 = 1877.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1600 mA; T_{case} = 25 °C; unless otherwise specified; in a water cooled class-AB test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 60 W	16.8	18.0	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 60 W	27	30	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 60 W	-	−15	−9	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 60 W	-	−30	−25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLC9G20LS-240PV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1600 mA; 2-carrier W-CDMA signal; P_L = 120 W average; f_c = 1805 MHz; 5 MHz spacing; 46 % clipping.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data per section; I_{Dq} = 800 mA; V_{DS} = 28 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1805	2.2 – j7.3	2.4 – j8.0	201.0	60.4	15.4
1840	2.3 – j8.0	2.4 – j8.6	199.4	58.6	15.4
1880	2.8 – j8.3	2.2 – j8.7	200.6	59.5	15.6
1930	3.6 – j8.5	2.3 – j8.9	195.2	58.9	15.8
1960	5.0 – j8.7	2.2 – j9.0	192.7	57.8	16.0
1990	6.4 – j9.2	2.4 – j9.0	190.6	58.3	16.3
Maximum drain efficiency load					
1805	2.2 – j7.3	3.4 – j5.0	120.8	71.3	18.0
1840	2.3 – j8.0	3.1 – j6.0	134.7	69.8	17.8
1880	2.8 – j8.3	2.5 – j6.2	127.0	69.9	18.0
1930	3.6 – j8.5	2.4 – j6.6	127.6	68.3	18.3
1960	5.0 – j8.7	2.4 – j6.7	127.4	68.2	18.7
1990	6.4 – j9.2	2.2 – j6.9	133.5	67.4	18.7

[1] Z_S and Z_L defined in Figure 1.

[2] at 3 dB gain compression.

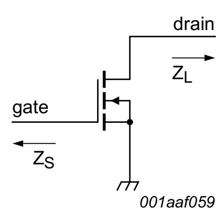
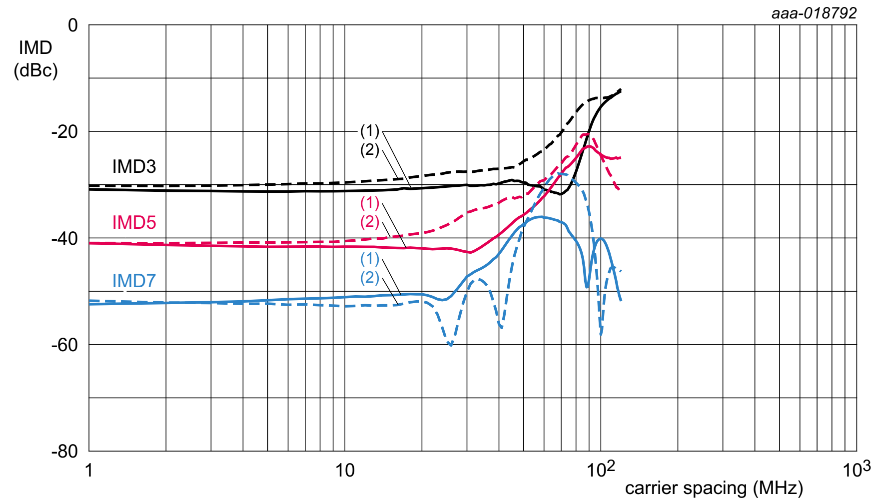


Fig 1. Definition of transistor impedance

7.3 VBW in a class-AB operation

The BLC9G20LS-240PV shows 70 MHz (typical) video bandwidth (IMD third-order intermodulation inflection point) in a class-AB test circuit in the 1805 MHz to 1880 MHz band at V_{DS} = 28 V and I_{Dq} = 1600 mA.



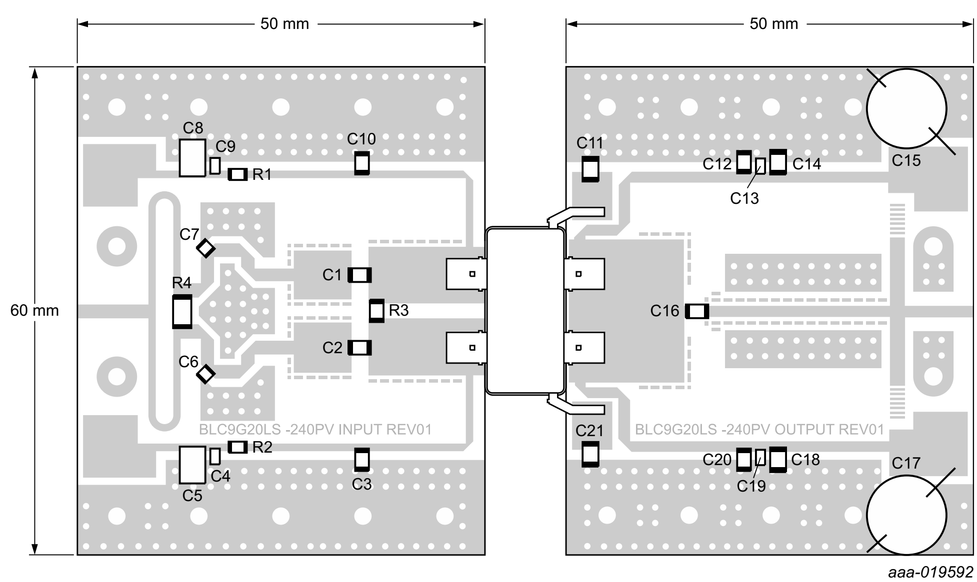
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) low

(2) high

Fig 2. VBW capability in class-AB test circuit

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B with a thickness of 0.76 mm.

See Table 9 for a list of components.

Fig 3. Component layout for test circuit

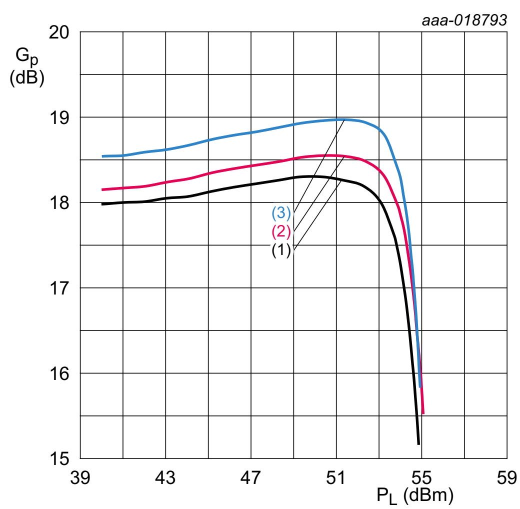
Table 9. List of components

See Figure 3 for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	0.5 pF	ATC 800B
C3, C10, C12, C20	multilayer ceramic chip capacitor	24 pF	ATC 800B
C4, C9	multilayer ceramic chip capacitor	100 nF	Murata
C5, C8	multilayer ceramic chip capacitor	1 μF	Murata
C6, C7	multilayer ceramic chip capacitor	3.3 pF	ATC 800A
C11, C14, C18, C21	multilayer ceramic chip capacitor	470 μF, 50 V	Murata
C13, C19	multilayer ceramic chip capacitor	220 nF	Murata
C15, C17	electrolytic capacitor	> 470 μF, 63 V	low ESR
C16	multilayer ceramic chip capacitor	1.2 pF	ATC 800B
R1, R2	resistor	4.7 Ω, 1 % tolerance	SMD 0805
R3	resistor	10 Ω, 1 % tolerance	SMD 0805
R4	resistor	100 Ω, 1 % tolerance	SMD 2010

7.5 Graphical data

7.5.1 Pulsed CW



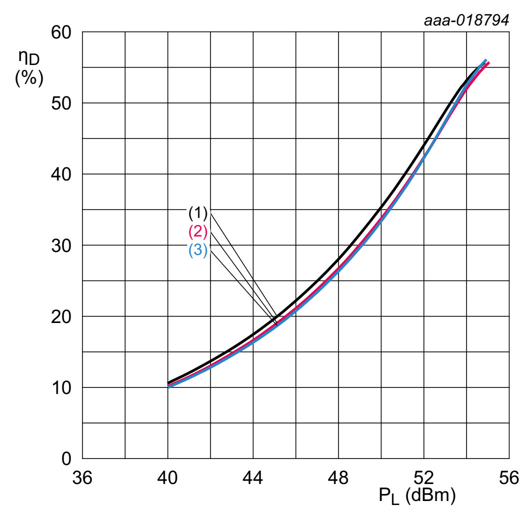
V_{DS} = 28 V; I_{Dq} = 1600 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 4. Power gain as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA; t_p = 100 μs; δ = 10 %.

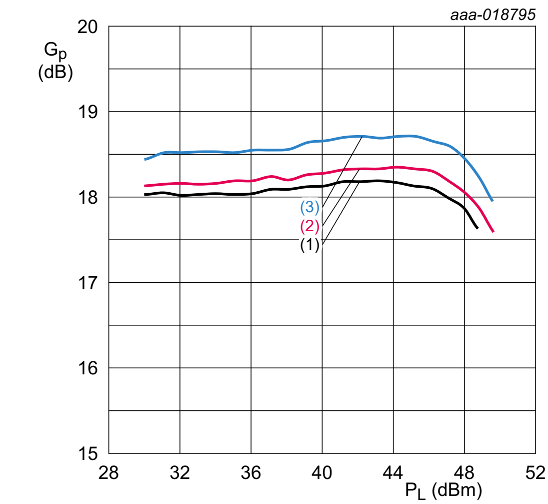
(1) f = 1805 MHz

(2) f = 1840 MHz

(3) f = 1880 MHz

Fig 5. Drain efficiency as a function of output power; typical values

7.5.2 IS-95



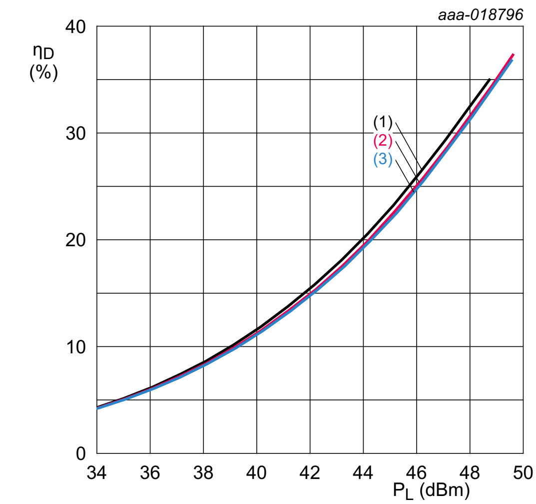
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 6. Power gain as a function of output power; typical values



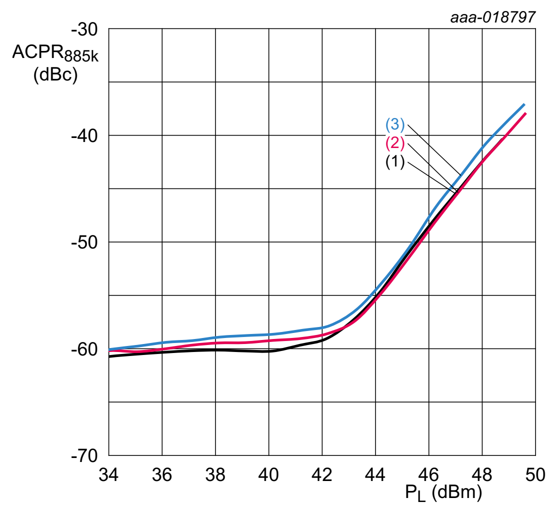
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 7. Drain efficiency as a function of output power; typical values



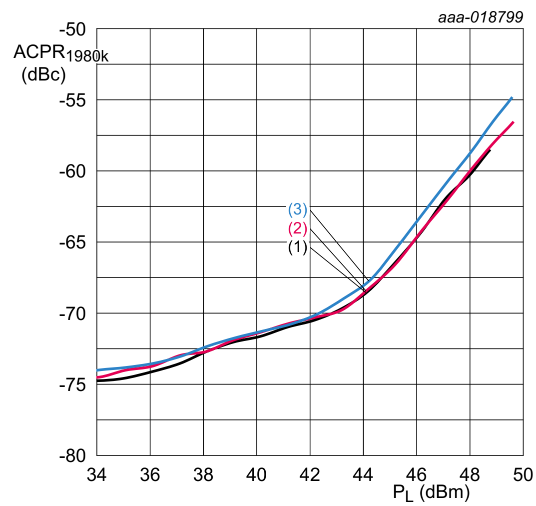
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 8. Adjacent channel power ratio (885 kHz) as a function of output power; typical values



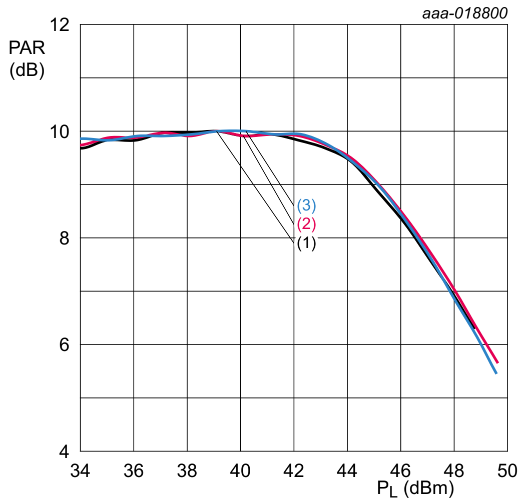
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 9. Adjacent channel power ratio (1980 kHz) as a function of output power; typical values



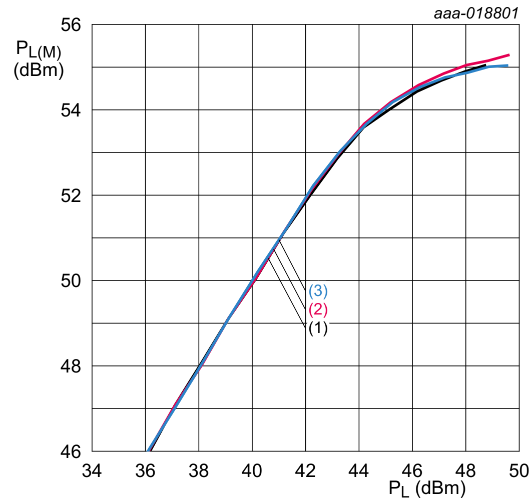
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 10. Peak-to-average ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA.

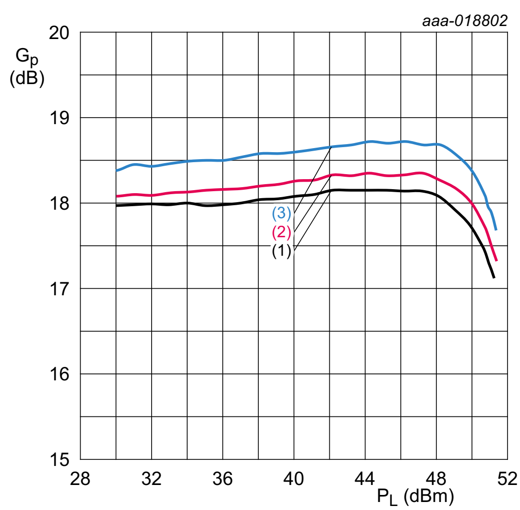
(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 11. Peak output power as a function of output power; typical values

7.5.3 1-Carrier W-CDMA



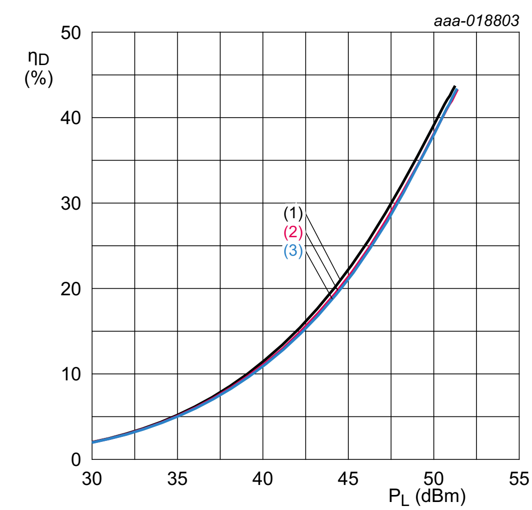
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 12. Power gain as a function of output power; typical values



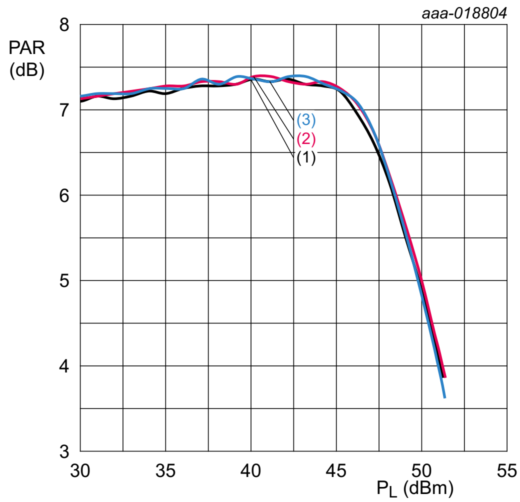
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 13. Drain efficiency as a function of output power; typical values



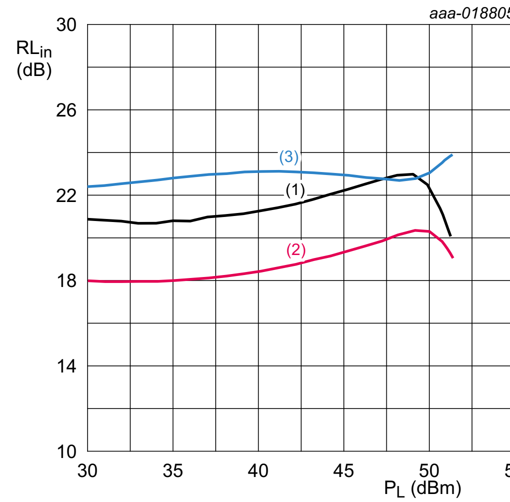
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 14. Peak-to-average ratio as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA.

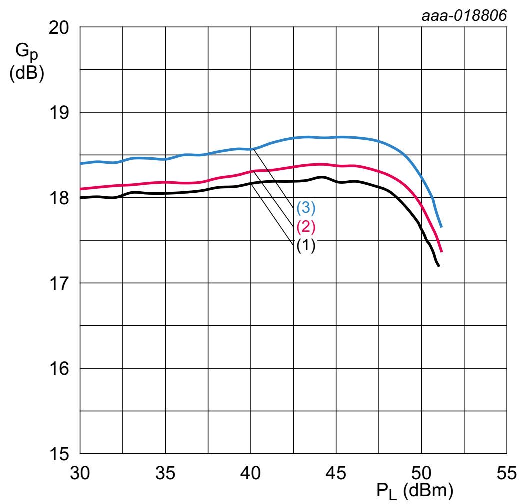
(1) f = 1807.5 MHz

(2) f = 1840 MHz

(3) f = 1877.5 MHz

Fig 15. Input return loss as a function of output power; typical values

7.5.4 2-Carrier W-CDMA



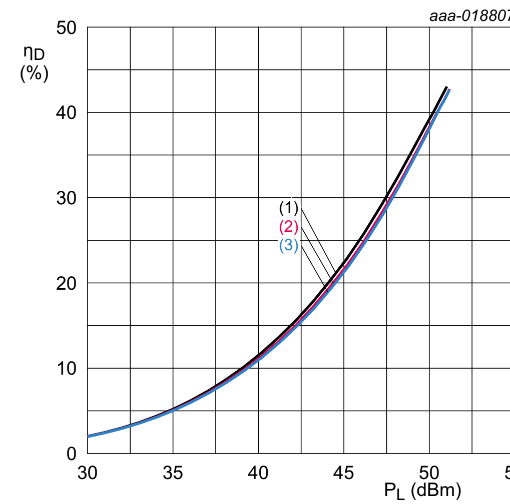
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 16. Power gain as a function of output power; typical values



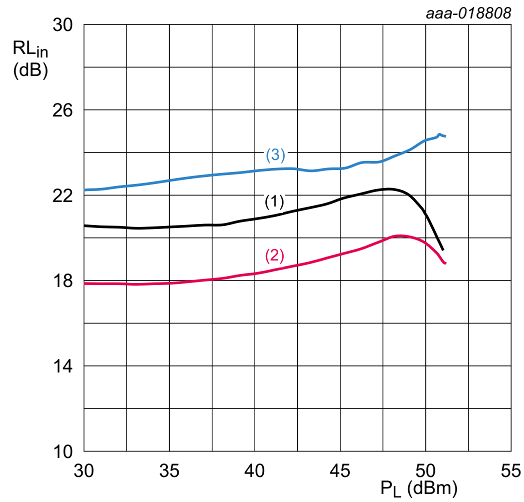
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 17. Drain efficiency as a function of output power; typical values



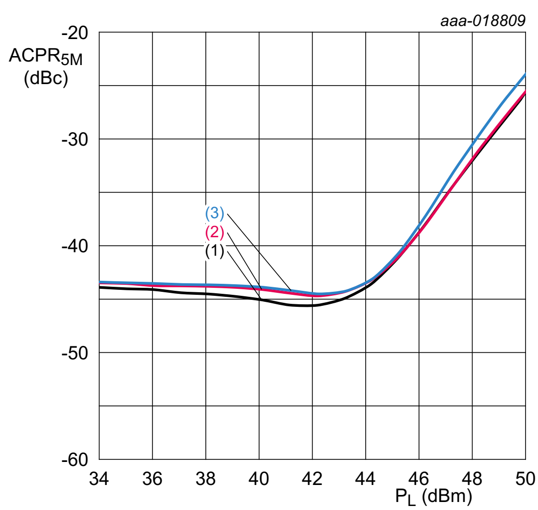
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 18. Input return loss as a function of output power; typical values



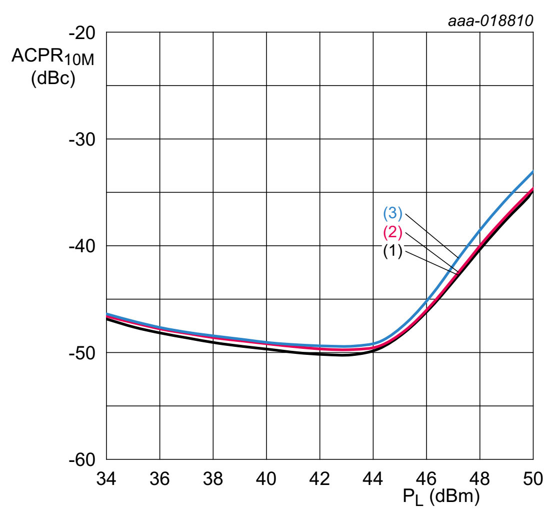
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 19. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1810 MHz

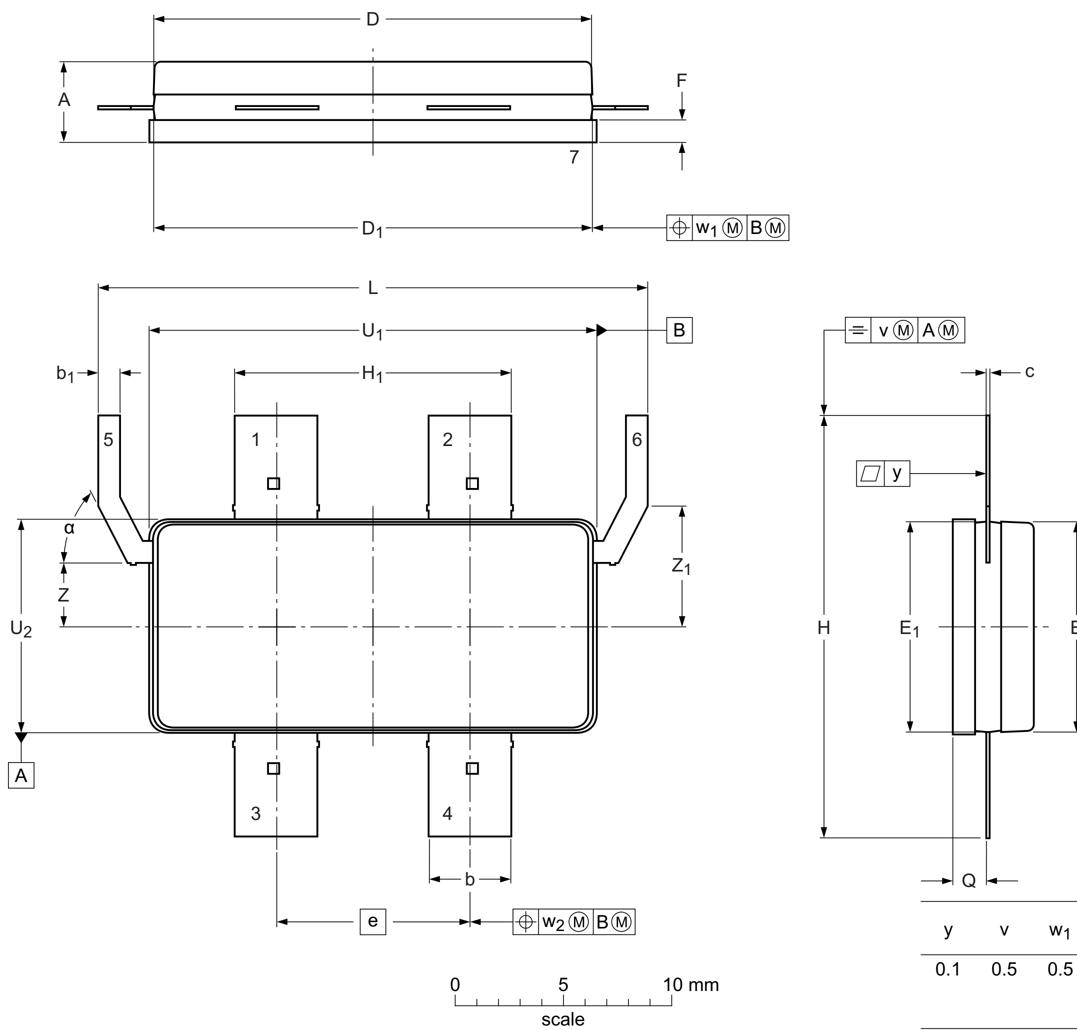
(2) f = 1840 MHz

(3) f = 1875 MHz

Fig 20. Adjacent channel power ratio (10 MHz) as a function of output power; typical values

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1275-1**



y	v	w1	w2
0.1	0.5	0.5	0.5

Dimensions

Unit		A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	L	Q(1)	U_1	U_2	Z	Z_1	α
mm	max	4.01	3.94	1.14	0.178	20.42	20.37	9.80	9.75		1.14	19.53	12.80	25.40	1.68	20.70	9.91	3.17	5.79	65°
	nom									8.89										
	min	3.40	3.68	0.89	0.127	20.12	20.17	9.50	9.55		0.94	19.33	12.60	25.20	1.45	20.50	9.70	2.67	5.29	61°

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1275-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1275-1						~~16-11-15~~ 17-04-13

Fig 21. Package outline SOT1275-1

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20LS-240PV v.4	20170524	Product data sheet	-	BLC9G20LS-240PV v.3
Modifications:	• Table 2 on page 2: change simplified outline • Table 3 on page 2: change version to SOT1275-1 • Figure 21 on page 11: change package outline drawing to SOT1275-1			
BLC9G20LS-240PV v.3	20161202	Product data sheet	-	BLC9G20LS-240PV v.2
BLC9G20LS-240PV v.2	20160219	Product data sheet	-	BLC9G20LS-240PV v.1
BLC9G20LS-240PV v.1	20151005	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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13. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

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