BLC9G20XS-400AVT

Power LDMOS transistor

Rev. 3 — 24 November 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

400 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1880 MHz and 1930 MHz to 1995 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty production test circuit. V_{DS} = 32 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 0.5 V, unless otherwise specified.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	32	87	16.2	45	–39 [1]

[1] Test signal: 1-carrier W-CDMA; 3GPP test model 1; 64 DPCH; PAR = 9.6 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

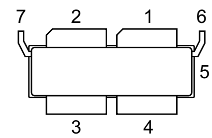
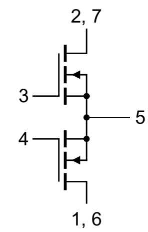
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1880 MHz and 1930 MHz to 1995 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		 aaa-014884
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source [1]		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20XS-400AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-4

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–6	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–6	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C
T_{case}	case temperature	operating [1]	–40	+125	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	V_{DS} = 32 V; I_{Dq} = 800 mA (main); $V_{GS(amp)peak}$ = 0,4 V; T_{case} = 80 °C		
		P_L = 85 W	0.25	K/W
		P_L = 110 W	0.26	K/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.62 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 162 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 850 mA	1.65	2.15	2.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	32	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 8.1 A	-	11.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 5.67 A	-	85	149	mΩ
Peak device						
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.0 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 300 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 32 V; I_D = 1500 mA	1.65	2.15	2.65	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 32 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V	-	52	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 15 A	-	20.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 10.5 A	-	46	85	mΩ

Table 7. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 1807.5 MHz; f_2 = 1877.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 850 mA (main); $V_{GS(amp)peak}$ = 0.9 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 87 W	15.2	16.2	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 87 W	-	−15	−10	dB
η_D	drain efficiency	$P_{L(AV)}$ = 87 W	41.5	45	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 87 W	-	−39	−34	dBc

Table 8. RF characteristics
Test signal: 1-carrier W-CDMA; PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f = 1877.5 MHz; RF performance at V_{DS} = 32 V; I_{Dq} = 850 mA (main); $V_{GS(amp)peak}$ = 0.9 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at a frequency of 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 120 W	6.25	6.8	-	dB
$P_{L(M)}$	peak output power	$P_{L(AV)}$ = 120 W	500	570	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC9G20XS-400AVT is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.9 V; f = 1807.5 MHz; P_L = 126 W (5 dB OBO); 100 % clipping.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f (MHz)	Z_S [1] (Ω)	Z_L [1] (Ω)	P_L [2] (W)	η_D [2] (%)	G_p [2] (dB)
Maximum power load					
1805	1.0 – j4.5	1.2 – j3.0	260	58.3	19.2
1840	1.2 – j4.8	1.2 – j3.1	260	58.4	19.4
1880	1.3 – j5.1	1.2 – j3.1	260	57.9	19.3
Maximum drain efficiency load					
1805	1.0 – j4.5	2.5 – j2.2	180	66.0	21.7
1840	1.1 – j4.8	2.0 – j2.5	200	65.4	21.3
1880	1.3 – j5.1	2.0 – j3.5	200	65.3	21.3

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1800 mA (peak); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	P_L [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum power load					
1805	1.7 – j6.0	1.7 – j3.2	430	56.4	18.9
1840	2.3 – j6.6	1.9 – j3.3	430	56.4	19.0
1880	3.1 – j7.1	1.9 – j3.2	430	56.4	19.1
Maximum drain efficiency load					
1805	1.7 – j6.0	2.7 – j2.9	380	63.8	20.0
1840	2.2 – j6.6	2.6 – j2.4	360	63.5	20.4
1880	3.1 – j7.2	2.6 – j2.3	360	63.7	20.5

[1] Z_S and Z_L defined in Figure 1.

[2] At 3 dB gain compression.

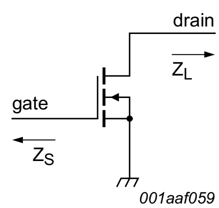


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main at 1 : 1 load

Measured load-pull data of main device; I_{Dq} = 800 mA (main); V_{DS} = 32 V; pulsed CW (t_p = 100 μs; δ = 10 %).

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1805	1.0 – j4.8	1.4 – j3.2	210	42.0	19.1
1840	1.1 – j5.0	1.4 – j2.9	210	42.3	19.3
1880	1.1 – j5.2	1.4 – j2.5	205	44.0	19.5

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 85 W.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; I_{Dq} *= 800 mA (main);* V_{DS} *= 32 V; pulsed CW (*t_p *= 100* μ*s;* δ *= 10 %).*

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1805	1.0 – j4.8	3.5 – j2.8	115	59.0	21.8
1840	1.1 – j5.0	3.4 – j2.6	110	58.0	22.0
1880	1.1 – j5.2	3.4 – j2.4	110	57.4	22.0

[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 85 W.

Table 13. Typical impedance of peak device at 1 : 1 load

Measured load-pull data of peak device; I_{Dq} *= 1750 mA (peak);* V_{DS} *= 32 V; pulsed CW (*t_p *= 100* μ*s;* δ *= 10 %).*

f	Z_S [1]	Z_L [1]	$P_{L(3dB)}$ [2]	η_D [2]	G_p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
1805	1.6 – j6.0	2.2 – j3.2	320	31.4	19.5
1840	2.1 – j6.5	2.1 – j2.9	320	31.5	19.6
1880	3.0 – j7.0	2.1 – j2.7	320	32.2	20.0

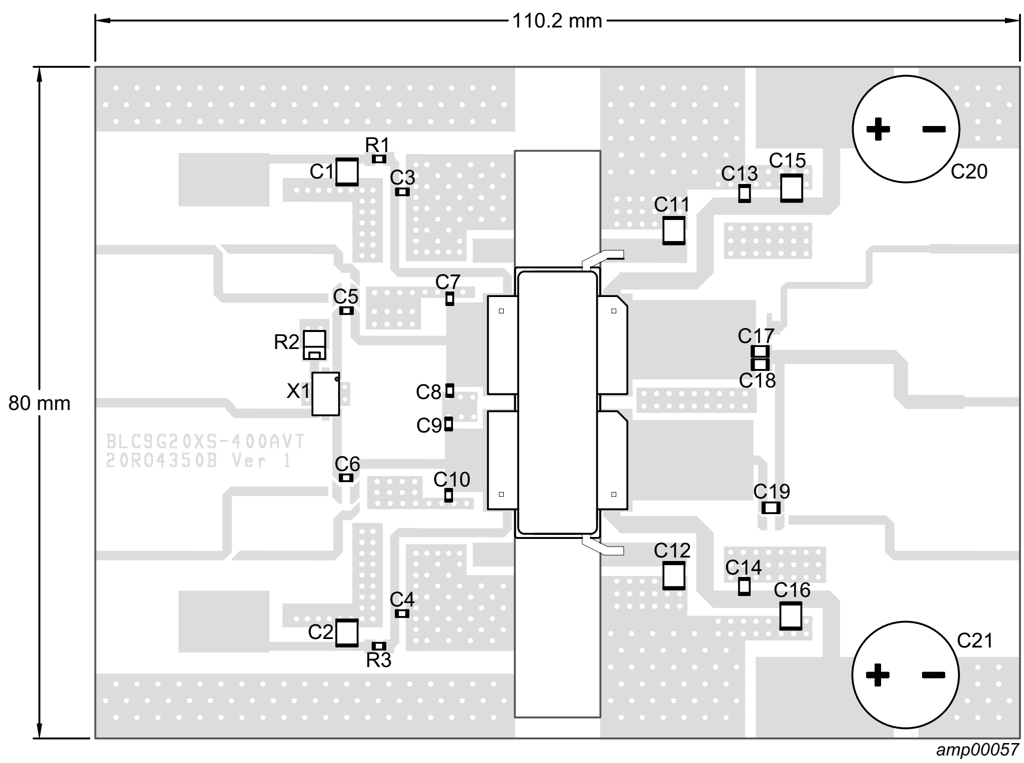
[1] Z_S and Z_L defined in Figure 1.

[2] At $P_{L(AV)}$ = 85 W.

Table 14. Off-state impedances of peak device

f	Z_{off}
(MHz)	(Ω)
1805	3.5 – j5.5
1840	1.4 – j2.9
1880	0.8 – j1.6

7.4 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B: ε_r = 3.66; thickness = 0.508 mm; thickness copper plating = 35 μm. See Table 15 for a list of components.

Fig 2. Component layout

Table 15. List of components

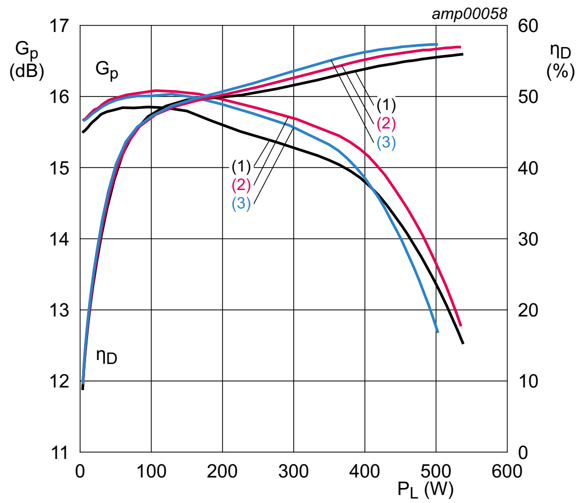
See Figure 2 for component layout.

Component	Description	Value	Remarks
C1, C2, C11, C12, C15, C16	multilayer ceramic chip capacitor	4.7 μF, 50 V [1]	Murata GRM32ER71H475KA88L
C3, C4, C5, C6, C13, C14 C19	multilayer ceramic chip capacitor	10 pF [1]	Murata Hi-Q 0805
C7	multilayer ceramic chip capacitor	3.0 pF [1]	Murata Hi-Q 0805
C8	multilayer ceramic chip capacitor	2.4 pF [1]	Murata Hi-Q 0805
C9	multilayer ceramic chip capacitor	1.5 pF [1]	Murata Hi-Q 0805
C10	multilayer ceramic chip capacitor	2.0 pF [1]	Murata Hi-Q 0805
(C17, C18)	multilayer ceramic chip capacitor	4.7 pF [1]	Murata Hi-Q 0805
C20, C21	electrolytic capacitor	100 μF	
R1, R2	SMD resistor	10 Ω, 1 %	SMD 0805
R3	SMD resistor	50 Ω, 25 W	Anaren C16A50Z4
X1	hybrid coupler	2 dB, 90°	Anaren Xinger III

[1] Murata or capacitor of same quality

7.5 Graphical data

7.5.1 Pulsed CW



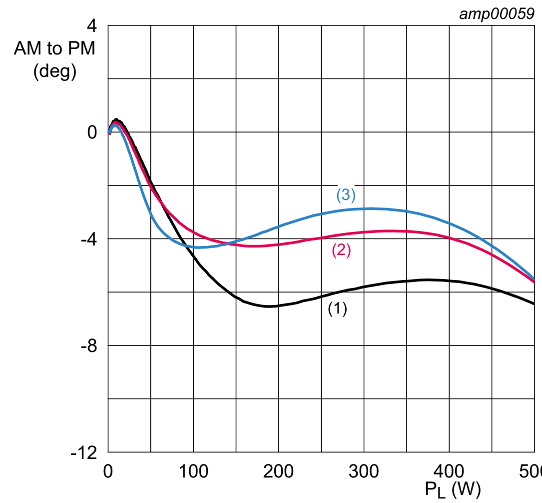
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V;
t_p = 100μs; δ = 10 %.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 3. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

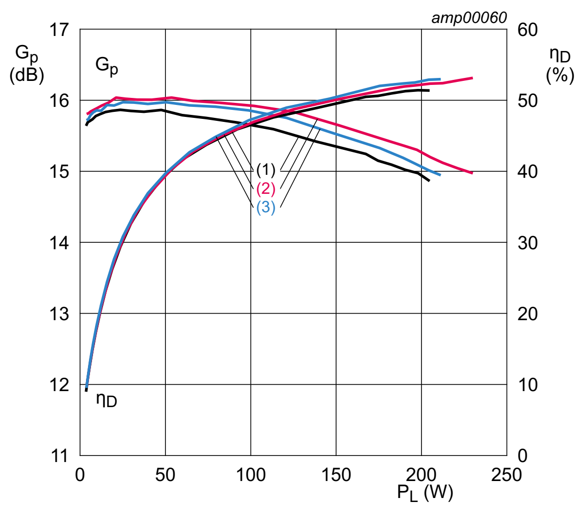
(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 4. AM to PM as a function of output power; typical values

7.5.2 1-Carrier W-CDMA

PAR = 9.6 dB per carrier at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (100 % clipping).



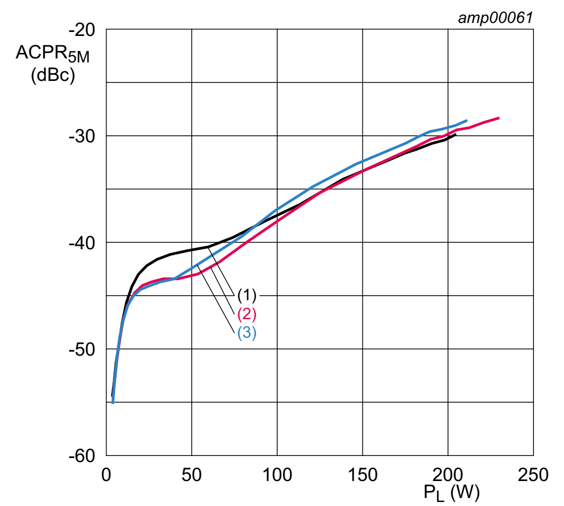
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



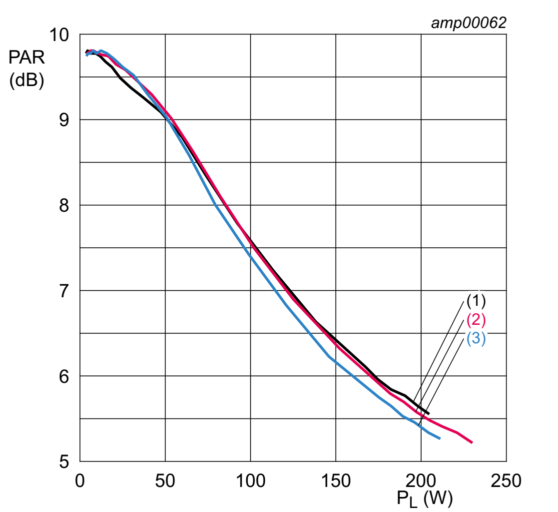
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



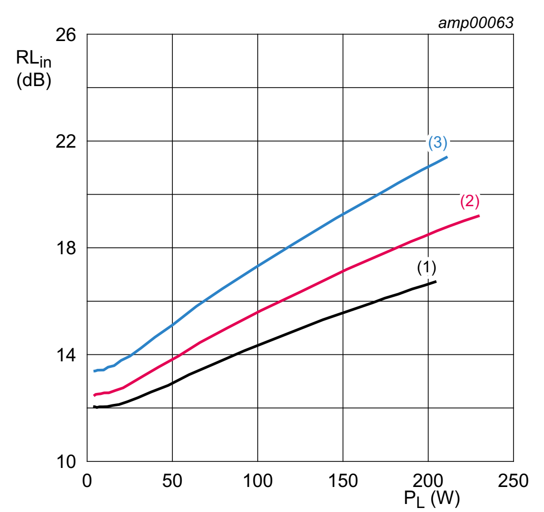
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 7. Peak-to-average power ratio as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

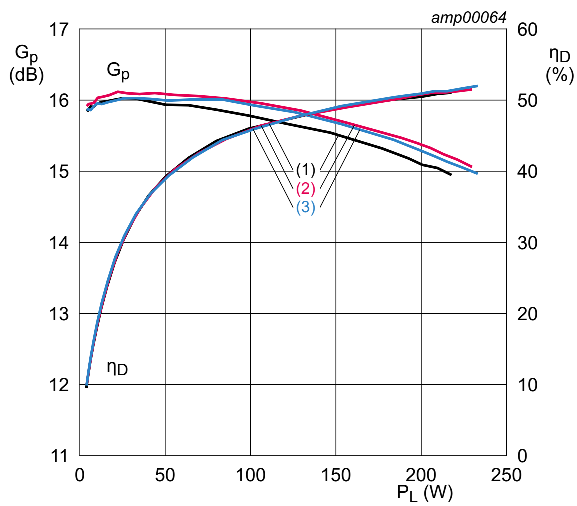
(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 8. Input return loss as a function of output power; typical values

7.5.3 2-Carrier W-CDMA

PAR = 9.6 dB at 0.01 % probability on the CCDF; 3GPP test model 1 with 64 DPCH (46 % clipping).



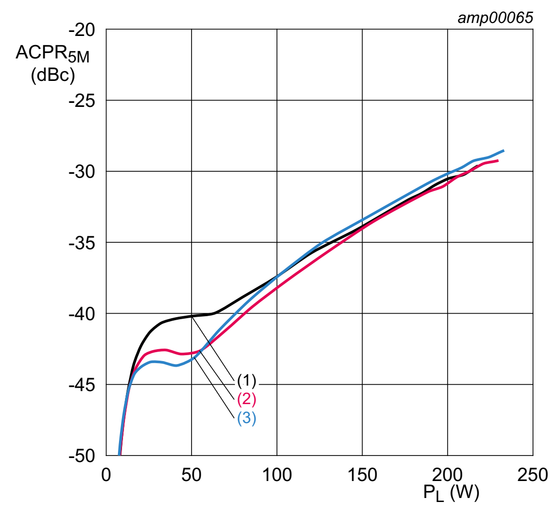
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 9. Power gain and drain efficiency as function of output power; typical values



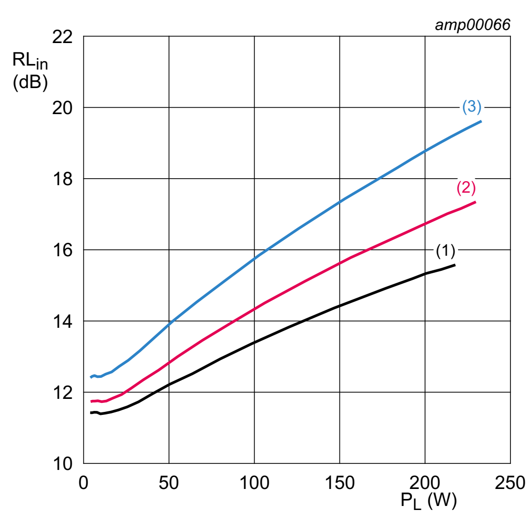
V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 10. Adjacent channel power ratio (5 MHz) as a function of output power; typical values



V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

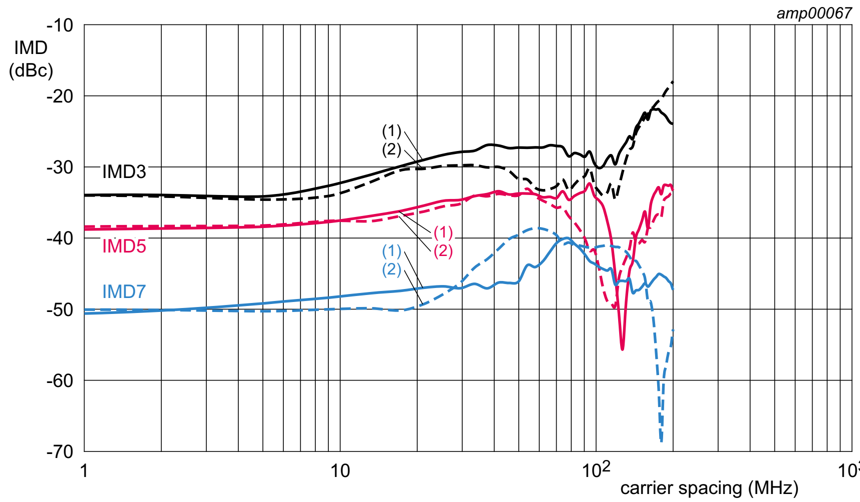
(1) f = 1807.5 MHz

(2) f = 1842.5 MHz

(3) f = 1877.5 MHz

Fig 11. Input return loss as a function of output power; typical values

7.5.4 2-Tone VBW



V_{DS} = 32 V; I_{Dq} = 850 mA; $V_{GS(amp)peak}$ = 0.6 V.

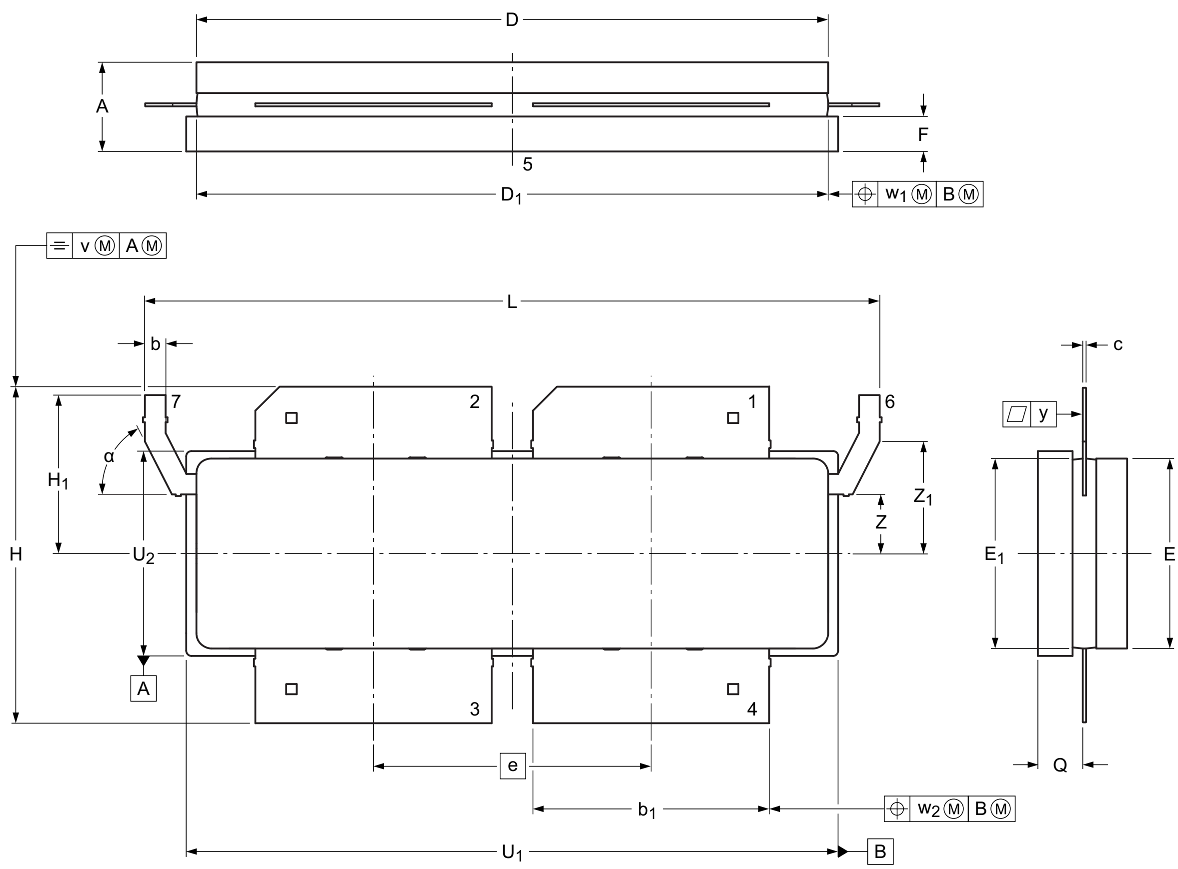
(1) IMD low

(2) IMD high

Fig 12. VBW capability

8. Package outline

Air cavity plastic earless flanged package; 6 leads **SOT1258-4**



y	α	Z	Z1
0.1	65°	3.17	5.79
	61°	2.67	5.29

Dimensions

Unit		A	b	b1	c	D	D1	E	E1	e	L	F	H	H1	Q(1)	U1	U2	v	w1	w2
mm	max	4.52	1.12	11.78	0.18	31.44	31.34	9.60	9.50		36.42	1.73	16.71	8.12	2.25	32.33	10.23	0.5	0.5	0.5
	nom									13.72										
	min	4.12	0.91	11.58	0.13	31.04	31.14	9.20	9.30		36.22	1.53	16.51	7.62	2.03	32.13	10.03			

Note
1. Dimension Q is measured 0.1 mm away from the flange.
2. Ringframe and/or ringframe glue shall not overhang at the side of the flange.

sot1258-4_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1258-4						17-08-31

Fig 13. Package outline SOT1258-4

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 16. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 17. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
AM	Amplitude Modulation
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OBO	Output Back Off
PAR	Peak-to-Average Ratio
PM	Phase Modulation
SMD	Surface Mounted device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20XS-400AVT v.3	20171124	Product data sheet	-	BLC9G20XS-400AVT v.2
Modifications:	• Table 2 on page 2: changed simplified version drawing SOT1258-7 to SOT1258-4 • Table 3 on page 2: changed version SOT1258-7 to SOT1258-4 • Figure 13 on page 12: changed package outline drawing SOT1258-7 to SOT1258-4			
BLC9G20XS-400AVT v.2	20161202	Product data sheet	-	BLC9G20XS-400AVT v.1
BLC9G20XS-400AVT v.1	20160513	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Ampleon does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

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13. Contact information

For more information, please visit: **http://www.ampleon.com**

For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

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