BLD6G22L-50; BLD6G22LS-50

W-CDMA 2110 MHz to 2170 MHz fully integrated Doherty transistor

Rev. 3 — 17 August 2010 Product data sheet

1. Product profile

1.1 General description

The BLD6G22L-50 and BLD22LS-50 incorporate a fully integrated Doherty solution using NXP's state of the art GEN6 LDMOS technology. This device is perfectly suited for CDMA base station applications at frequencies from 2110 MHz to 2170 MHz. The main and peak device, input splitter and output combiner are integrated in a single package. This package consists of one gate and drain lead and two extra leads of which one is used for biasing the peak amplifier and the other is not connected. It only requires the proper input/output match and bias setting as with a normal class-AB transistor.

Table 1. Typical performance

RF performance at T_h = 25 °C.

Mode of operation	f (MHz)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR (dBc)	$P_{L(3dB)}$ (W)
W-CDMA [1][2]	2110 to 2170	28	8	14	40	–30	55

[1] Test signal: 2-carrier W-CDMA; test model 1; 64 DPCH; PAR = 8.3 dB at 0.01 % probability on CCDF; carrier spacing 5 MHz.

[2] I_{Dq} = 170 mA (main); $V_{GS(amp)peak}$ = 0 V.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical W-CDMA performance at frequencies from 2110 MHz to 2170 MHz:
  - Average output power = 8 W
  - Power gain = 14 dB
  - Efficiency = 40 %
- Fully optimized integrated Doherty concept:
  - integrated asymmetrical power splitter at input
  - integrated power combiner
  - peak biasing down to 0 V
  - low junction temperature
  - high efficiency

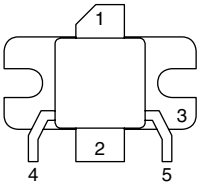
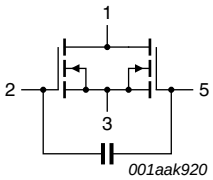
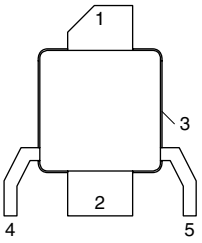
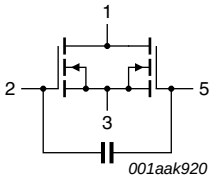
- 100 % peak power tested for guaranteed output power capability
- Integrated ESD protection
- Good pair match (main and peak on the same chip)
- Independent control of main and peak bias
- Internally matched for ease of use
- Excellent ruggedness
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- High efficiency RF power amplifiers with digital pre-distortion for W-CDMA multi carrier applications in the 2110 MHz to 2170 MHz range.

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLD6G22L-50 (SOT1130A)				
1	drain			
2	gate + bias main			
3	source	[1]		
4	n.c.			
5	bias peak			
BLD6G22LS-50 (SOT1130B)				
1	drain			
2	gate + bias main			
3	source	[1]		
4	n.c.			
5	bias peak			

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLD6G22L-50	-	flanged ceramic package; 2 mounting holes; 4 leads	SOT1130A
BLD6G22LS-50	-	earless flanged ceramic package; 4 leads	SOT1130B

4. Block diagram

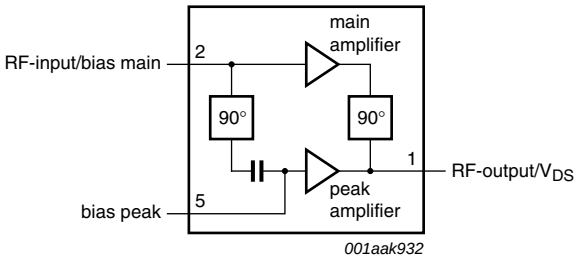


Fig 1. Block diagram of BLD6G22L-50 and BLD6G22LS-50

5. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).
Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		–0.5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		–0.5	+13	V
I_D	drain current		-	10.2	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	200	°C

6. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 8 W	[1]	1.9	K/W

[1] When operated with a 2-carrier (W-CDMA) modulated signal with PAR = 8.3 dB at 0.01 % probability on the CCDF.

7. Characteristics

Table 6. Characteristics

Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.62 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 31 mA	1.4	1.8	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 170 mA	1.55	2.05	2.55	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	1.4	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	4.95	5.5	-	A

Table 6. Characteristics *...continued*

Valid for both main and peak device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 1.55 A	1.4	2.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 1.085 A	-	0.52	0.736	Ω

8. Application information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 8.3 dB at 0.01 % probability on CCDF; carrier spacing = 5 MHz; f = 2140 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 170 mA; $V_{GS(amp)peak}$ = 0 V; T_{case} = 25 °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	8	-	W
G_p	power gain	$P_{L(AV)}$ = 8 W	12.5	14	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 8 W	37	40	-	%
PAR_O	output peak-to-average ratio	$P_{L(AV)}$ = 8 W	-	7.6	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 8 W	10	17	-	dB
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 8 W	-	–30	–24	dBc

Table 8. Application information

Mode of operation: Pulsed CW; δ = 10 %; t_p = 100 μs; RF performance at V_{DS} = 28 V; I_{Dq} = 170 mA; $V_{GS(amp)peak}$ = 0 V; T_{case} = 25 °C; unless otherwise specified; in a production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(3dB)}$	output power at 3 dB gain compression		46	55	-	W

8.1 Ruggedness in Doherty operation

The BLD6G22L-50 and BLD6G22LS-50 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 170 mA; P_L = 8 W (W-CDMA); f = 2140 MHz.

8.2 Impedance information

Table 9. Typical impedance

Measured load-pull data; typical values unless otherwise specified.

f	Z_S	Z_L
MHz	Ω	Ω
2050	9.4 – 12.3j	5.5 – 7.6j
2110	11.4 – 11.2j	6.7 – 8.2j
2140	12.3 – 10.5j	7.0 – 7.5j
2170	12.2 – 9.3j	7.2 – 6.8j
2230	11.8 – 7.3j	5.4 – 5.5j

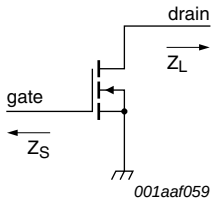
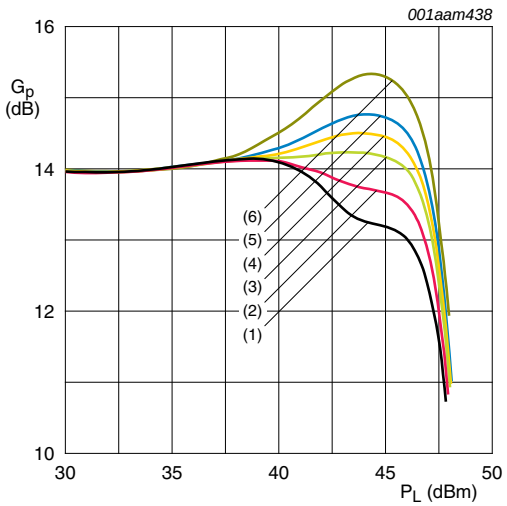


Fig 2. Definition of transistor impedance

8.3 Performance curves

Performance curves are measured in a BLD6G22L-50 application circuit.

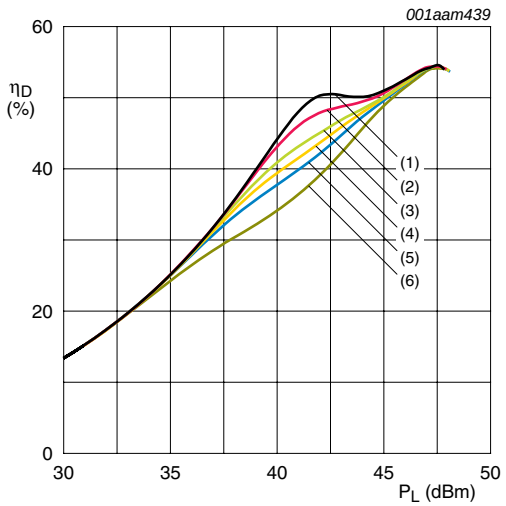
8.3.1 CW pulsed



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C;
f = 2140 MHz; δ = 10 %; t_p = 100 µs on 1 ms period.

(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

Fig 3. Power gain as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C;
f = 2140 MHz; δ = 10 %; t_p = 100 µs on 1 ms period.

(1) $V_{GS(amp)peak}$ = 0 V
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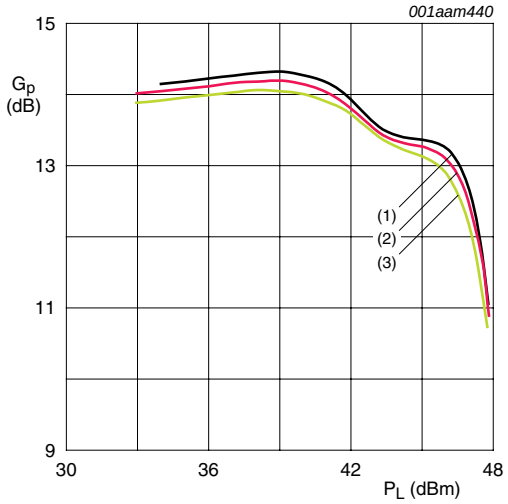
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

Fig 4. Drain efficiency as a function of load power; typical values



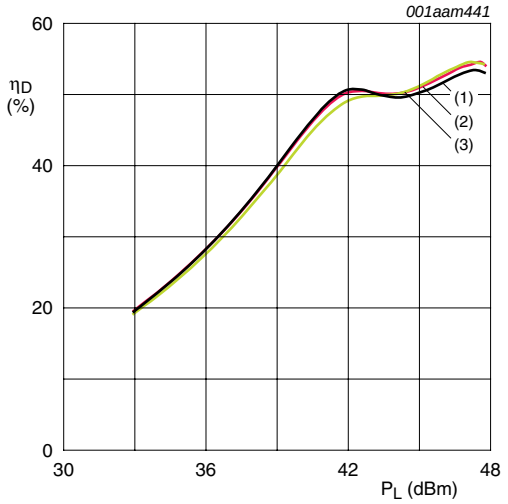
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 µs on 1 ms period.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 5. Power gain as a function of load power; typical values



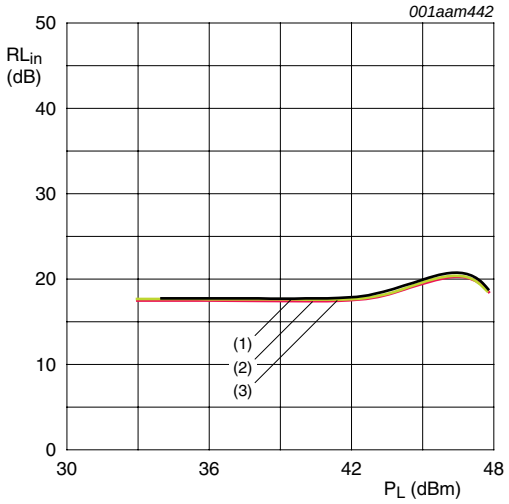
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 µs on 1 ms period.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 6. Drain efficiency as a function of load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; δ = 10 %; t_p = 100 µs on 1 ms period.

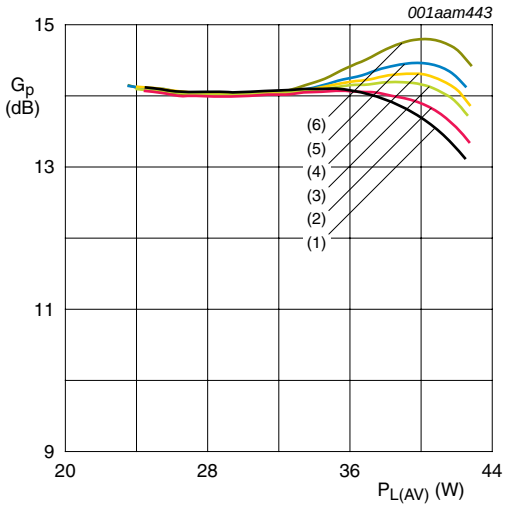
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 7. Input return loss as a function of load power; typical values

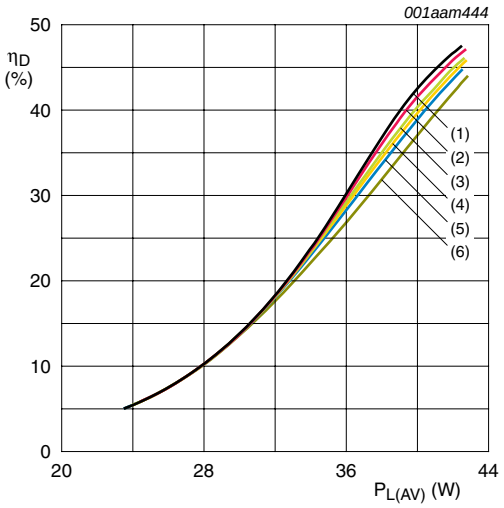
8.3.2 W-CDMA



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

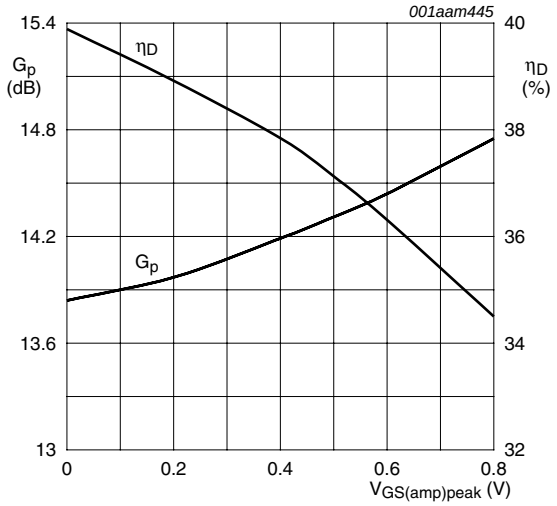
Fig 8. Power gain as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

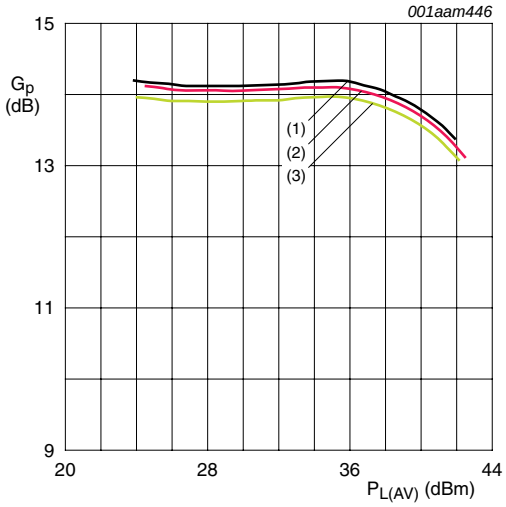
(1) $V_{GS(amp)peak}$ = 0 V
(2) $V_{GS(amp)peak}$ = 0.2 V
(3) $V_{GS(amp)peak}$ = 0.4 V
(4) $V_{GS(amp)peak}$ = 0.5 V
(5) $V_{GS(amp)peak}$ = 0.6 V
(6) $V_{GS(amp)peak}$ = 0.8 V

Fig 9. Drain efficiency as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; f = 2140 MHz; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

Fig 10. Power gain and drain efficiency as function of load power; typical values



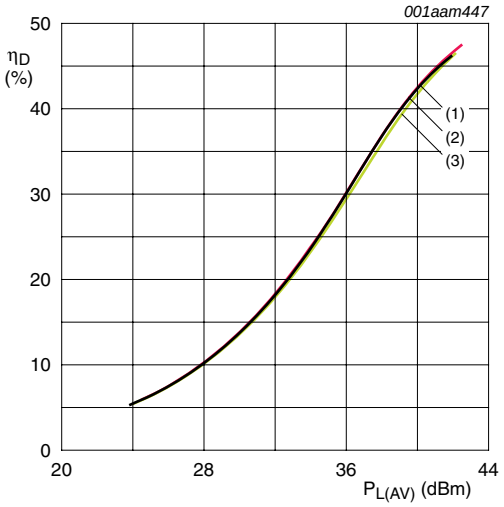
V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 11. Power gain as a function of average load power; typical values



V_{DS} = 28 V; I_{Dq} = 170 mA (main); T_{case} = 25 °C; $V_{GS(amp)peak}$ = 0 V; 2-carrier W-CDMA; PAR = 8.3 dB at 0.01 % probability on CCDF.

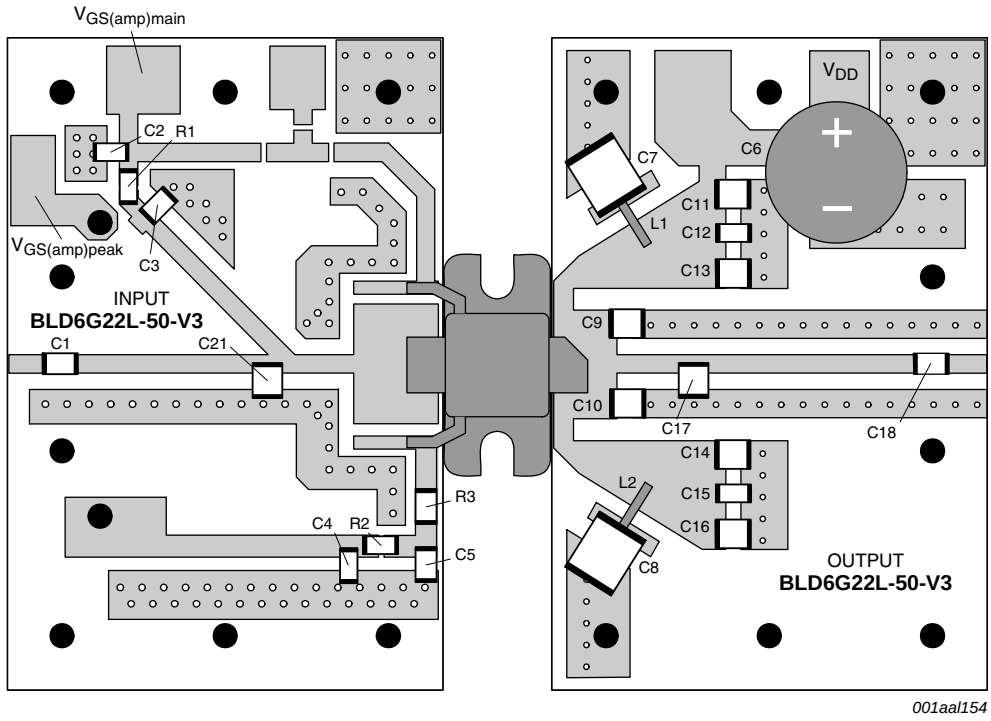
(1) f = 2110 MHz

(2) f = 2140 MHz

(3) f = 2170 MHz

Fig 12. Drain efficiency as a function of average load power; typical values

9. Test information



The striplines are on a double copper-clad gold plated Rogers 4350B Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm.

See Table 10 for list of components.

Fig 13. Component layout

Table 10. List of components

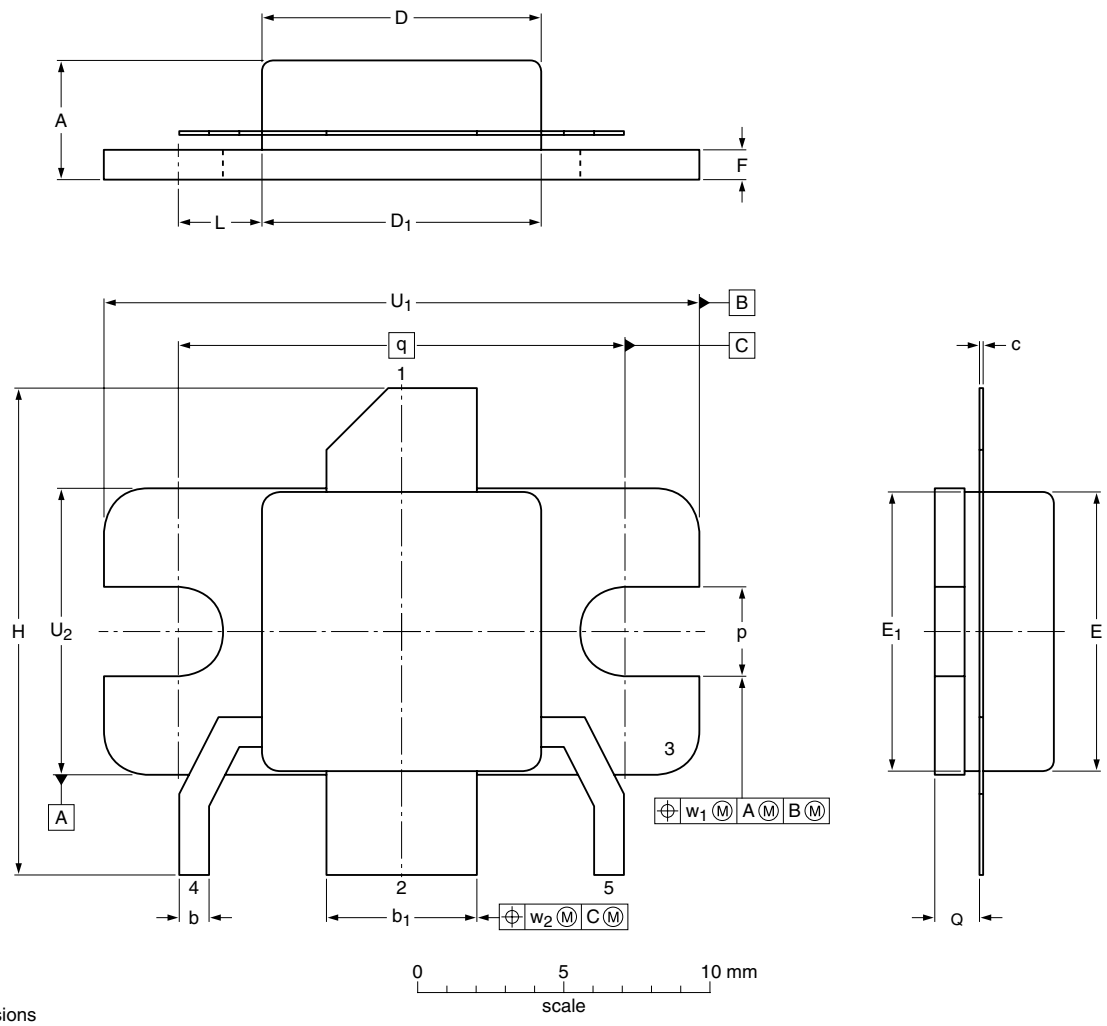
See Figure 13 for component layout.

Component	Description	Value		Dimensions
C1, C3, C5, C18	multilayer ceramic chip capacitor	9.1 pF	[1]	
C2, C4, C12, C15	multilayer ceramic chip capacitor	100 nF		
C6	electrolytic capacitor	470 µF; 63 V		
C7, C8	multilayer ceramic chip capacitor	10 µF		
C9, C10	multilayer ceramic chip capacitor	1.2 pF	[1]	
C11, C13, C14, C16	multilayer ceramic chip capacitor	8.2 pF	[1]	
C17	multilayer ceramic chip capacitor	0.8 pF	[1]	
C21	multilayer ceramic chip capacitor	1.0 pF	[1]	
L1, L2	copper wire	-		diameter = 0.8 mm; length = 8 mm
R1	SMD resistor	3.6 Ω		1206
R2	SMD resistor	33 Ω		1206
R3	SMD resistor	10 Ω		1206

[1] American Technical Ceramics type 100B or capacitor of same quality.

10. Package outline

Flanged ceramic package; 2 mounting holes; 4 leads **SOT1130A**



Dimensions

Unit[1]		A	b	b_1	c	D	D_1	E	E_1	F	H	L	p	Q[2]	q	U_1	U_2	w_1	w_2
mm	max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	3.30	1.70		20.45	9.91		
	nom														15.24			0.25	0.51
	min	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	2.92	1.45		20.19	9.65		
inches	max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.130	0.067		0.805	0.39		
	nom														0.6			0.01	0.02
	min	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.115	0.057		0.795	0.38		

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1130a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1130A						~~09-10-12~~ 10-02-02

Fig 14. Package outline SOT1130A

分销商库存信息:		
NXP		
BLD6G22LS-50,112		