BLF10M6135; BLF10M6LS135

Power LDMOS transistor

Rev. 1 — 24 June 2014 Product data sheet

1. Product profile

1.1 General description

135 W LDMOS power transistor for industrial applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in a class-AB production test circuit.

Test signal	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
2-carrier W-CDMA	869 to 894	28	26.5	21.0	28.0	–39[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

1.2 Features and benefits

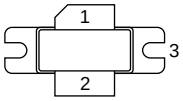
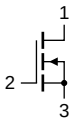
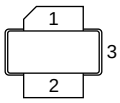
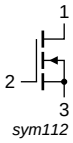
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

- RF power amplifiers for ISM applications in the 700 MHz to 1000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF10M6135 (SOT502A)			
1	drain		
2	gate		
3	source [1]		
BLF10M6LS135 (SOT502B)			
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF10M6135	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF10M6LS135	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Type	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 25 W	BLF10M6135	0.68	K/W
			BLF10M6LS135	0.56	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.8 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 180 mA	1.4	1.9	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 950 mA	1.6	2.1	2.6	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	3	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	24	32	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	300	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 9 A	7	13	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 6.3 A	-	0.1	-	Ω

Table 7. AC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	2.0	-	pF

Table 8. RF characteristics

Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH; f_1 = 871.5 MHz; f_2 = 876.5 MHz; f_3 = 886.5 MHz; f_4 = 891.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 950 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

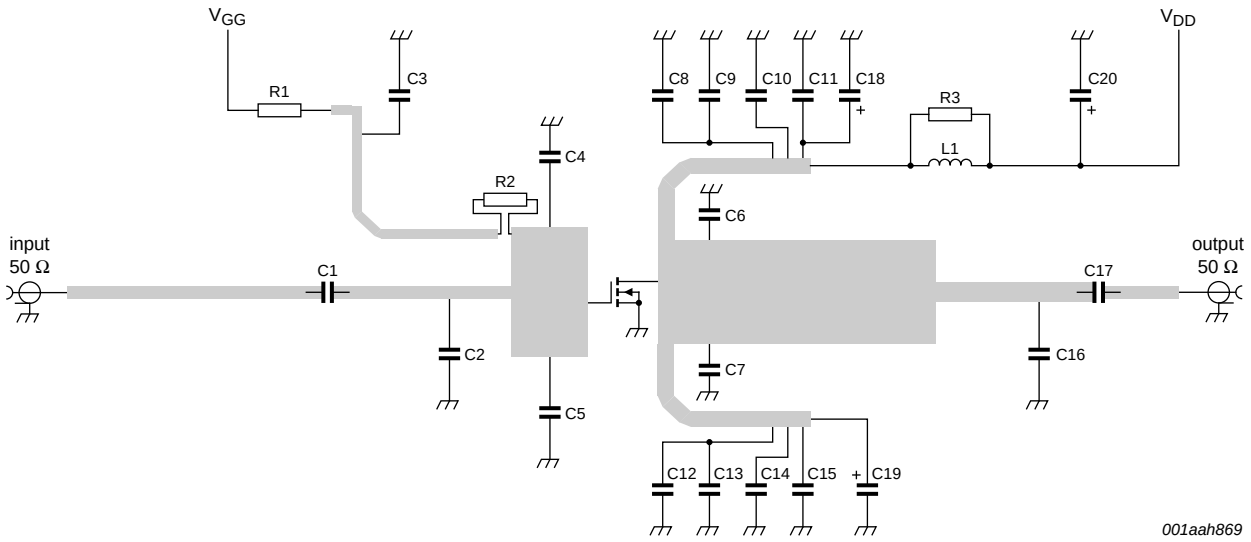
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 26.5 W	20.0	21.0	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 26.5 W	-	–10.0	–6.5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 26.5 W	26.0	28.0	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 26.5 W	-	–39	–36.5	dBc

7. Test information

7.1 Ruggedness in class-AB operation

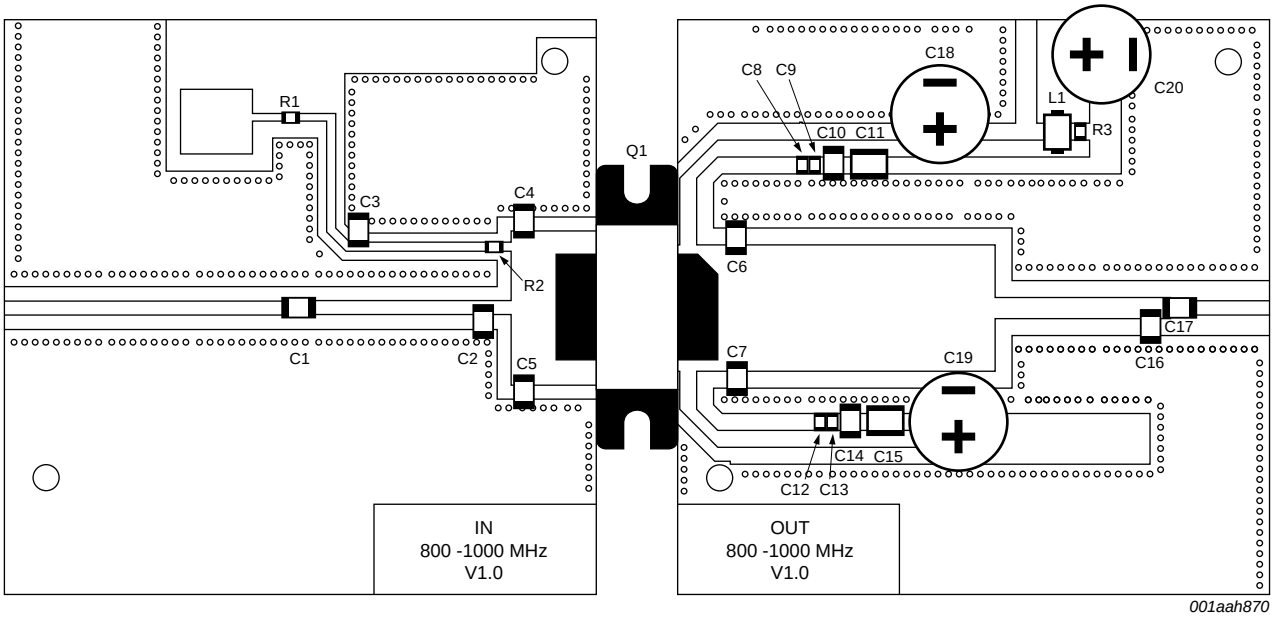
The BLF10M6135 and BLF10M6LS135 are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 950 mA; P_L = 135 W; f = 894 MHz.

7.2 Test circuit information



The drawing is not to scale.

Fig 1. Test circuit for operation at 800 MHz



The striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm.

See Table 9 for list of components.

The drawing is not to scale.

Fig 2. Component layout

Table 9. List of components

See Figure 1 and Figure 2.

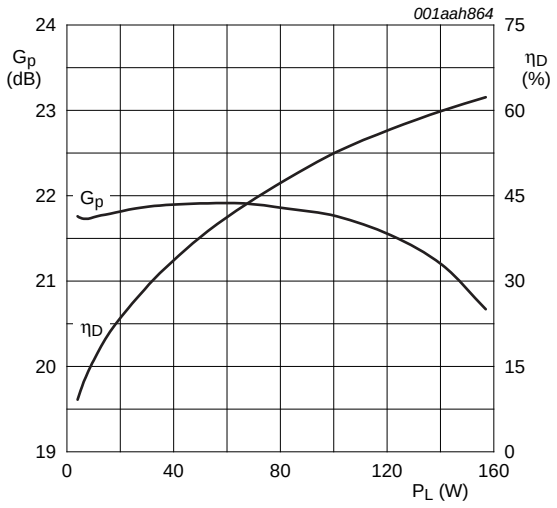
Component	Description	Value	Remarks
C1, C3, C10, C14, C17	multilayer ceramic chip capacitor	68 pF [1]	solder vertically
C2, C4, C5	multilayer ceramic chip capacitor	8.2 pF [1]	solder vertically
C6, C7	multilayer ceramic chip capacitor	10 pF [1]	solder vertically
C8, C9, C12, C13	electrolytic capacitor	100 nF	Vishay or capacitor of same quality
C11, C15	multilayer ceramic chip capacitor	4.7 μF, 50 V [2]	
C16	multilayer ceramic chip capacitor	3.0 pF [1]	solder vertically
C18, C19, C20	electrolytic capacitor	220 μF, 63 V	
L1	ferrite SMD bead		Ferroxcube BDS 3/3/4.6-4S2 or equivalent
Q1	BLF10M6135		
R1, R2, R3	SMD resistor	9.1 Ω, 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] TDK or capacitor of same quality.

7.3 Graphical data

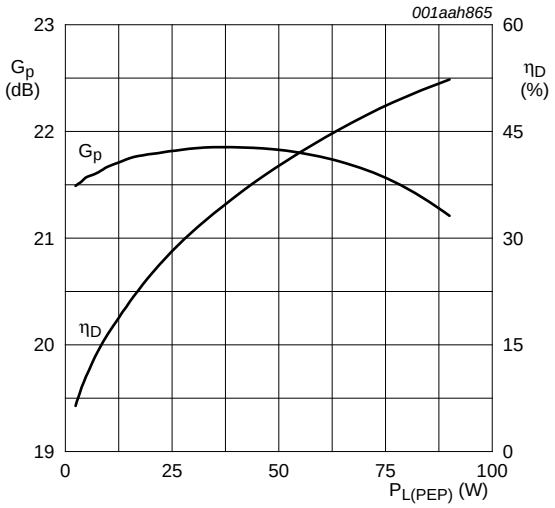
7.3.1 1-Tone CW



V_{DS} = 28 V; I_{Dq} = 950 mA; f = 881 MHz.

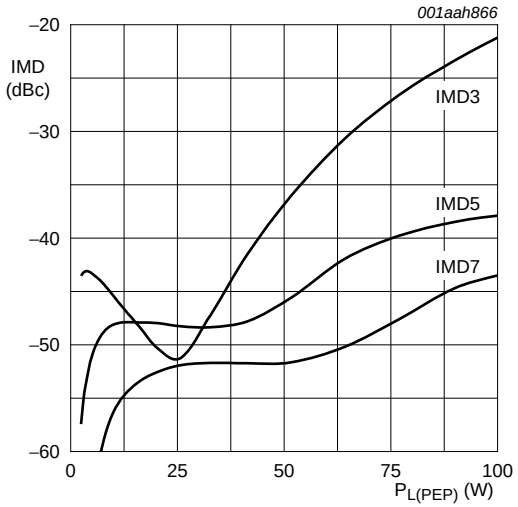
Fig 3. Power gain and drain efficiency as function of output power; typical values

7.3.2 2-Tone CW



V_{DS} = 28 V; I_{Dq} = 950 mA; f = 881 MHz (± 100 kHz).

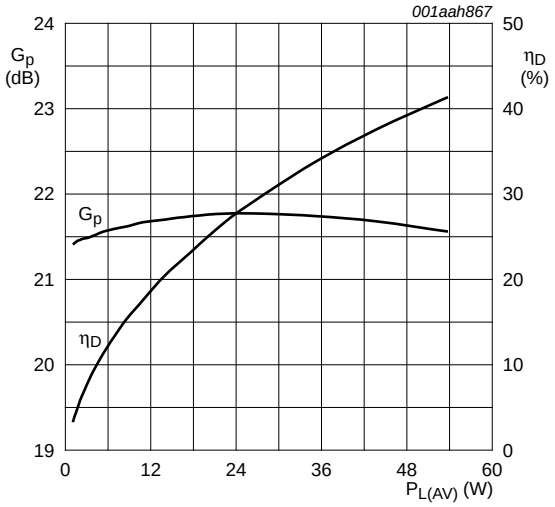
Fig 4. Power gain and drain efficiency as function of peak envelope power load power; typical values



V_{DS} = 28 V; I_{Dq} = 950 mA; f = 881 MHz (± 100 kHz).

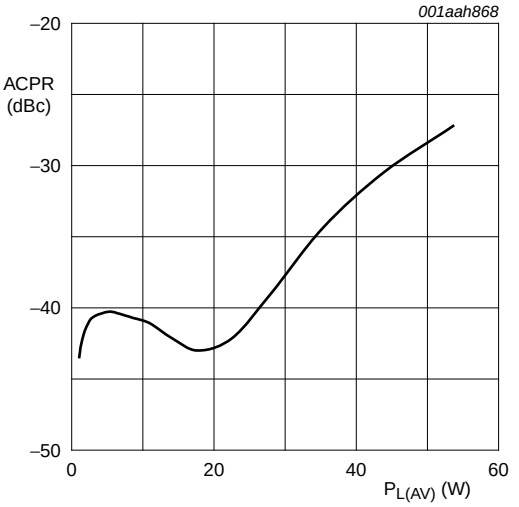
Fig 5. Intermodulation distortion as a function of peak envelope power load power; typical values

7.3.3 2-Carrier W-CDMA



V_{DS} = 28 V; I_{Dq} = 950 mA; f_1 = 881 MHz; f_2 = 886 MHz; carrier spacing 5 MHz.

Fig 6. Power gain and drain efficiency as function of average output power; typical values

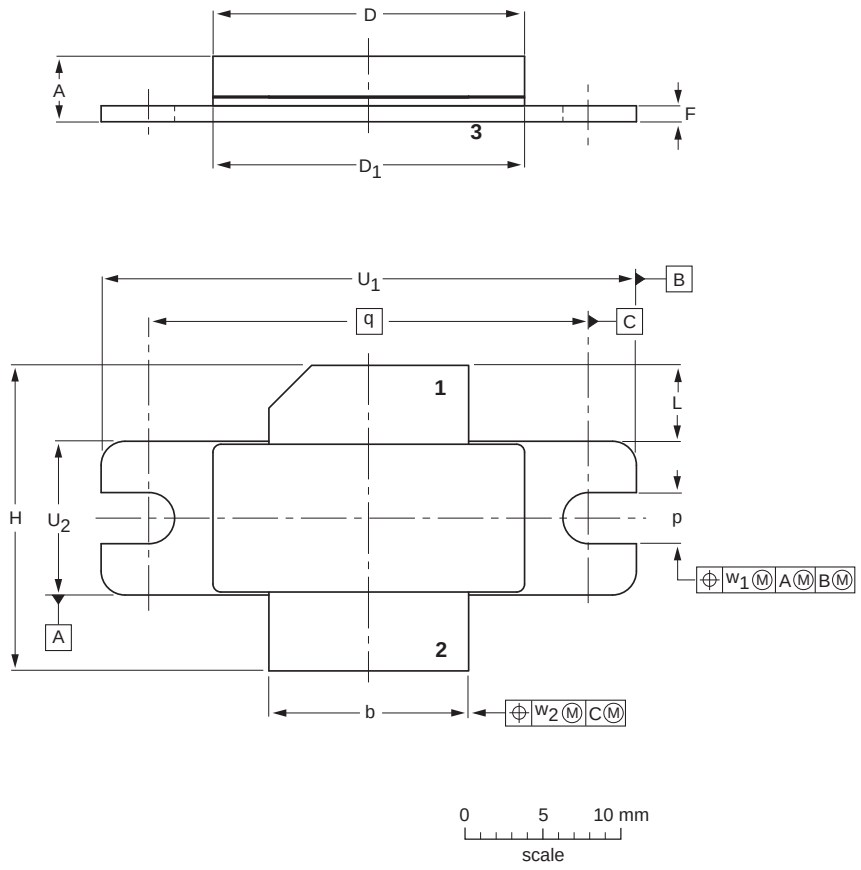


V_{DS} = 28 V; I_{Dq} = 950 mA; f_1 = 881 MHz; f_2 = 886 MHz; carrier spacing 5 MHz.

Fig 7. Adjacent power channel ratio as a function of average output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT502A**



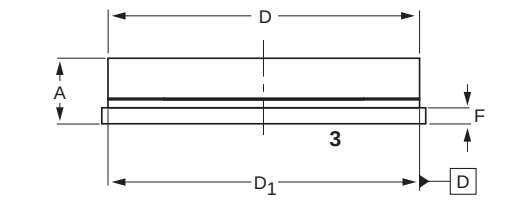
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

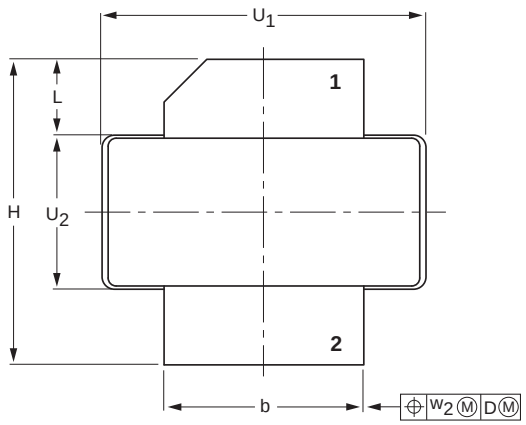
UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

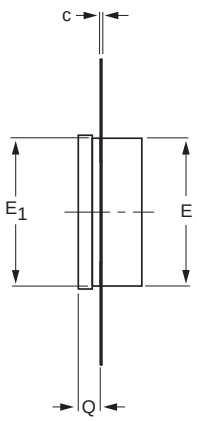
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502A						~~03-01-10~~ 12-05-02

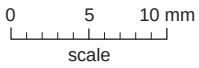
Fig 8. Package outline SOT502A

Earless flanged ceramic package; 2 leads **SOT502B**









DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 9. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF10M6135_BLF10M6LS135 v.1	20140624	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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