

# BLF10M6160; BLF10M6LS160

Power LDMOS transistor

Rev. 1 — 24 June 2014

Product data sheet

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for industrial applications at frequencies from 700 MHz to 1000 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a class-AB production test circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L(AV)</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	ACPR (dBc)
2-carrier W-CDMA	920 to 960	32	32	22.5	27	-41 <sup>[1]</sup>

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

### 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

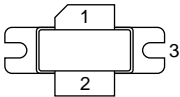
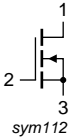
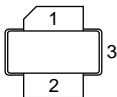
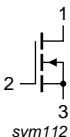
### 1.3 Applications

- RF power amplifiers for ISM applications in the 700 MHz to 1000 MHz frequency range



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF10M6160 (SOT502A)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		
<b>BLF10M6LS160 (SOT502B)</b>			
1	drain		 sym112
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF10M6160	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF10M6LS160	-	earless flanged ceramic package; 2 leads	SOT502B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect reliability.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Type	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 32\text{ W}$	BLF10M6160	0.5	K/W
			BLF10M6LS160	0.44	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.72\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 216\text{ mA}$	1.4	1.9	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 32\text{ V}; I_D = 1300\text{ mA}$	1.7	2.2	2.7	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	5	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	30.6	39	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 13\text{ V}; V_{DS} = 0\text{ V}$	-	-	450	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.5\text{ A}$	-	13.5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 6.3\text{ A}$	-	0.1	-	$\Omega$

**Table 7. AC characteristics**

$T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}; f = 1\text{ MHz}$	-	4.2	-	pF

**Table 8. RF characteristics**

Test signal: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 DPCH;  $f_1 = 922.5\text{ MHz}; f_2 = 927.5\text{ MHz}; f_3 = 952.5\text{ MHz}; f_4 = 957.5\text{ MHz}$ ; RF performance at  $V_{DS} = 32\text{ V}; I_{Dq} = 1200\text{ mA}; T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 32\text{ W}$	21	22.5	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 32\text{ W}$	-	-8	-5.5	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 32\text{ W}$	25	27	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 32\text{ W}$	-	-41	-38	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF10M6160 and BLF10M6LS160 are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 32\text{ V}; I_{Dq} = 1200\text{ mA}; P_L = 160\text{ W (CW)}; f = 960\text{ MHz}$ .

## 7.2 Test circuit information

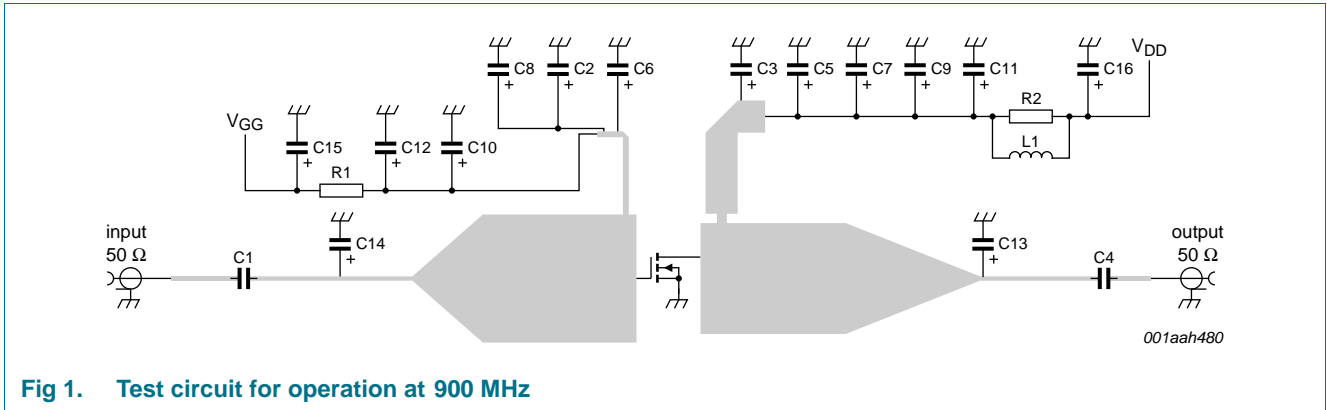


Fig 1. Test circuit for operation at 900 MHz

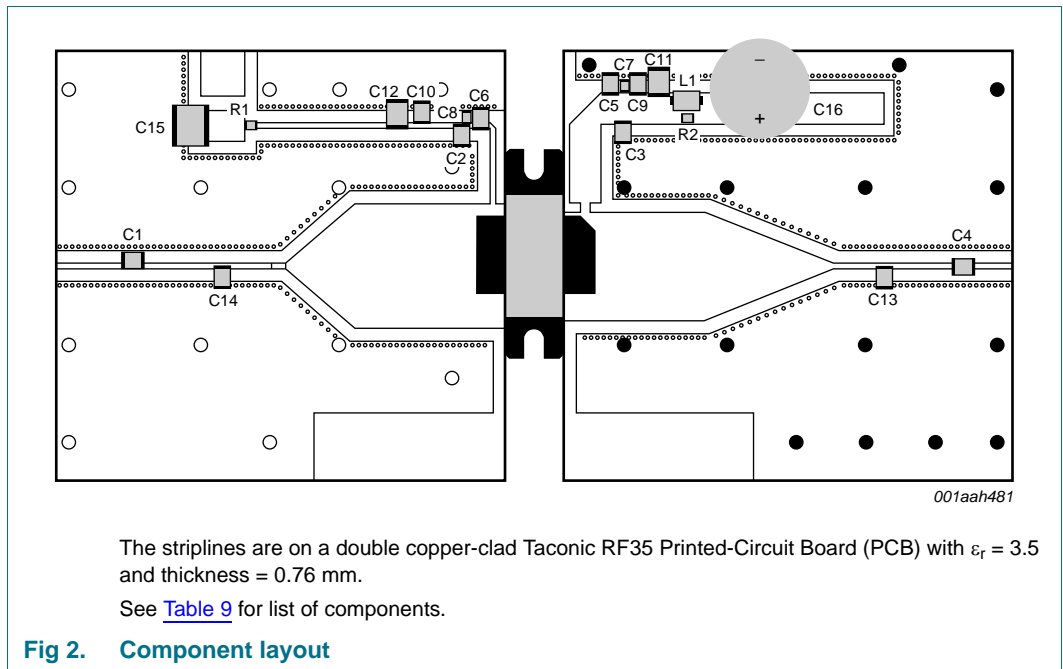


Fig 2. Component layout

**Table 9. List of components (see Figure 1 and Figure 2)**

All capacitors should be soldered vertically.

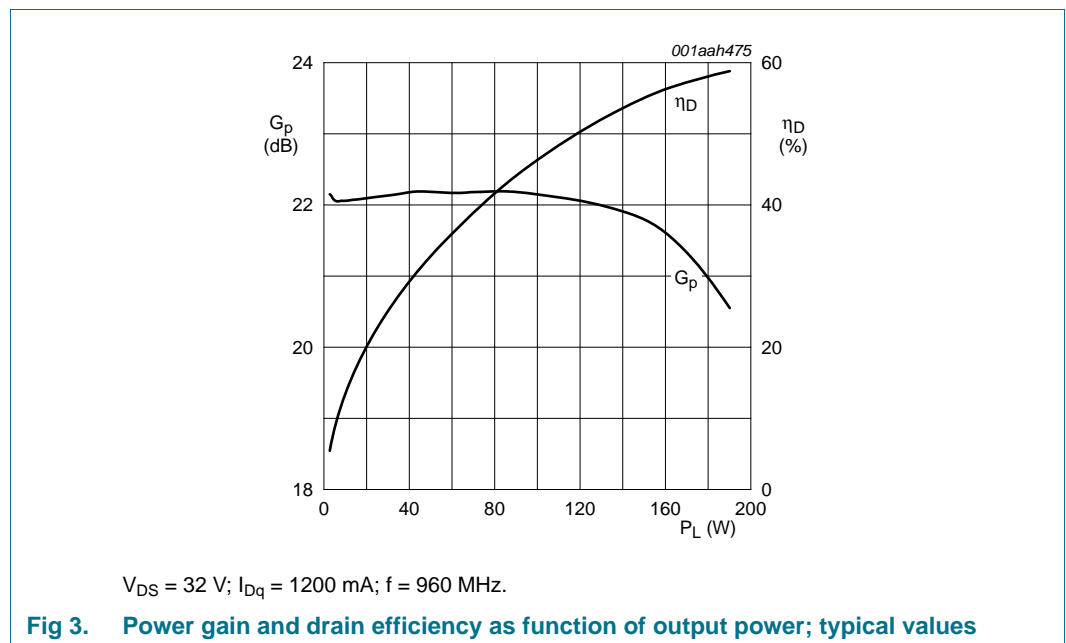
Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	68 pF [1]	
C5, C6	multilayer ceramic chip capacitor	560 pF [1]	
C7, C8	multilayer ceramic chip capacitor	330 nF, 50 V [2]	
C9, C10	multilayer ceramic chip capacitor	1.5 μF, 50 V [2]	
C11, C12	multilayer ceramic chip capacitor	4.5 μF, 50 V [2]	
C13	multilayer ceramic chip capacitor	2.20 pF [1]	
C14	multilayer ceramic chip capacitor	2.7 pF [1]	
C15	SMD tantalum capacitor	47 μF, 20 V	
C16	electrolytic capacitor	220 μF	
L1	ferrite SMD bead	-	Ferroxcube BDS 3/3/8.9-4S2 or equivalent
R1	SMD resistor	4.7 Ω, 0.1 W	
R2	SMD resistor	6.8 Ω, 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

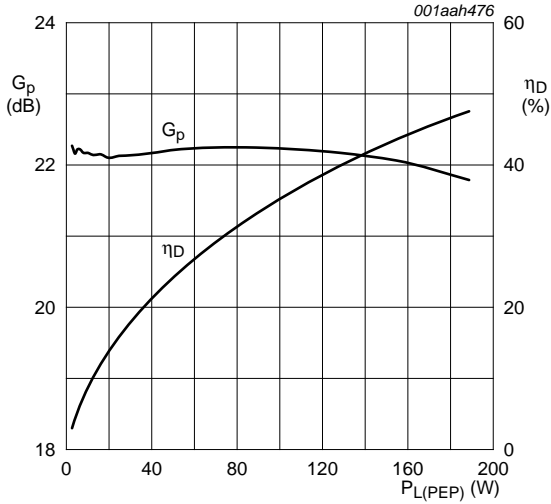
[2] TDK or capacitor of same quality.

## 7.3 Graphical data

### 7.3.1 1-Tone CW

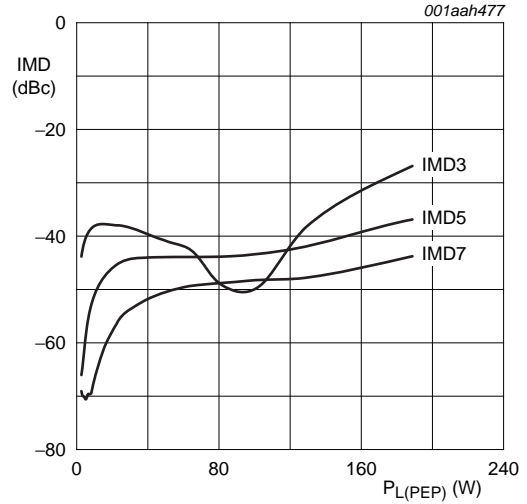


7.3.2 2-Tone CW



$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1200\text{ mA}$ ;  $f_1 = 959.95\text{ MHz}$ ;  $f_2 = 960.05\text{ MHz}$ .

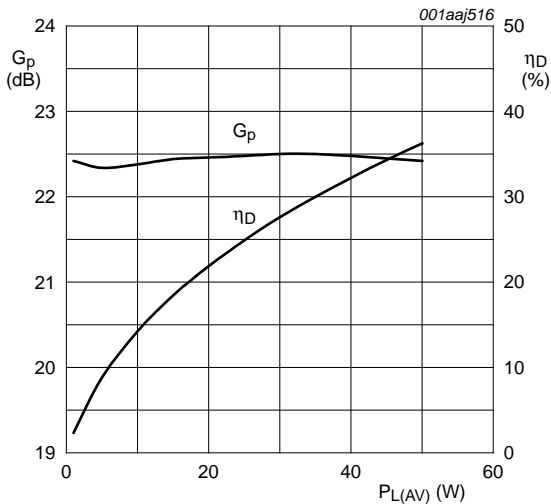
Fig 4. Power gain and drain efficiency as function of peak envelope power load power; typical values



$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1200\text{ mA}$ ;  $f_1 = 959.95\text{ MHz}$ ;  $f_2 = 960.05\text{ MHz}$ .

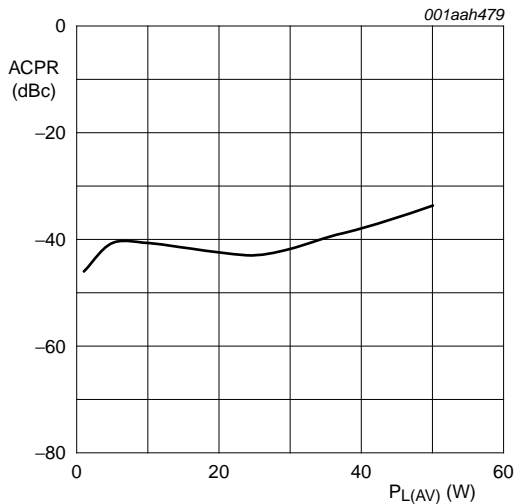
Fig 5. Intermodulation distortion as a function of peak envelope power load power; typical values

7.3.3 2-Carrier W-CDMA



$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1200\text{ mA}$ ;  $f_1 = 952.5\text{ MHz}$ ;  $f_2 = 957.5\text{ MHz}$ ; carrier spacing 5 MHz.

Fig 6. Power gain and drain efficiency as function of average output power; typical values



$V_{DS} = 32\text{ V}$ ;  $I_{DQ} = 1200\text{ mA}$ ;  $f_1 = 952.5\text{ MHz}$ ;  $f_2 = 957.5\text{ MHz}$ ; carrier spacing 5 MHz.

Fig 7. Adjacent power channel ratio as a function of average output power; typical values

## 8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

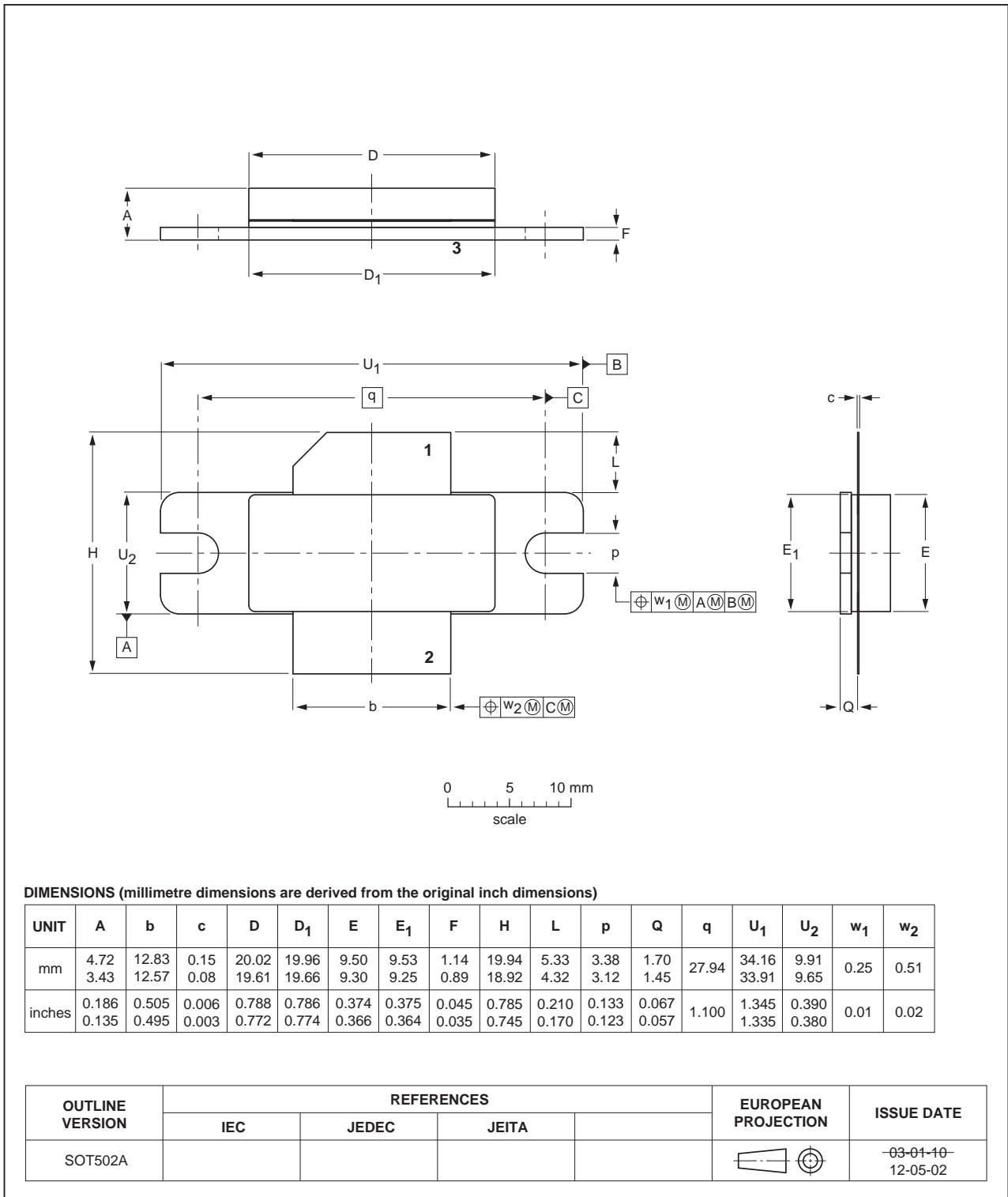


Fig 8. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

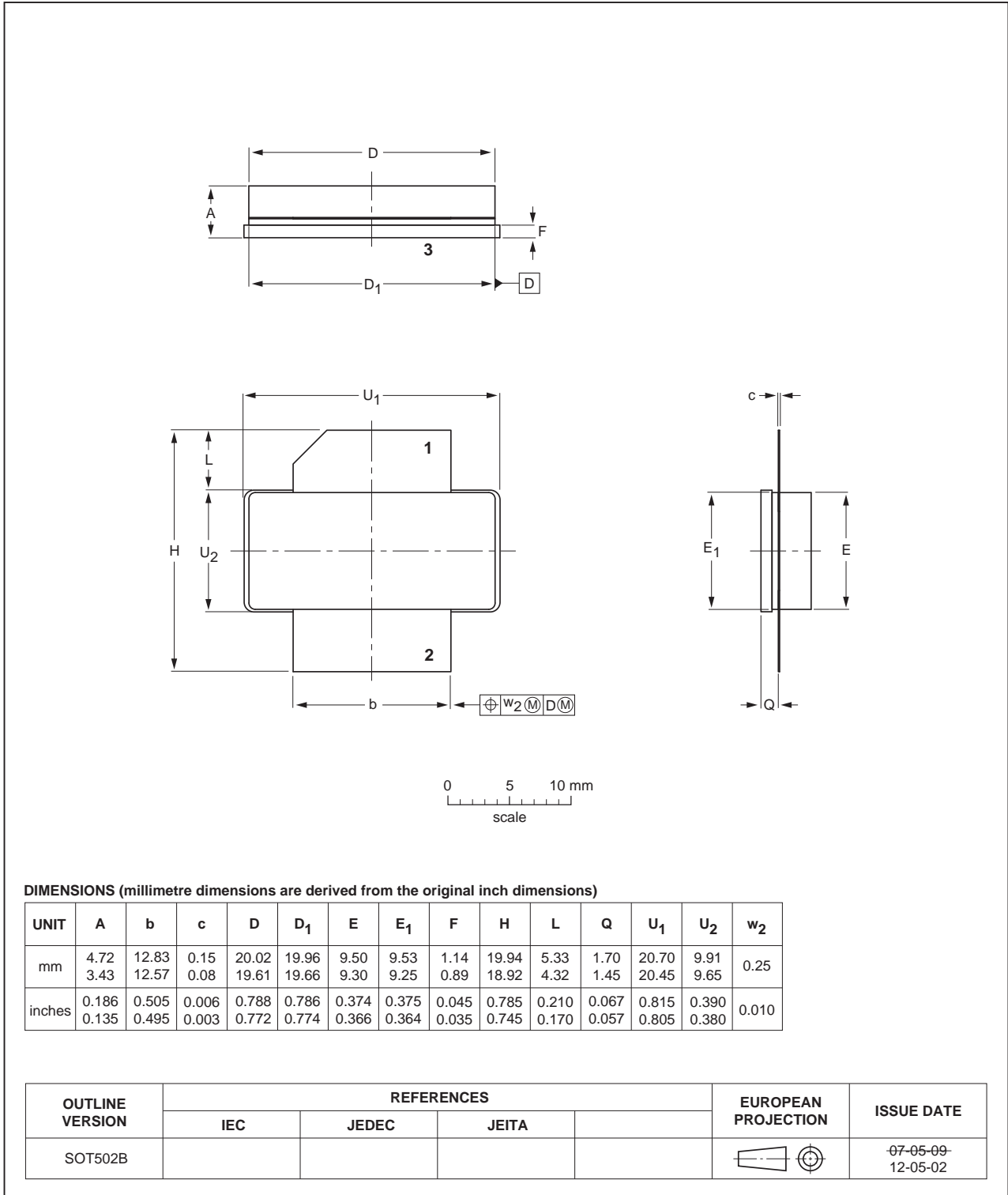


Fig 9. Package outline SOT502B



## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

**Table 10. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
DESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 11. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF10M6160_BLF10M6LS160 v.1	20140624	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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