BLF1721M8LS200

Power LDMOS transistor

Rev. 1 — 22 January 2016

AMPLEON

Product data sheet

1. Product profile

1.1 General description

200 W LDMOS power transistor for various applications such as Industrial, Scientific and Medical (ISM) and industrial heating at frequencies from 1700 MHz to 2100 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C; V_{DS} = 28 V; I_{Dq} = 1600 mA; in a class-AB demo circuit.

Test signal	f	$P_{L(1dB)}$	G_p [1]	η_D [1]	IMD3 [2]
	(MHz)	(W)	(dB)	(%)	(dBc)
CW RF	1700 to 1950	223.5	14.9	49.5	–35.4
	1900 to 2100	215.1	15.3	44.8	–26.9
pulsed RF [3]	1700 to 1950	276.0	15.2	55.8	-
	1900 to 2100	262.4	15.6	49.5	-

[1] at 1 dB compression.

[2] at V_{DS} = 28 V; I_{Dq} = 1600 mA; 2-tones; carrier spacing 5 MHz.

[3] t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

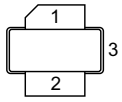
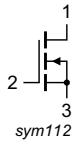
- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for pulsed and CW applications in the 1700 MHz to 2100 MHz frequency range such as ISM and industrial heating

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF1721M8LS200	-	earless flanged ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		−0.5	+13	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 55 W (CW); V_{DS} = 28 V; I_{Dq} = 2000 mA	0.263	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.3 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 330 mA	1.55	1.77	2.25	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	4.2	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	60	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	420	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 330 mA	-	2.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 11.55 A	-	45	-	mΩ

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 8.4 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2112.5 MHz; f_2 = 2117.5 MHz; f_3 = 2162.5 MHz; f_4 = 2167.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 2000 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)}$ = 55 W	18	19	-	dB
η_D	drain efficiency	$P_{L(AV)}$ = 55 W	23	28.5	-	%
RL_{in}	input return loss	$P_{L(AV)}$ = 55 W	-	−17	−6	dB
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)}$ = 55 W	-	−30	−25	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF1721M8LS200 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1600 mA; P_L = 200 W (CW); f = 2110 MHz.

7.2 Impedance information

Table 8. Typical impedance information

Measured load pull data. Typical values unless otherwise specified.
Z_S and Z_L defined in Figure 1.

f	Z_S	Z_L
(MHz)	(Ω)	(Ω)
1700	0.7 – j2.0	2.1 – j2.1
1800	0.7 – j2.1	2.4 – j2.4
1900	0.7 – j2.4	2.8 – j2.3
2000	0.6 – j2.9	3.7 – j1.9
2100	0.8 – j3.9	4.2 – j1.9

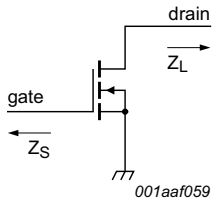
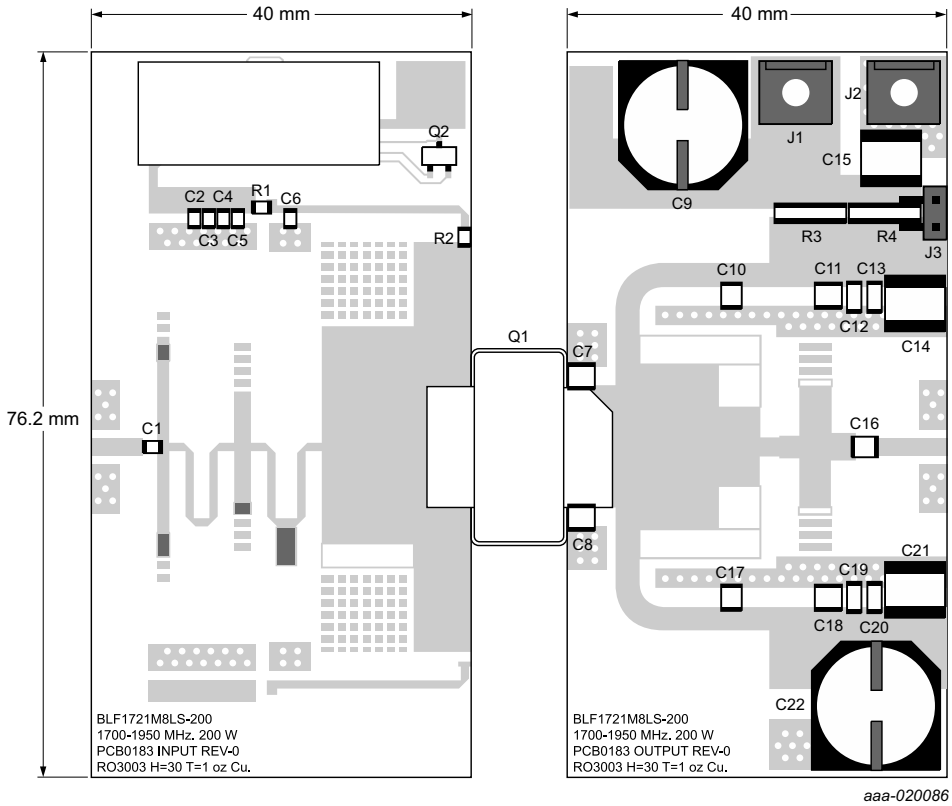


Fig 1. Definition of transistor impedance

7.3 Test circuit



Printed-Circuit Board (PCB): Rogers RO3003; ε_r = 3.0; thickness = 0.76 mm.

See Table 9 for list of components.

Fig 2. Component layout for test circuit for 1700 MHz to 1950 MHz

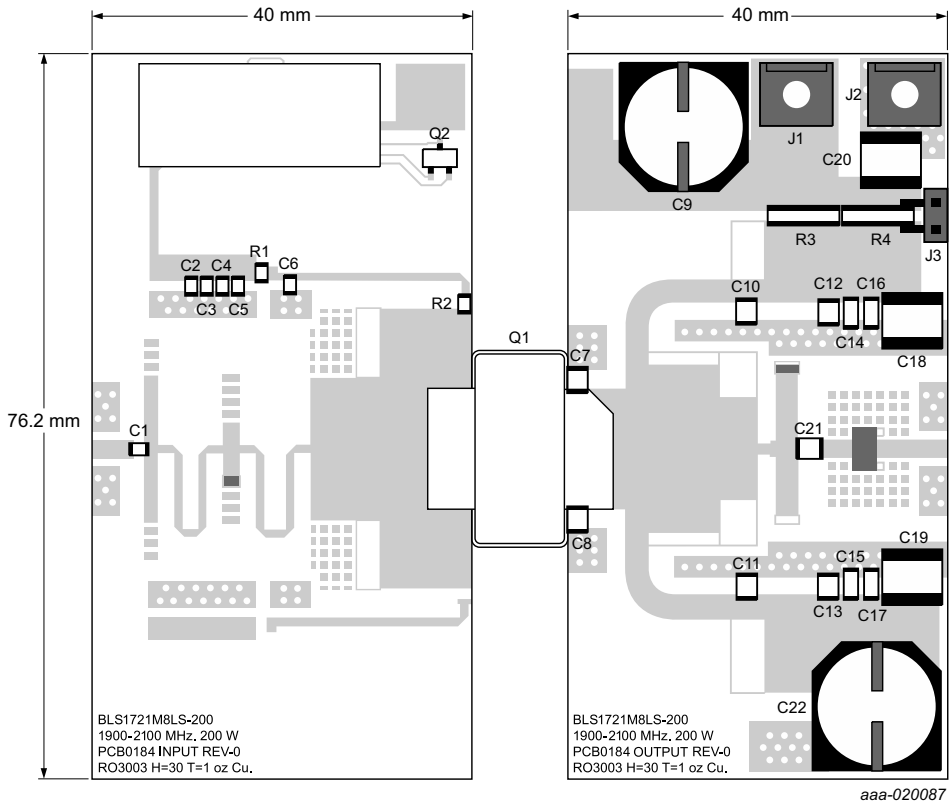
Table 9. List of components

For test circuit, see Figure 2.

Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	27 pF	ATC: ATC600F270
C2	multilayer ceramic chip capacitor	10 μF, 10 V	Murata: GRM21BR61A106KE19L
C3	multilayer ceramic chip capacitor	100 nF, 100 V	

Table 9. List of components *…continued*
For test circuit, see Figure 2.

Component	Description	Value	Remarks
C4	multilayer ceramic chip capacitor	10 nF, 50 V	Multicomp: U0805W103K1HRN-P4
C5	multilayer ceramic chip capacitor	240 pF	Passive Plus: 0805N
C7, C8	multilayer ceramic chip capacitor	3.3 pF	Passive Plus: 1111N
C9, C22	electrolytic capacitor	220 μF, 50 V	
C10, C17	multilayer ceramic chip capacitor	10 pF	ATC: ATC100B100
C11, C18	multilayer ceramic chip capacitor	330 pF	Passive Plus: 1111N
C12, C19	multilayer ceramic chip capacitor	0.01 μF, 250 V	TDK: C3225C0G2E103J160AA
C13, C20	multilayer ceramic chip capacitor	0.1 μF, 250 V	Murata: GRM32DR72E104KW01L
C14, C15, C21	multilayer ceramic chip capacitor	10 μF, 100 V	TDK: C5750X7S2A106M
C16	multilayer ceramic chip capacitor	33 pF,	Passive Plus: 1111N
C23	multilayer ceramic chip capacitor	-	
J1, J2	power connector	-	
J3	header connector	2 pin, 2.54 mm	Sullins: GBC02SFBN-M30
Q1	transistor	-	BLF1721M8LS200
Q2	PNP transistor	-	NXP: BC857B
R1	resistor	9.1 Ω	SMD 0805
R2	resistor	5 Ω	SMD 0805
R3, R4	resistor	0.005 Ω, 1 %	Susumu: RL7520WT-R005-F



Printed-Circuit Board (PCB): Rogers RO3003; ε_r = 3.0; thickness = 0.76 mm.

See Table 10 for list of components.

Fig 3. Component layout for test circuit for 1900 MHz to 2100 MHz

Table 10. List of components

For test circuit, see Figure 3.

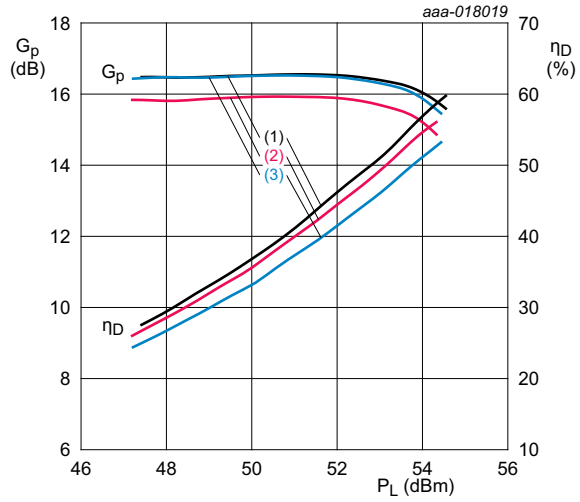
Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	27 pF	ATC: ATC600F270
C2	multilayer ceramic chip capacitor	10 μF, 10 V	Murata: GRM21BR61A106KE19L
C3	multilayer ceramic chip capacitor	100 nF, 100 V	
C4	multilayer ceramic chip capacitor	10 nF, 50 V	Multicomp: U0805W103K1HRN-P4
C5	multilayer ceramic chip capacitor	240 pF	Passive Plus: 0805N
C7, C8	multilayer ceramic chip capacitor	2.7 pF	ATC: ATC100B
C9, C22	electrolytic capacitor	220 μF, 50 V	
C10, C11	multilayer ceramic chip capacitor	10 pF	ATC: ATC100B100
C12, C13	multilayer ceramic chip capacitor	330 pF	Passive Plus: 1111N
C14, C15	multilayer ceramic chip capacitor	0.01 μF, 250 V	TDK: C3225C0G2E103J160AA
C16, C17	multilayer ceramic chip capacitor	0.1 μF, 250 V	Murata: GRM32DR72E104KW01L
C18, C19, C20	multilayer ceramic chip capacitor	10 μF, 100 V	TDK: C5750X7S2A106M

Table 10. List of components *...continued*
For test circuit, see Figure 3.

Component	Description	Value	Remarks
C21	multilayer ceramic chip capacitor	33 pF,	Passive Plus: 1111N
J1, J2	power connector	-	
J3	header connector	2 pin, 0.1 inch	Sullins: GBC02SFBN-M30
Q1	transistor	-	BLF1721M8LS200
Q2	PNP transistor	-	NXP: BC857B
R1	resistor	9.1 Ω	SMD 0805
R2	resistor	5 Ω	SMD 0805
R3, R4	resistor	0.005 Ω, 1 %	Susumu: RL7520WT-R005-F

7.4 Graphical data

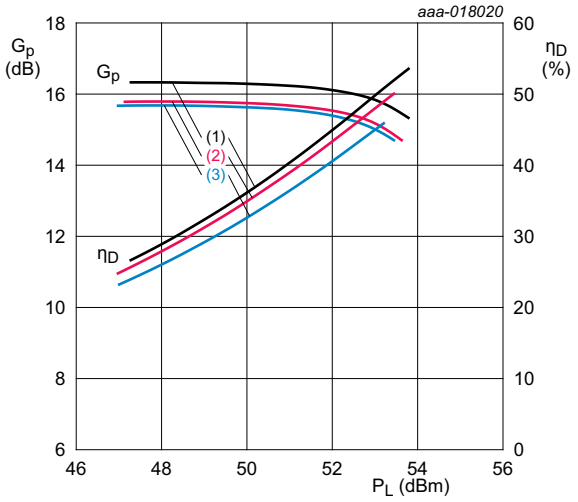
7.4.1 1700 MHz to 1950 MHz



V_{DS} = 28 V; I_{Dq} = 1600 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1700 MHz
(2) f = 1800 MHz
(3) f = 1900 MHz

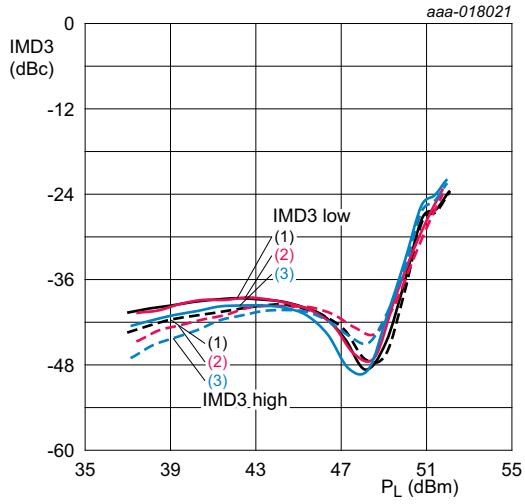
Fig 4. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1700 MHz
(2) f = 1800 MHz
(3) f = 1900 MHz

Fig 5. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA; CW; 2-tones; carrier spacing 5 MHz.

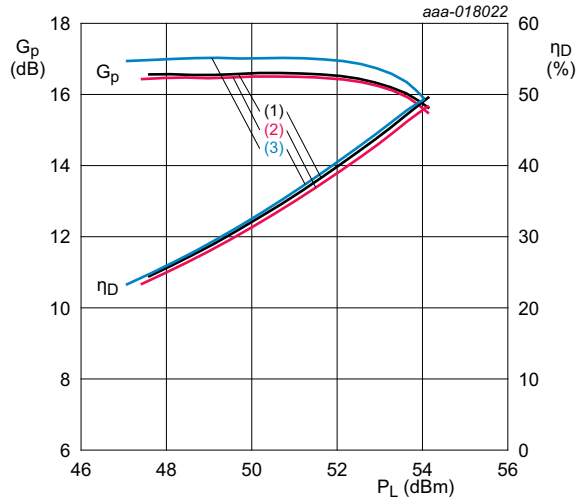
(1) f = 1700 MHz

(2) f = 1800 MHz

(3) f = 1900 MHz

Fig 6. Third-order intermodulation distortion as a function of output power; typical values

7.4.2 1900 MHz to 2100 MHz



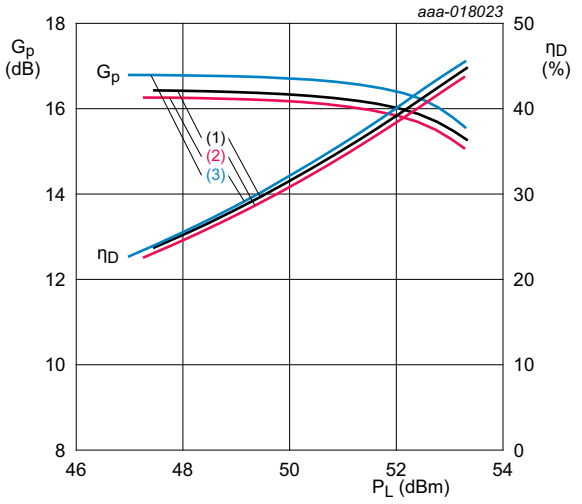
V_{DS} = 28 V; I_{Dq} = 1600 mA; t_p = 100 μs; δ = 10 %.

(1) f = 1900 MHz

(2) f = 2000 MHz

(3) f = 2100 MHz

Fig 7. Power gain and drain efficiency as function of output power; typical values



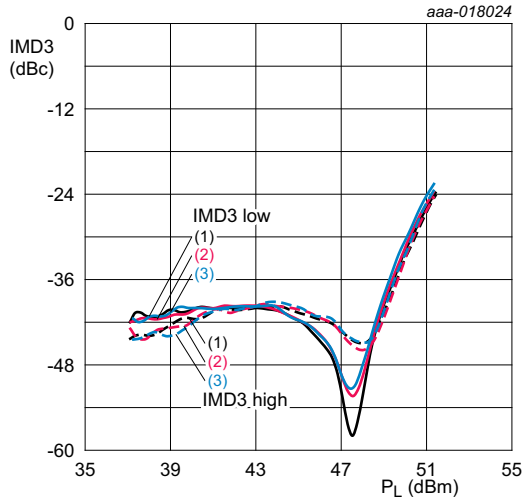
V_{DS} = 28 V; I_{Dq} = 1600 mA.

(1) f = 1900 MHz

(2) f = 2000 MHz

(3) f = 2100 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values



V_{DS} = 28 V; I_{Dq} = 1600 mA; CW; 2-tones; carrier spacing 5 MHz.

(1) f = 1900 MHz

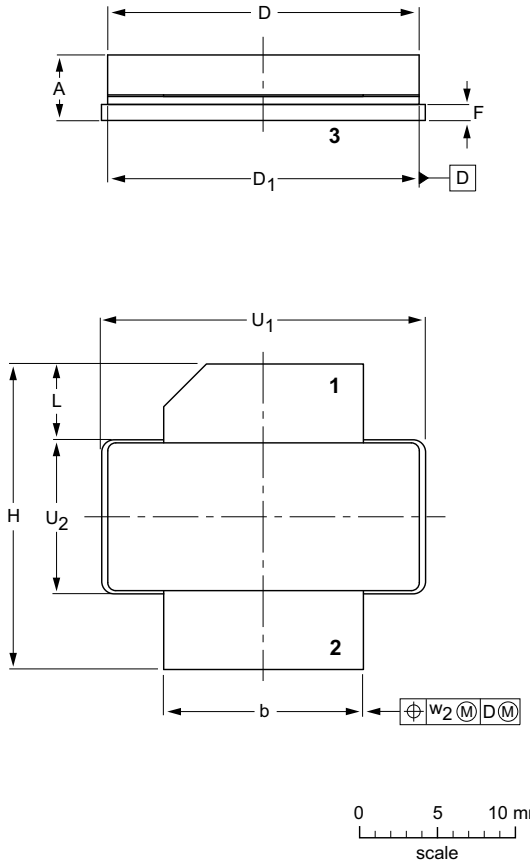
(2) f = 2000 MHz

(3) f = 2100 MHz

Fig 9. Third-order intermodulation distortion as a function of output power; typical values

8. Package outline

Earless flanged ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~07-05-09~~ 12-05-02

Fig 10. Package outline SOT502B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF1721M8LS200 v.1	20160122	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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14. Contents

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