BLF189XRB; BLF189XRBS

Power LDMOS transistor

Rev. 1 — 3 October 2017 **Product data sheet**

1. Product profile

1.1 General description

A 1900 W extremely rugged LDMOS power transistor for industrial pulsed applications in the HF to 150 MHz band.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	1900	26	72.5

1.2 Features and benefits

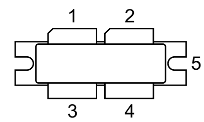
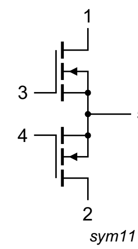
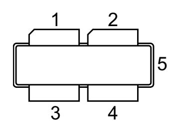
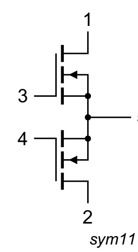
- Easy power control
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness VSWR > 65 : 1
- High efficiency
- Excellent thermal stability
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF189XRB (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF189XRBS (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF189XRB	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF189XRBS	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

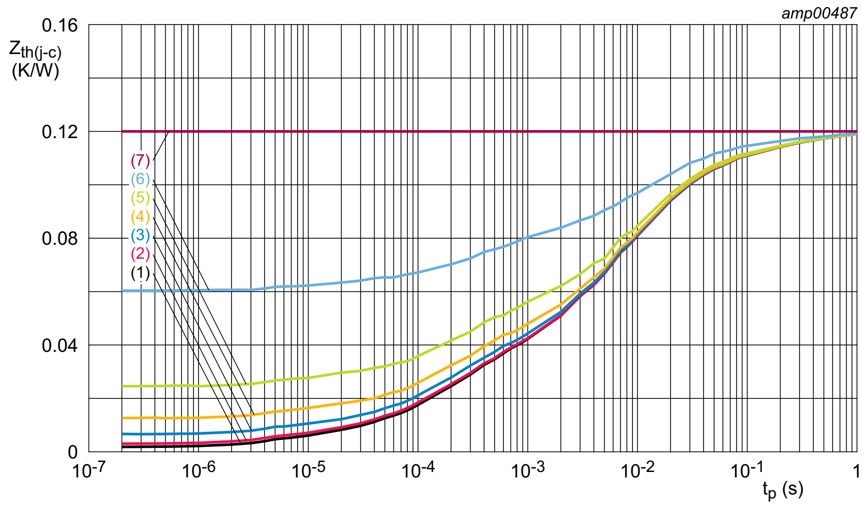
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 150 °C [1][2]	0.12	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	0.036	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 7.8 mA	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 780 mA	1.33	1.9	2.33	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 100 mA	1.10	1.67	2.10	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA

Table 6. DC characteristics *...continued*

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75$ V; V_{DS} = 10 V	-	106	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75$ V; I_D = 27.3 A	-	0.06	-	Ω

Table 7. AC characteristics

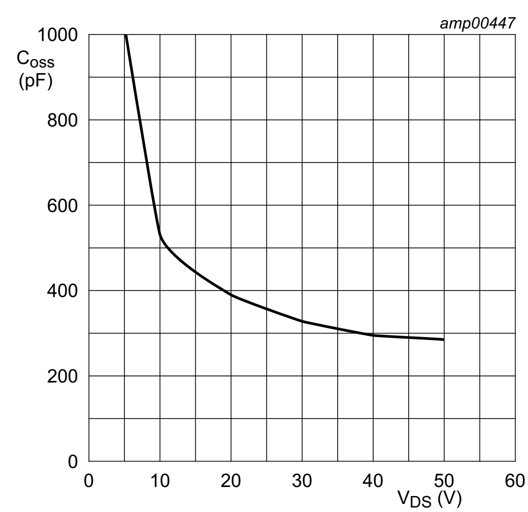
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	6.7	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	750	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	284	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 200 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1900 W	24.5	26	-	dB
RL_{in}	input return loss	P_L = 1900 W	-	–9	-	dB
η_D	drain efficiency	P_L = 1900 W	69	72.5	-	%



V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLF189XRB and BLF189XRBS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 200 mA; P_L = 1900 W pulsed; f = 108 MHz.

7.2 Impedance information

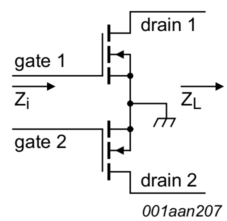


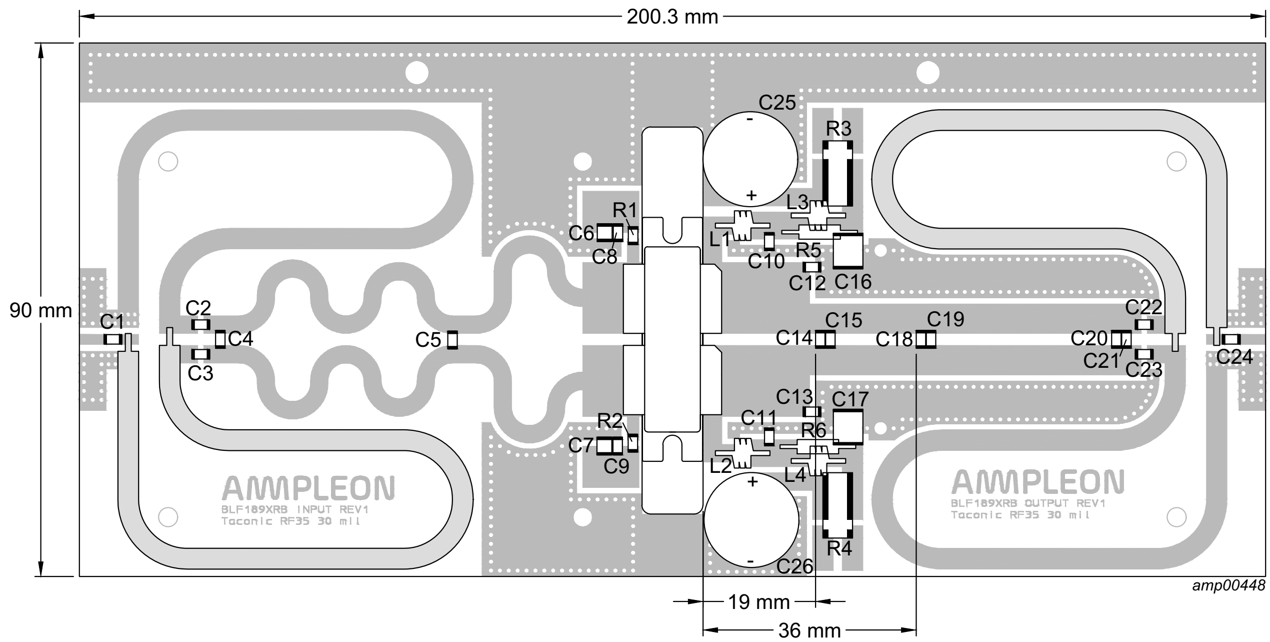
Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 1900 W.

f	Z_i	Z_L
(MHz)	(Ω)	(Ω)
108	1.7 – j6.0	2.0 + j0.4

7.3 Test circuit



Printed-Circuit Board (PCB): RF-35; ε_r = 3.5 F/m; thickness = 0.765 mm; thickness copper plating = 35 μm.

See Table 10 for a list of components.

Fig 4. Component layout for class-AB production test circuit

Table 10. List of components

For test circuit see Figure 4.

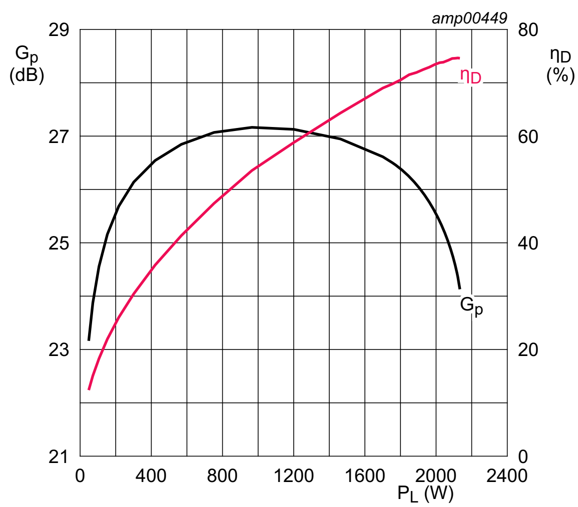
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	470 pF [1]	
C2, C3	multilayer ceramic chip capacitor	68 pF [1]	
C4	multilayer ceramic chip capacitor	43 pF [1]	
C5	multilayer ceramic chip capacitor	240 pF [1]	
C6, C7	multilayer ceramic chip capacitor	4.7 μF, 50 V	
C8, C9	multilayer ceramic chip capacitor	920 pF [1]	
C10, C11	multilayer ceramic chip capacitor	920 pF [1]	
C12, C13	multilayer ceramic chip capacitor	160 pF [1]	
C14, C15	multilayer ceramic chip capacitor	120 pF [1]	
C16, C17	multilayer ceramic chip capacitor	4.7 μF, 100 V	
C18, C19	multilayer ceramic chip capacitor	51 pF [1]	
C20, C21	multilayer ceramic chip capacitor	56 pF [1]	
C22, C23	multilayer ceramic chip capacitor	100 pF [1]	
C24	multilayer ceramic chip capacitor	470 pF [1]	
C25, C26	electrolytic capacitor	2200 μF, 64 V	
L1, L2	air inductor	3 turns, D = 4 mm	1mm copper wire
L3, L4	air inductor	5 turns, D = 4 mm	1mm copper wire

Table 10. List of components *...continued*
For test circuit see Figure 4.

Component	Description	Value	Remarks
R1, R2	resistor	4.7 kΩ	SMD 1206
R3, R4	resistor	0.01 Ω	FC4L110R010FER
R5, R6	resistor	4.7 Ω, 0.6 w	SMD 1206
T1, T2	semi rigid coax	50 Ω, 160 mm	EZ 141-AL-TP/M17

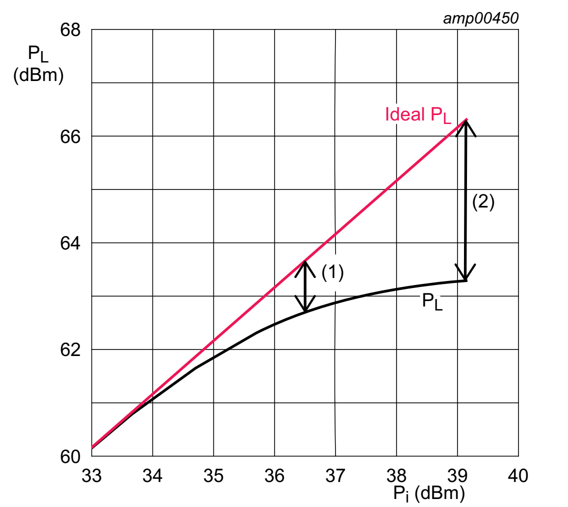
[1] American Technical Ceramics type 100B or capacitor of same quality

7.4 Graphical data



V_{DS} = 50 V; I_{Dq} = 200 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values

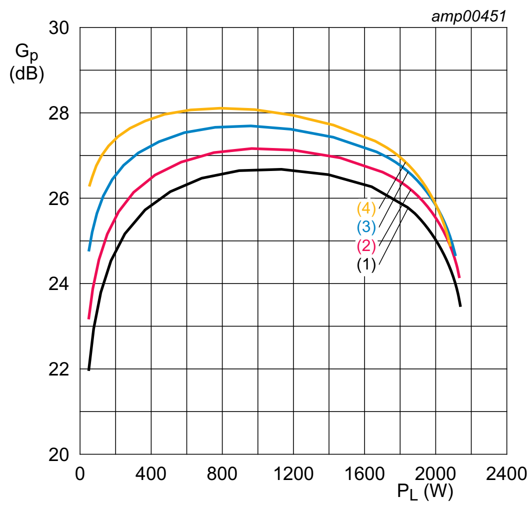


V_{DS} = 50 V; I_{Dq} = 200 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) $P_{L(1dB)}$ = 62.7 dBm (1870 W)

(2) $P_{L(3dB)}$ = 63.3 dBm (2132 W)

Fig 6. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

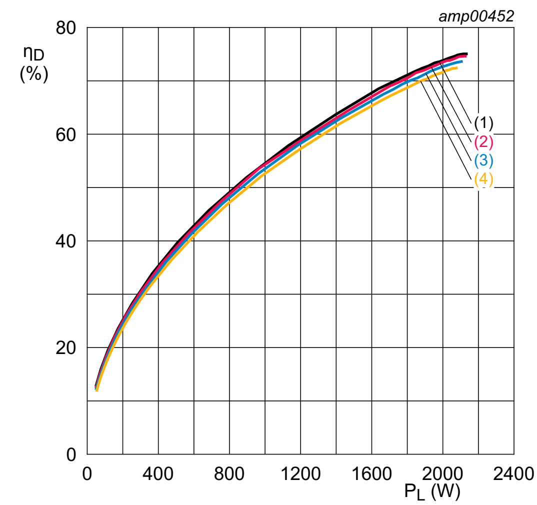
(1) I_{Dq} = 50 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 800 mA

(4) I_{Dq} = 2000 mA

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 108 MHz; t_p = 100 μs; δ = 20 %.

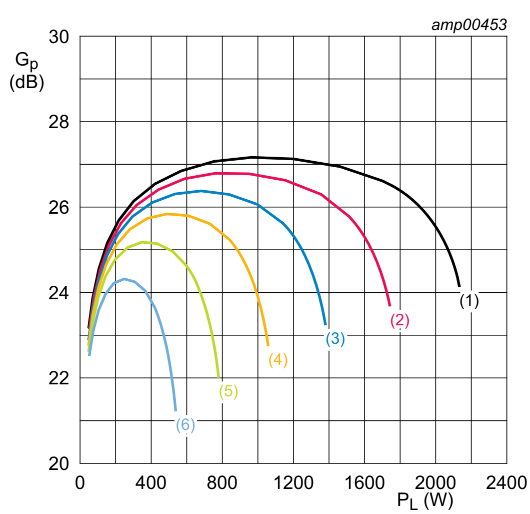
(1) I_{Dq} = 50 mA

(2) I_{Dq} = 200 mA

(3) I_{Dq} = 800 mA

(4) I_{Dq} = 2000 mA

Fig 8. Drain efficiency as a function of output power; typical values



I_{Dq} = 200 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

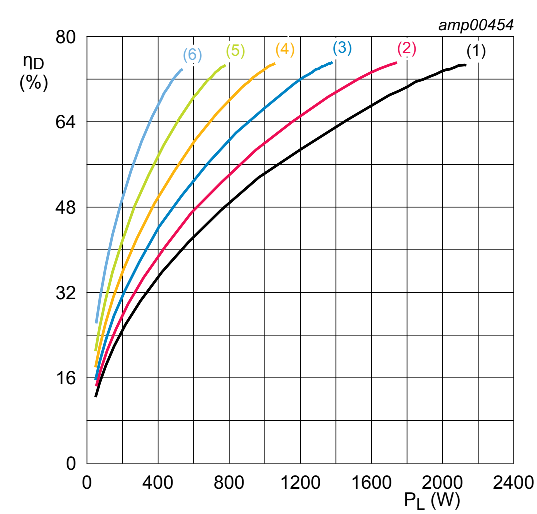
(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 9. Power gain as a function of output power; typical values



I_{Dq} = 200 mA; f = 108 MHz; t_p = 100 μs; δ = 20 %.

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

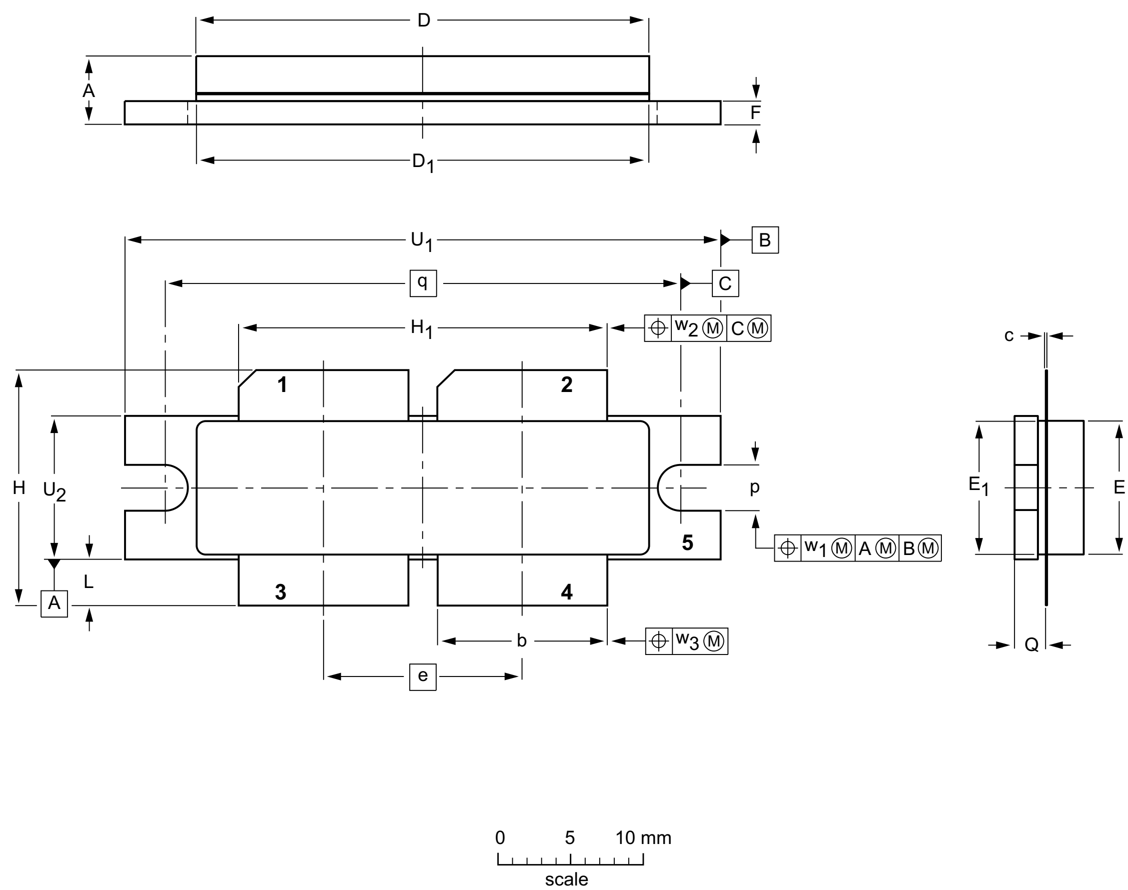
(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

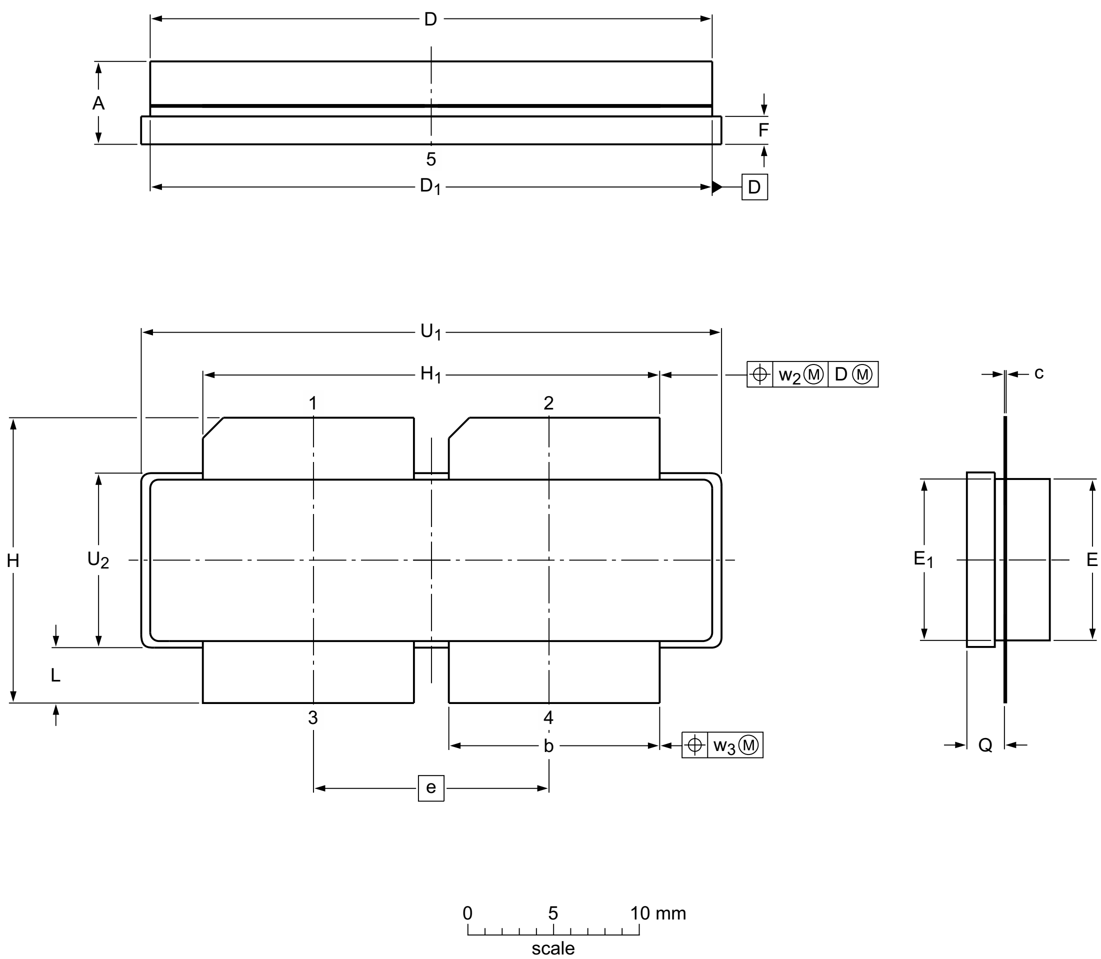
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 11. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539B						~~12-05-02~~ 13-05-24

Fig 12. Package outline SOT539B

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF189XRB_BLF189XRBS v.1	20171003	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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For sales office addresses, please visit: **http://www.ampleon.com/sales**

14. Contents

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