

# BLF2425M6L180P; BLF2425M6LS180P

Power LDMOS transistor

Rev. 3 — 12 July 2013

Product data sheet

## 1. Product profile

### 1.1 General description

180 W LDMOS power transistor for various applications such as ISM and industrial heating at frequencies from 2400 MHz to 2500 MHz.

**Table 1. Typical performance**

*RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.*

Test signal	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)
CW	2450	10	28	180	13.3	53.5

### 1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

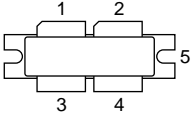
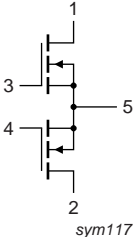
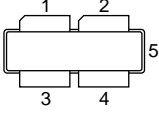
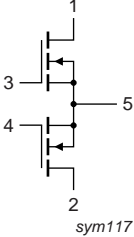
### 1.3 Applications

- RF power amplifiers for CW applications in the 2400 MHz to 2500 MHz frequency range such as ISM and industrial heating.



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF2425M6L180P (SOT539A)</b>			
1	drain1		 <p style="text-align: right; font-size: small;">sym117</p>
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF2425M6LS180P (SOT539B)</b>			
1	drain1		 <p style="text-align: right; font-size: small;">sym117</p>
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF2425M6L180P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF2425M6LS180P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 180\text{ W}$	0.38	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.4	1.8	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$				
		$V_{DS} = 28\text{ V}$	-	-	3	$\mu\text{A}$
		$V_{DS} = 65\text{ V}$	-	-	5	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $V_{DS} = 10\text{ V}$	-	24	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	300	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 7.2\text{ A}$	-	10	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V};$ $I_D = 5\text{ A}$	-	0.1	-	$\Omega$

**Table 7. RF characteristics**

Test signal: CW;  $f = 2450\text{ MHz}$ ;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 10\text{ mA}$ ;  $T_{case} = 25\text{ °C}$  unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 180\text{ W}$	11.0	13.3	-	dB
$\eta_D$	drain efficiency	$P_L = 180\text{ W}$	50	53.5	-	%
$RL_{in}$	input return loss	$P_L = 180\text{ W}$	-	-15	-9	dB

## 7. Test information

### 7.1 Ruggedness in class-AB operation

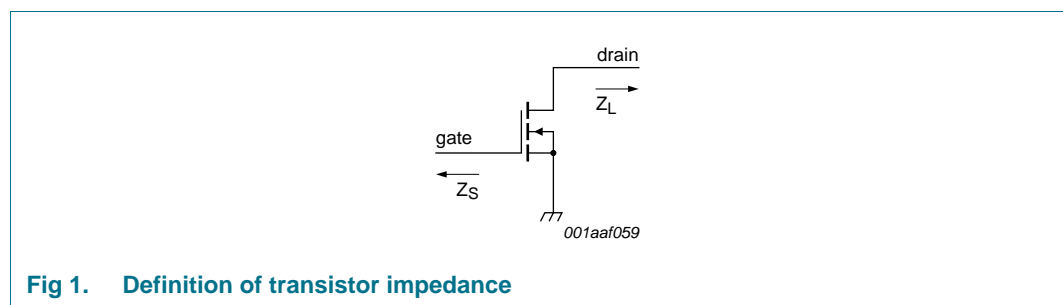
The BLF2425M6L180P and BLF2425M6LS180P are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 5 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 10\text{ mA}$ ;  $P_L = 180\text{ W}$  (CW);  $f = 2450\text{ MHz}$ .

7.2 Impedance information

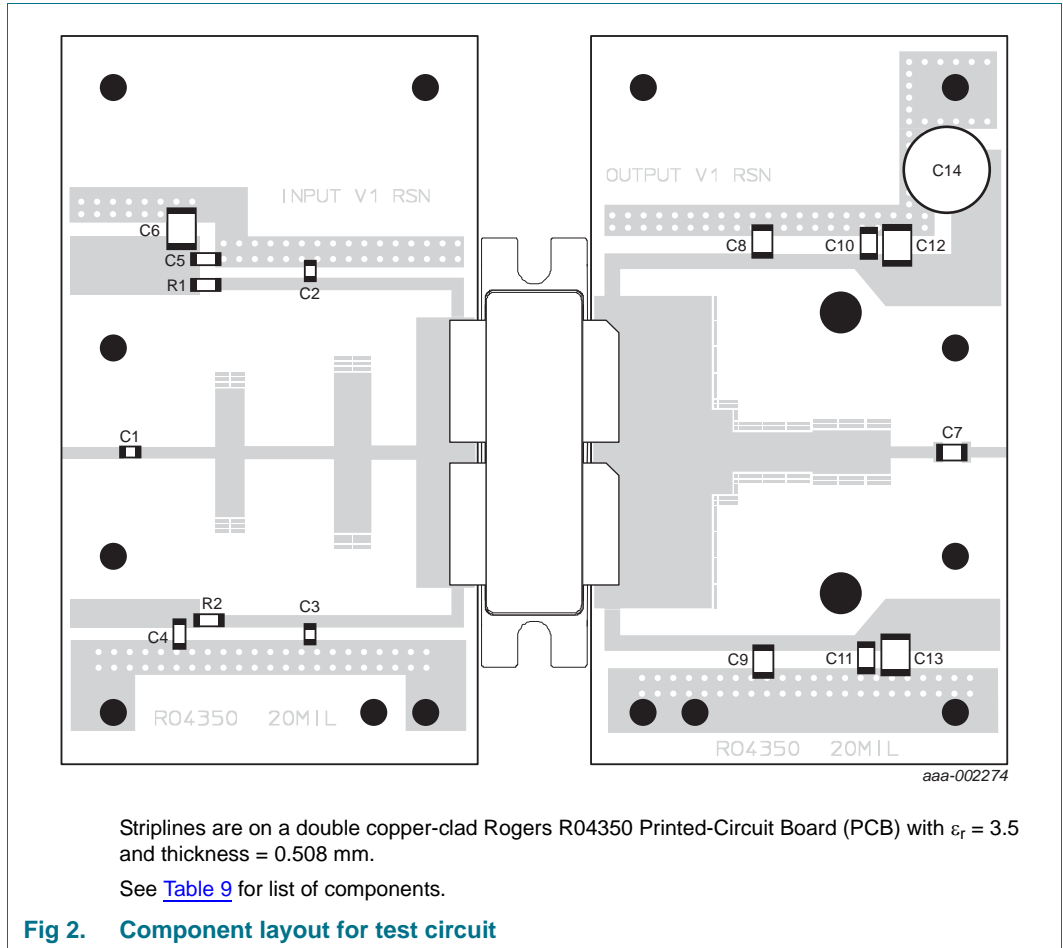
Table 8. Typical impedance

Measured load-pull data. Typical values per section.  
 $Z_S$  and  $Z_L$  defined in Figure 1.

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
2400	5.9 – j8.0	2.8 – j3.1
2450	8.4 – j7.6	2.5 – j3.1
2500	10.6 – j5.8	2.3 – j3.0



7.3 Test circuit



**Table 9. List of components**

For test circuit, see [Figure 2](#).

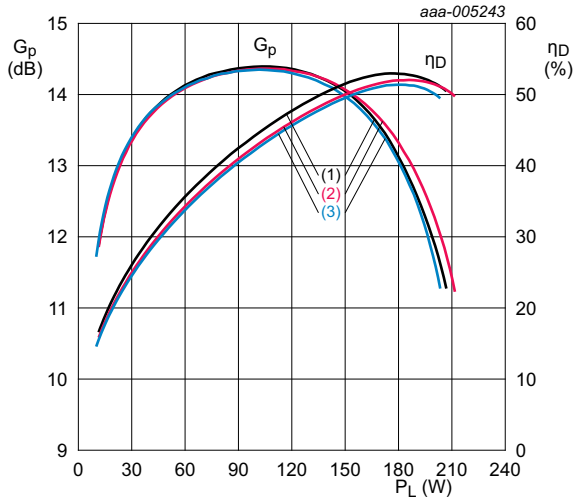
Component	Description	Value	Remarks
C1, C2, C3	multilayer ceramic chip capacitor	15 pF	[1]
C4, C5, C10, C11	multilayer ceramic chip capacitor	220 nF	SMD 1206
C6, C12, C13	multilayer ceramic chip capacitor	4.7 $\mu$ F	
C7	multilayer ceramic chip capacitor	39 pF	[2]
C8, C9	multilayer ceramic chip capacitor	6.8 pF	[3]
C14	electrolytic capacitor	220 $\mu$ F, 63 V	
R1, R2	chip resistor	6.2 $\Omega$	SMD 1206

[1] American technical ceramics type 100A or capacitor of same quality.

[2] American technical ceramics type 800B or capacitor of same quality.

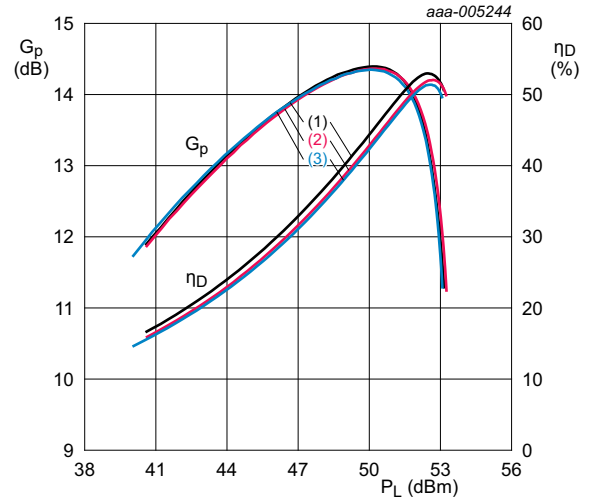
[3] American technical ceramics type 100B or capacitor of same quality.

7.4 Graphical data



V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 10 mA.  
 (1) f = 2400 MHz  
 (2) f = 2450 MHz  
 (3) f = 2500 MHz

Fig 3. Power gain and drain efficiency as function of load power; typical values



V<sub>DS</sub> = 28 V; I<sub>Dq</sub> = 10 mA.  
 (1) f = 2400 MHz  
 (2) f = 2450 MHz  
 (3) f = 2500 MHz

Fig 4. Power gain and drain efficiency as function of load power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

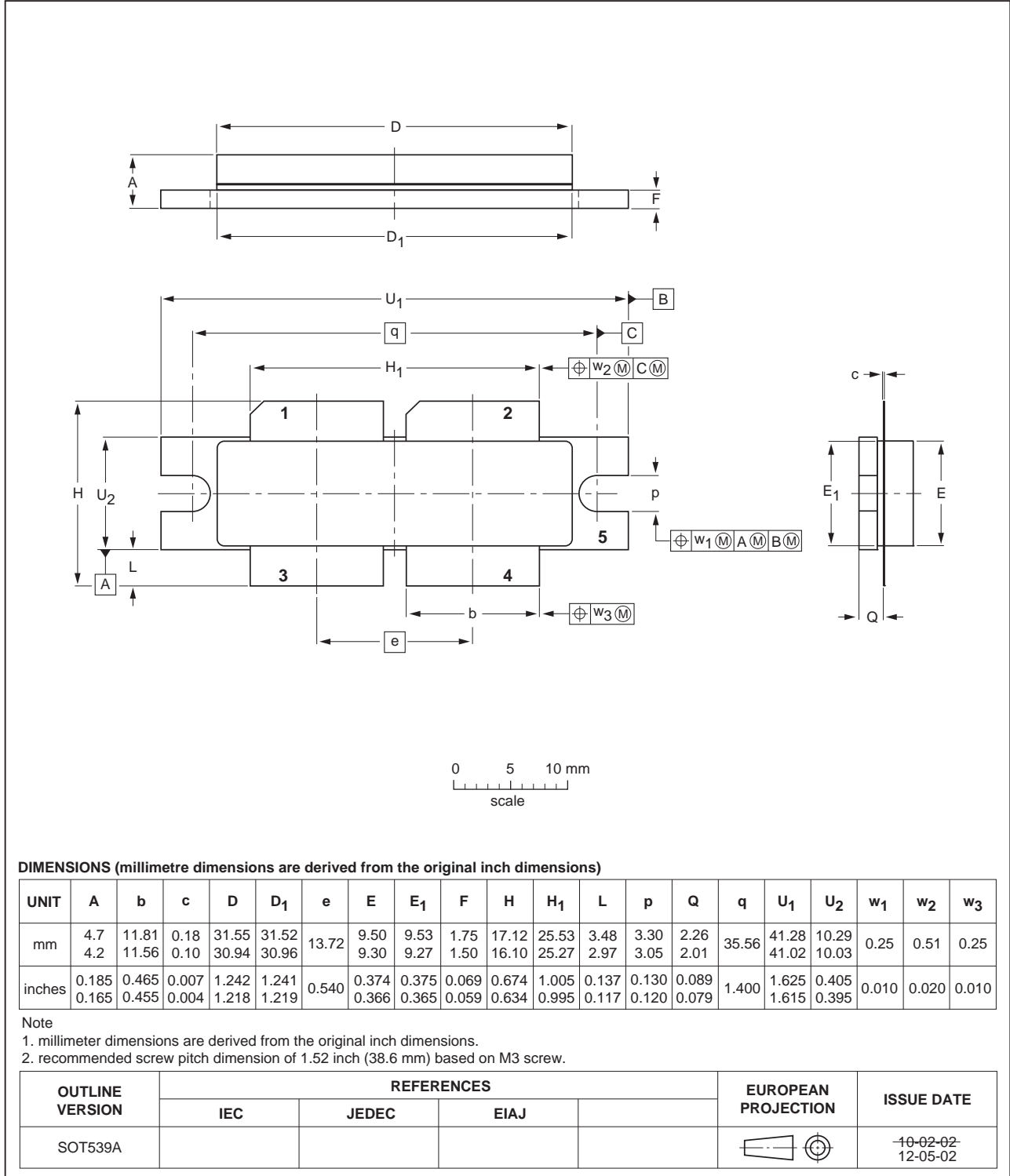


Fig 5. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

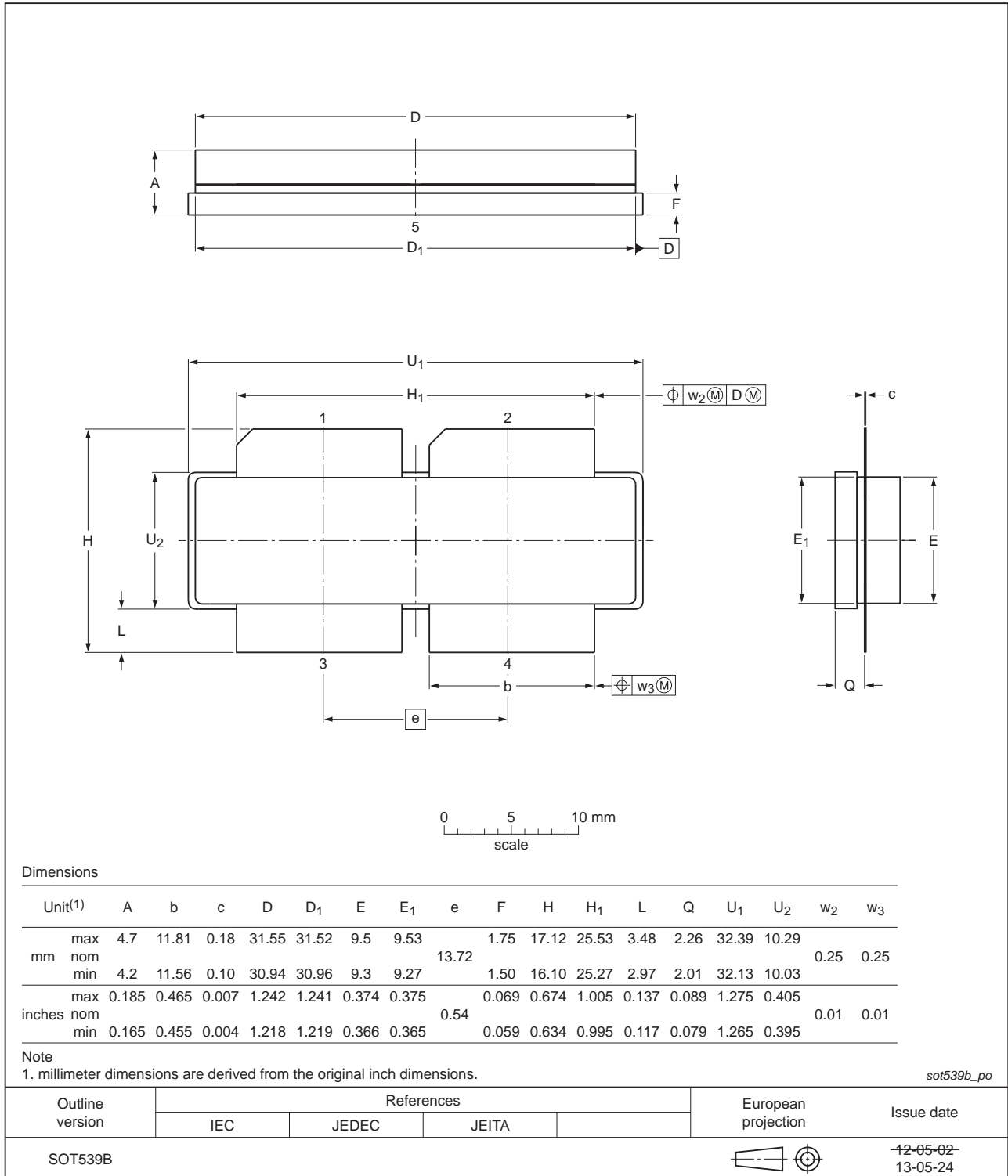


Fig 6. Package outline SOT539B



## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF2425M6L180P_25M6LS180P v.3	20130712	Product data sheet	-	BLF2425M6L180P_25M6LS180P v.2
Modifications:	<ul style="list-style-type: none"> <li>The package outline <a href="#">Figure 6</a> is updated.</li> </ul>			
BLF2425M6L180P_25M6LS180P v.2	20120920	Product data sheet	-	BLF2425M6L180P_25M6LS180P v.1
Modifications:	<ul style="list-style-type: none"> <li>The status of this document has been changed to Product data sheet.</li> <li>Table 1 on page 1: several changes have been made.</li> <li>Section 1.2 on page 1: several changes have been made.</li> <li>Table 4 on page 2: an item has been removed.</li> <li>Table 6 on page 3: several changes have been made.</li> <li>Table 7 on page 3: several changes have been made.</li> <li>Section 7.1 on page 3: a value has been added.</li> <li>Section 7.4 on page 6: this section has been added.</li> </ul>			
BLF2425M6L180P_25M6LS180P v.1	20120207	Objective data sheet	-	-

## 12. Legal information

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[2] The term 'short data sheet' is explained in section "Definitions".

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