

BLF4G10-120; BLF4G10S-120

UHF power LDMOS transistor

Rev. 01 — 10 January 2006

Product data sheet

1. Product profile

1.1 General description

120 W LDMOS power transistor for base station applications at frequencies from 800 MHz to 1000 MHz.

Table 1: Typical performance

RF performance at $T_h = 25^\circ\text{C}$ in a common base class-AB test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _L (W)	G _p (dB) (typ)	η_D (%)	ACPR ₄₀₀ (dBc) (typ)	ACPR ₆₀₀ (dBc) (typ)	EVM _{rms} (%)	IMD3 (dBc) (typ)
CW	861 to 961	28	120	19	57	-	-	-	-
GSM EDGE	861 to 961	28	48 (AV)	19	40	-61 [1]	-72 [2]	1.5	-
2-tone	861 to 961	28	120 (PEP)	19	46	-	-	-	-31

[1] ACPR₄₀₀ at 30 kHz resolution bandwidth

[2] ACPR₆₀₀ at 30 kHz resolution bandwidth

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

- Typical GSM EDGE performance at frequency of 960 MHz, a supply voltage of 28 V and an I_{DQ} of 850 mA:
 - ◆ Load power = 48 W (AV)
 - ◆ Gain = 19 dB (typ)
 - ◆ Efficiency = 40 % (typ)
 - ◆ ACPR₄₀₀ = -61 dBc (typ)
 - ◆ ACPR₆₀₀ = -72 dBc (typ)
 - ◆ EVM_{rms} = 1.5 % (typ)
- Easy power control
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (800 MHz to 1000 MHz)
- Internally matched for ease of use

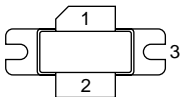
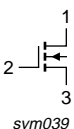
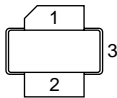
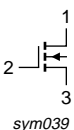
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1.3 Applications

- RF power amplifiers for GSM, GSM EDGE and CDMA base stations and multicarrier applications in the 800 MHz to 1000 MHz frequency range.

2. Pinning information

Table 2: Pinning

Pin	Description	Simplified outline	Symbol
BLF4G10-120 (SOT502A)			
1	drain		 sym039
2	gate		
3	source		
BLF4G10S-120 (SOT502B)			
1	drain		 sym039
2	gate		
3	source		

[1] Connected to flange

3. Ordering information

Table 3: Ordering information

Type number	Package		
	Name	Description	Version
BLF4G10-120	-	flanged LDMOST ceramic package; 2 mounting holes; 2 leads	SOT502A
BLF4G10S-120	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+15	V
I_D	drain current		-	12	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$				
		$P_L = 60\text{ W}$	-	0.76	0.85	K/W
		$P_L = 120\text{ W}$	-	0.65	0.74	K/W

6. Characteristics

Table 6: Characteristics

$T_j = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.9\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 180\text{ mA}$	2.5	3.1	3.5	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}$; $I_D = 900\text{ mA}$	2.7	3.2	3.7	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	3	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $V_{DS} = 10\text{ V}$	27	30	-	A
I_{GSS}	gate leakage current	$V_{GS} = 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 10\text{ A}$	-	9.0	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 6\text{ V}$; $I_D = 6\text{ A}$	-	0.09	-	Ω
C_{rs}	feedback capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$; $f = 1\text{ MHz}$	-	2.5	-	pF

7. Application information

Table 7: Application information

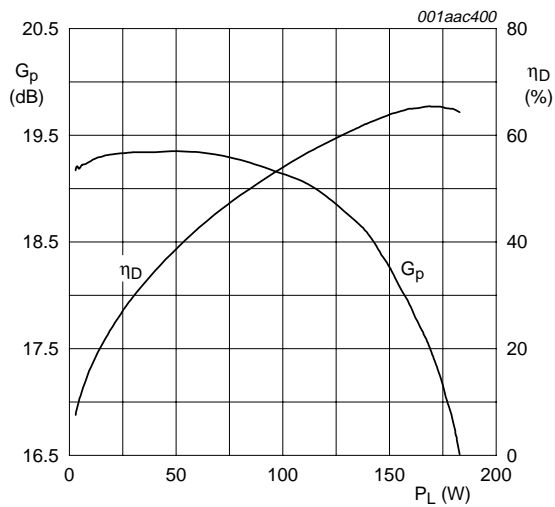
Mode of operation: 2-tone (100 kHz tone spacing); $f = 960\text{ MHz}$.

$V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $T_{case} = 25\text{ °C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(PEP)} = 120\text{ W}$	18	19	-	dB
IRL	input return loss	$P_{L(PEP)} = 120\text{ W}$	-	-8	-5	dB
η_D	drain efficiency	$P_{L(PEP)} = 120\text{ W}$	44	46	-	%
IMD3	third order intermodulation distortion	$P_{L(PEP)} = 120\text{ W}$	-	-31	-27	dBc

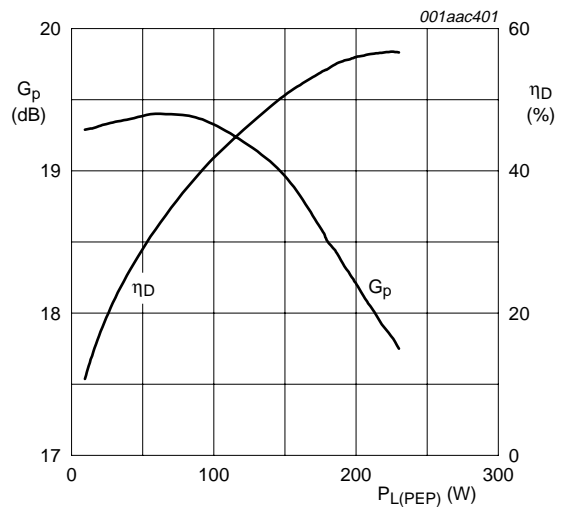
7.1 Ruggedness in class-AB operation

The BLF4G10-120 and BLF4G10S-120 are capable of withstanding a load mismatch corresponding to $V_{SWR} = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $P_L = 120\text{ W (CW)}$; $f = 960\text{ MHz}$.



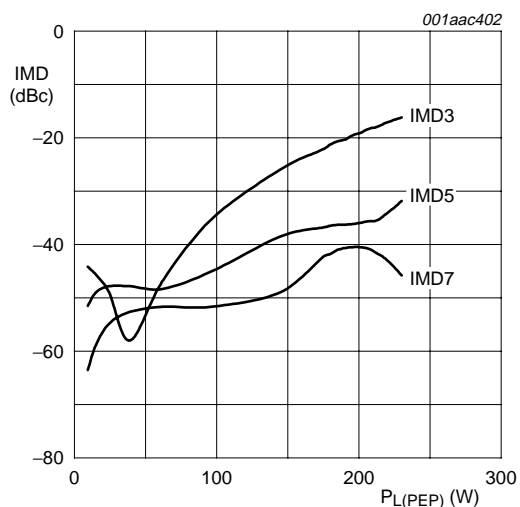
$V_{DS} = 28 \text{ V}$; $I_{Dq} = 850 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$;
 $f = 960 \text{ MHz}$

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



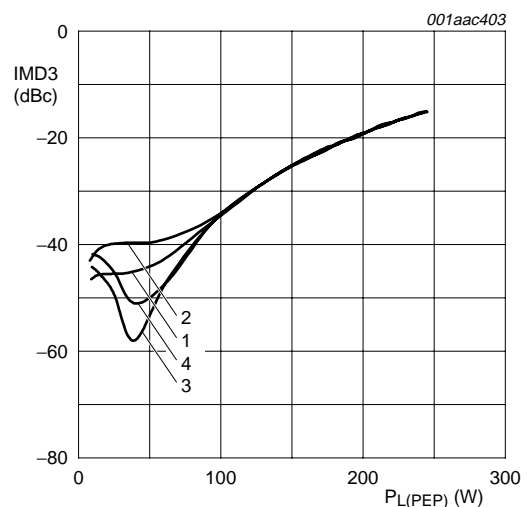
$V_{DS} = 28 \text{ V}$; $I_{Dq} = 850 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$;
 $f = 960 \text{ MHz}$

Fig 2. Two-tone CW power gain and drain efficiency as functions of peak envelope load power; typical values



$V_{DS} = 28 \text{ V}$; $I_{Dq} = 850 \text{ mA}$; $T_{case} = 25 \text{ }^\circ\text{C}$;
 $f = 960 \text{ MHz}$

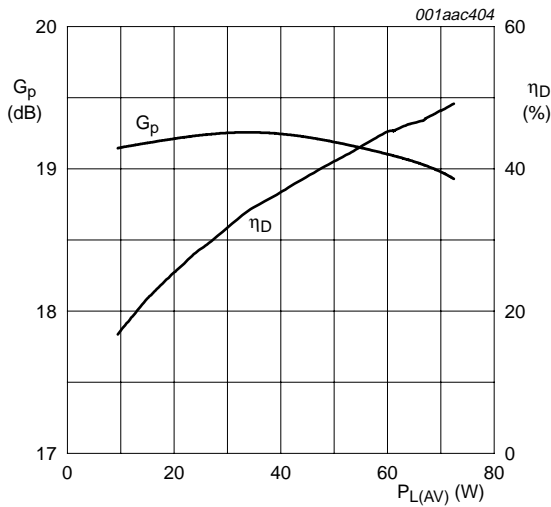
Fig 3. Intermodulation distortion as a function of peak envelope load power; typical values



$V_{DS} = 28 \text{ V}$; $T_{case} = 25 \text{ }^\circ\text{C}$; $f = 960 \text{ MHz}$

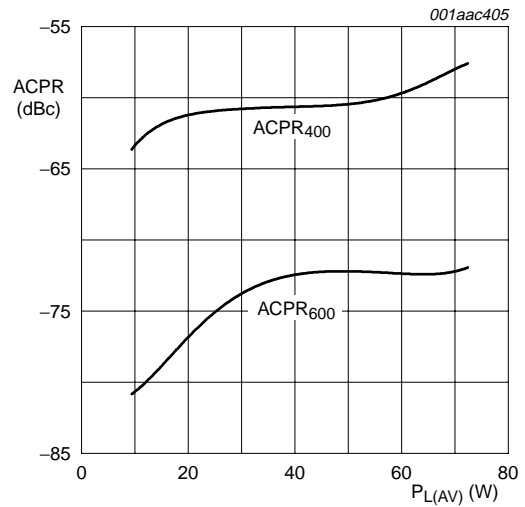
- (1) $I_{Dq} = 650 \text{ mA}$
- (2) $I_{Dq} = 750 \text{ mA}$
- (3) $I_{Dq} = 850 \text{ mA}$
- (4) $I_{Dq} = 950 \text{ mA}$

Fig 4. Third order intermodulation distortion as a function of peak envelope load power; typical values



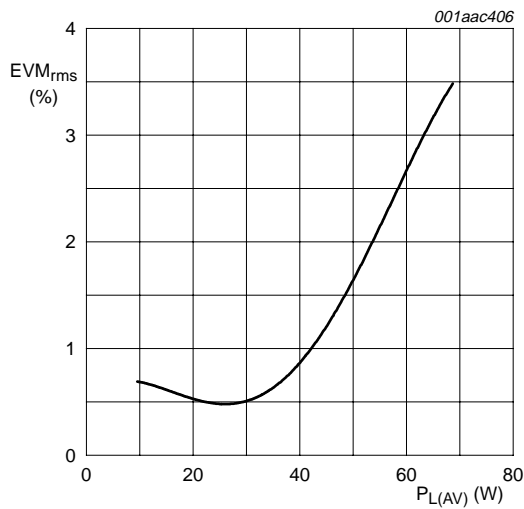
$V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 960\text{ MHz}$

Fig 5. GSM EDGE power gain and drain efficiency as functions of average load power; typical values



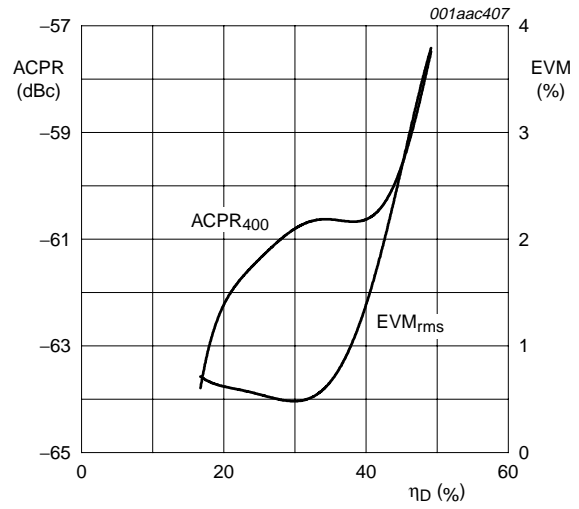
$V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 960\text{ MHz}$

Fig 6. GSM EDGE ACPR at 400 kHz and at 600 kHz as functions of average load power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 960\text{ MHz}$

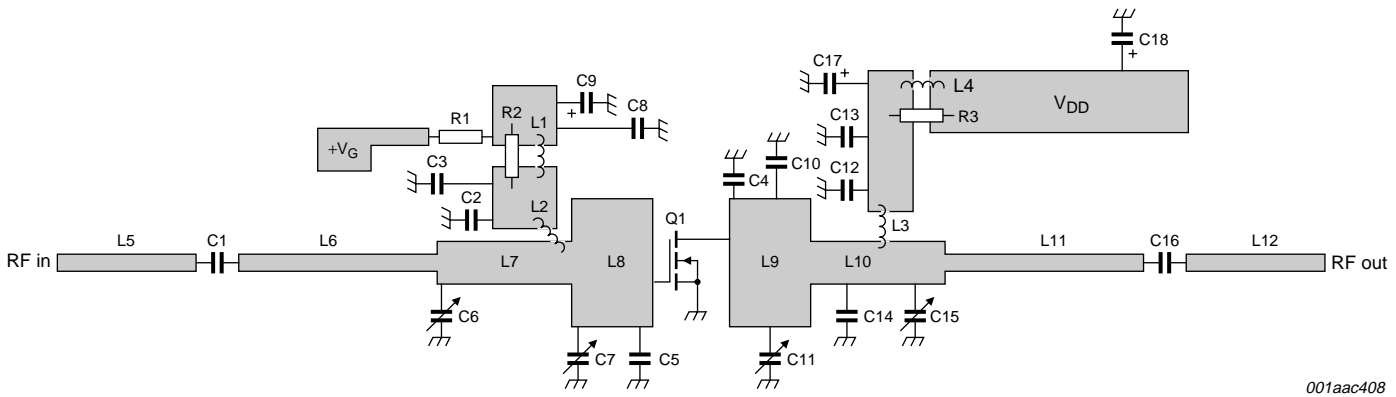
Fig 7. GSM EDGE rms EVM as a function of average load power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 850\text{ mA}$; $T_{case} = 25\text{ }^\circ\text{C}$;
 $f = 960\text{ MHz}$

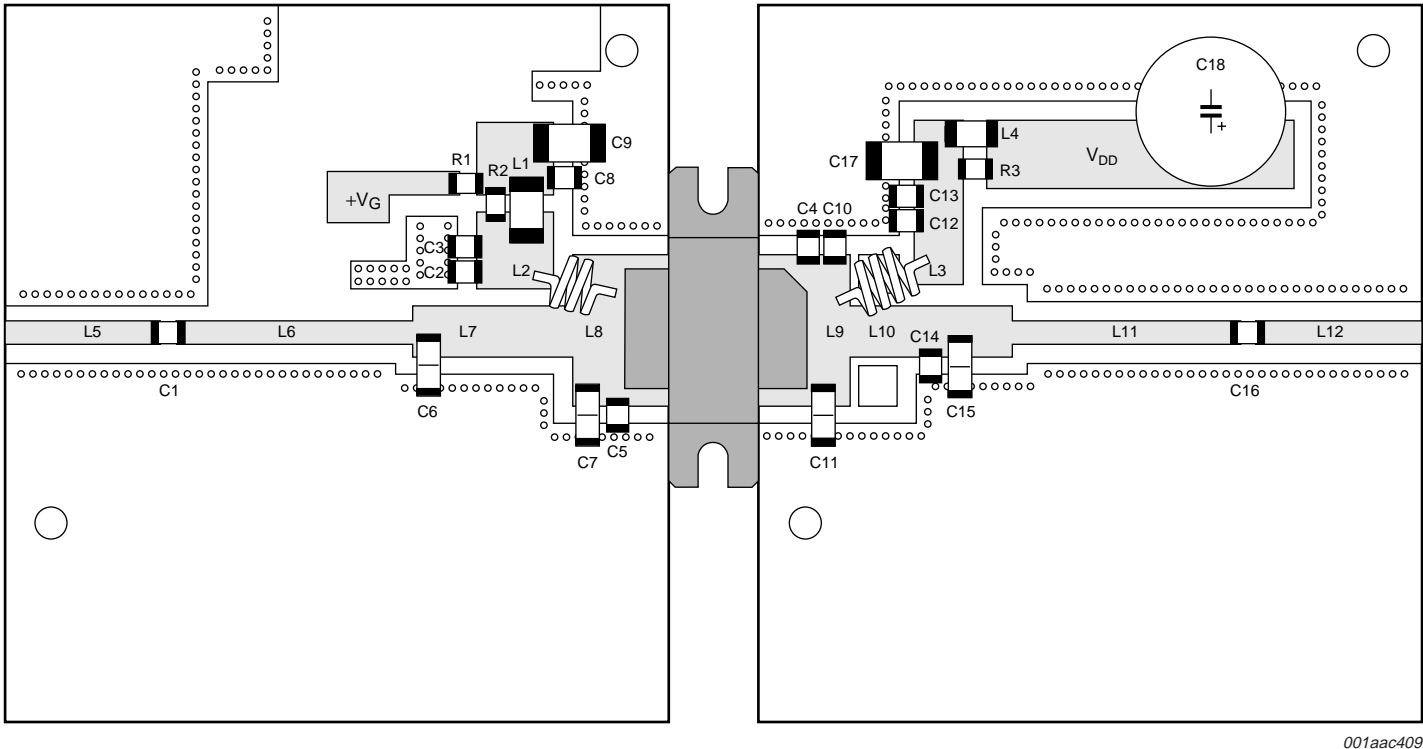
Fig 8. GSM EDGE ACPR at 400 kHz and rms EVM as functions of drain efficiency; typical values

8. Test information



001aac408

See [Table 8](#) for list of components.**Fig 9.** Class-AB test circuit for operation at 960 MHz



001aac409

The components are situated on one side of the copper-clad Printed-Circuit Board (PCB) with Duroid dielectric ($\epsilon_r = 2.5$), thickness 31 mils.

The other side is unetched and serves as a ground plane.

See [Table 8](#) for list of components.

Fig 10. Component layout for 960 MHz test circuit

Table 8: List of components (see Figure 9 and Figure 10)

Component	Description	Value	Dimensions
C1	multilayer ceramic chip capacitor	[1] 30 pF	
C2, C12	multilayer ceramic chip capacitor	[1] 47 pF	
C3, C13	multilayer ceramic chip capacitor	[1] 300 pF	
C4	multilayer ceramic chip capacitor	[1] 6.2 pF	
C5	multilayer ceramic chip capacitor	[1] 7.5 pF	
C6, C7, C11, C15	trimmer capacitors (Tekelec)	[2] 0.8 pF to 8 pF	
C8	multilayer ceramic chip capacitor	20 nF	
C9	tantalum capacitor	10 μ F; 35 V	
C10	multilayer ceramic chip capacitor	[1] 6.8 pF	
C14	multilayer ceramic chip capacitor	[1] 5.1 pF	
C16	multilayer ceramic chip capacitor	[1] 56 pF	
C17	tantalum capacitor	[3] 10 μ F; 35 V	
C18	electrolytic capacitor	220 μ F; 63 V	
L1	ferrite bead (long)	grade 4S2	
L2	3 turn inductor ID 4.5 mm, Cu-wire diameter 1 mm		
L3	4 turn inductor ID 3 mm, Cu-wire diameter 1 mm		
L4	ferrite bead (short)	grade 4S2	
L5	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 2 mm \times 17.2 mm
L6	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 2 mm \times 25.4 mm
L7	stripline	[4] $Z_0 = 25 \Omega$	(W \times L) 5.6 mm \times 17.4 mm
L8	stripline	[4] $Z_0 = 10 \Omega$	(W \times L) 16 mm \times 10.2 mm
L9	stripline	[4] $Z_0 = 10 \Omega$	(W \times L) 16 mm \times 10.2 mm
L10	stripline	[4] $Z_0 = 25 \Omega$	(W \times L) 5.6 mm \times 17.4 mm
L11	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 2 mm \times 25.4 mm
L12	stripline	[4] $Z_0 = 50 \Omega$	(W \times L) 2 mm \times 17.2 mm
R1	SMD resistor	8.2 Ω ; 0.1 W	
R2	SMD resistor	4.7 Ω ; 0.1 W	
R3	metal film resistor	10 Ω ; 0.6 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Mounted flat.

[3] Low ESR.

[4] Striplines are on a double copper-clad Ultralam 2000 PCB ($\epsilon_r = 2.5$); thickness = 31 mils.

9. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A

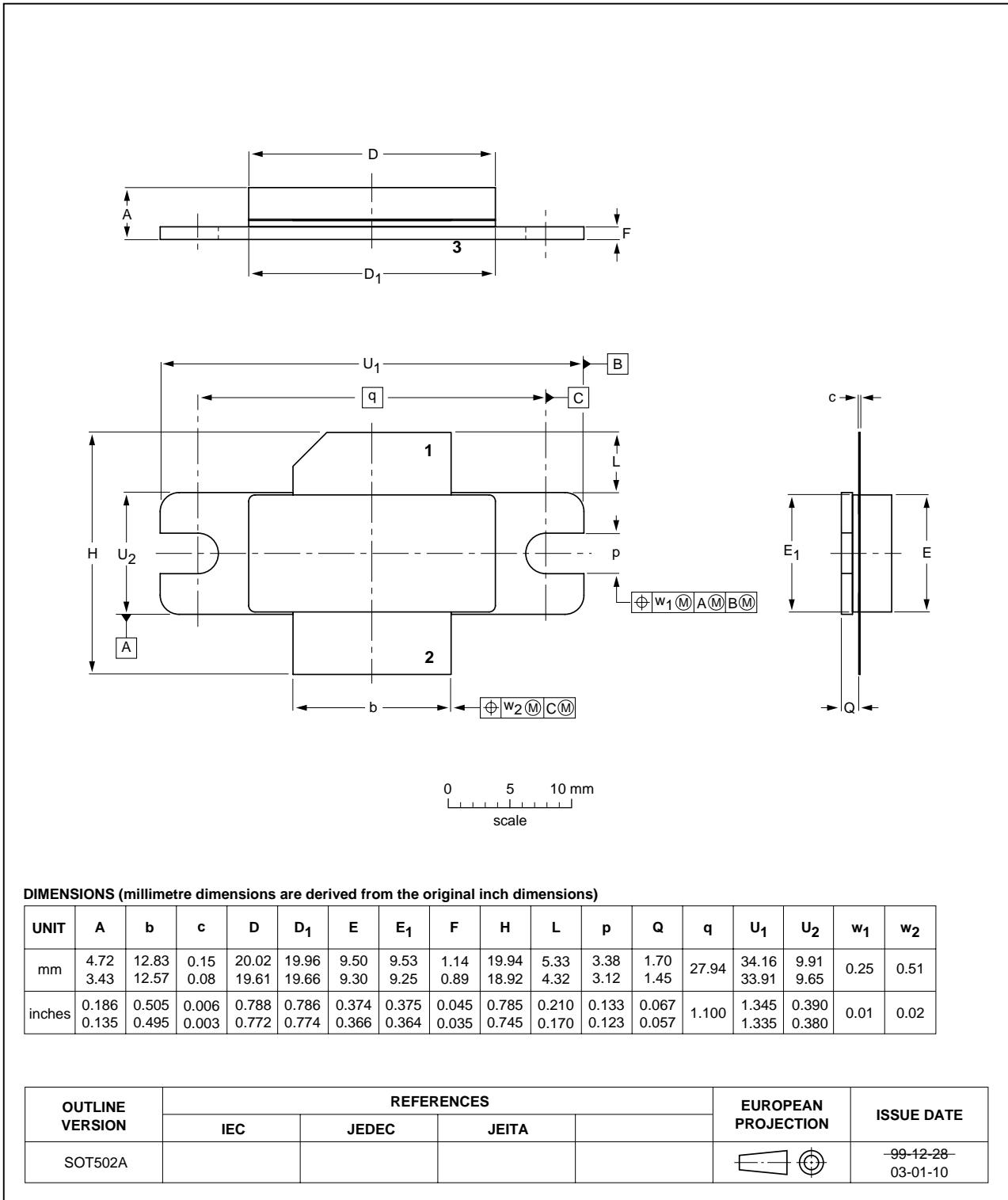


Fig 11. Package outline SOT502A

Earless flanged LDMOST ceramic package; 2 leads

SOT502B

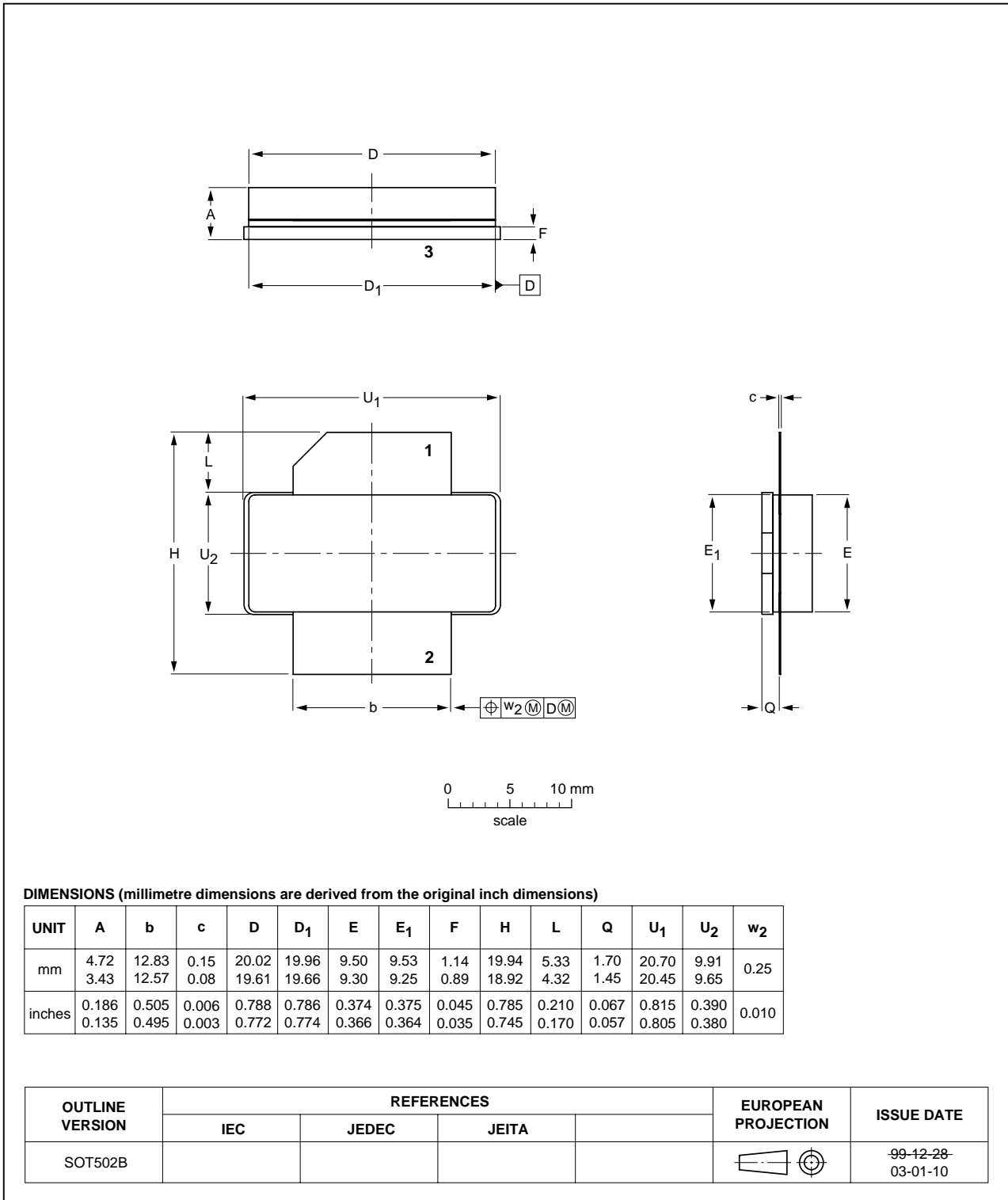


Fig 12. Package outline SOT502B

10. Abbreviations

Table 9: Abbreviations

Acronym	Description
ACPR	Adjacent Channel Power Ratio
CDMA	Code Division Multiple Access
CW	Continuous Wave
EDGE	Enhanced Data rates for GSM Evolution
ESR	Equivalent Series Resistance
EVM	Error Vector Magnitude
GSM	Global System for Mobile communications
I_{Dq}	quiescent drain current
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PEP	Peak Envelope Power
RF	Radio Frequency
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 10: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
BLF4G10-120_ 4G10S-120_1	20060110	Product data sheet	-	9397 750 14549	-

12. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2] [3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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