

BLF6G10L-40BRN

Power LDMOS transistor

Rev. 01 — 9 August 2010

Preliminary data sheet

1. Product profile

1.1 General description

40 W LDMOS power transistor for base station applications at frequencies from 700 MHz to 1 GHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a class-AB production test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR (dBc)
2-carrier W-CDMA ^[1]	791 to 821	28	2.5	23.0	15.0	-42.5

[1] Test signal: 3GPP test model 1; 1 to 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical 2-carrier W-CDMA performance at frequencies of 791 MHz and 821 MHz, a supply voltage of 28 V and an I_{DQ} of 360 mA:
 - ◆ Average output power (P_{L(AV)}) = 2.5 W
 - ◆ Power gain (G_p) = 23.0 dB
 - ◆ Drain efficiency (η_D) = 15.0 %
 - ◆ ACPR = -42.5 dBc
- Easy power control
- Integrated ESD protection
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (728 MHz to 960 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)
- Integrated current sense

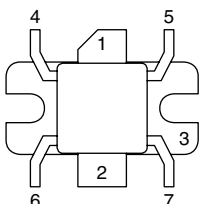
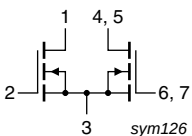


1.3 Applications

RF power amplifiers for W-CDMA base stations and multi-carrier GSM and LTE applications in the 728 MHz to 960 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF6G10L-40BRN (SOT1112A)			
1	drain		
2	gate		
3	source		
4, 5	sense drain		
6, 7	sense gate		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G10L-40BRN	-	flanged ceramic package; 2 mounting holes; 6 leads	SOT1112A

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+11	V
$V_{GS(sense)}$	sense gate-source voltage		-0.5	+9	V
I_D	drain current		-	11	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	200	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 2.5\text{ W (CW)}$	1.7	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$ per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 0.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 59\text{ mA}$	1.4	1.9	2.4	V
I_{Dq}	quiescent drain current	sense transistor: $I_{DS} = 8.2\text{ mA}$, $V_{DS} = 26.5\text{ V}$; main transistor: $V_{DS} = 28\text{ V}$	280	360	420	mA
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	8.8	10	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 2.9\text{ A}$	2.7	4.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 2.1\text{ A}$	0.09	0.25	0.39	Ω

7. Application information

Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH; $f_1 = 788.5$ MHz; $f_2 = 793.5$ MHz; $f_3 = 818.5$ MHz; $f_4 = 823.5$ MHz; RF performance at $V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $T_{case} = 25$ °C; unless otherwise specified in a class AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	2.5	-	W
G_p	power gain	$P_{L(AV)} = 2.5$ W	22.2	23.0	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 2.5$ W	11	15	-	dB
η_D	drain efficiency	$P_{L(AV)} = 2.5$ W	14	15	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 2.5$ W	-	-42.5	-41	dBc

Table 8. Application information

Mode of operation; 1 carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1 to 64 DPCH; $f_1 = 821$ MHz; RF performance at $V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $T_{case} = 25$ °C; unless otherwise specified in a class AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR	peak-to-average ratio	$P_{L(AV)} = 10$ W at 0.01 % probability on CCDF	5.5	5.9	-	dB

7.1 Ruggedness in class-AB operation

The BLF6G10L-40BRN is capable of withstanding a load mismatch corresponding to $VSWR = 1 : 10$ through all phases under the following conditions: $V_{DS} = 28$ V; $I_{Dq} = 360$ mA; $P_L = 40$ W; $f = 791$ MHz and 821 MHz.

7.2 Impedance information

Table 9. Typical impedance per section

$I_{Dq} = 360$ mA; main transistor $V_{DS} = 28$ V.

f (MHz)	$Z_S^{[1]}$ (Ω)	$Z_L^{[1]}$ (Ω)
800	$2.0 - j5.0$	$5.3 + j2.9$
810	$2.0 - j5.5$	$5.6 + j2.3$

[1] Z_S and Z_L are defined in [Figure 1](#).

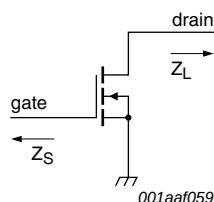
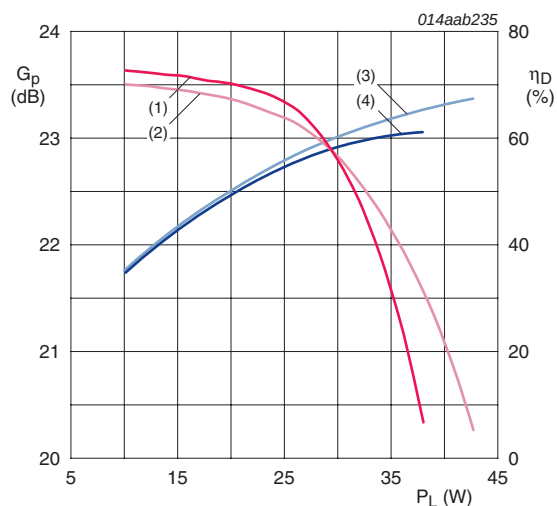


Fig 1. Definition of transistor impedance

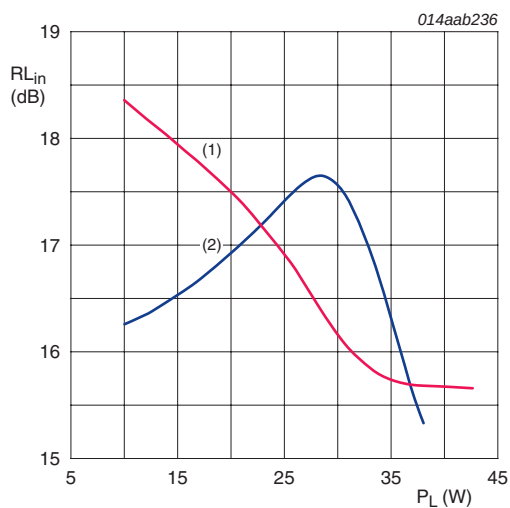
7.3 Typical power sweep

7.3.1 CW



- (1) dB power gain at 791 MHz.
- (2) dB power gain at 821 MHz.
- (3) % drain efficiency at 821 MHz.
- (4) % drain efficiency at 791 MHz.

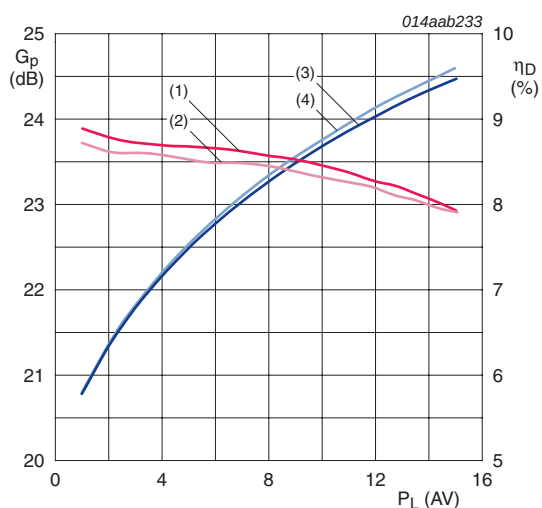
Fig 2. Typical continuous wave: power gain and drain efficiency as a function of output power



- (1) dB return loss at 821 MHz.
- (2) dB return loss at 791 MHz.

Fig 3. Typical continuous wave: input return loss as a function of output power

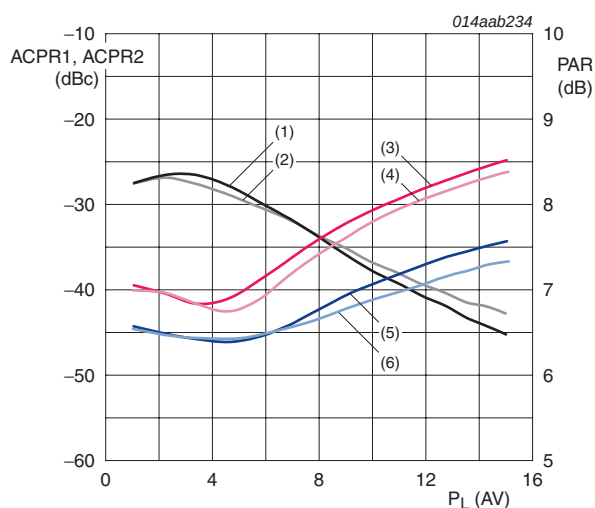
7.3.2 2-carrier W-CDMA (5 MHz spacing)



- (1) dB power gain at 791 MHz.
- (2) dB power gain at 821 MHz.
- (3) % drain efficiency at 791 MHz.
- (4) % drain efficiency at 821 MHz.

a. Power gain and drain efficiency as a function of average output power

3GPP test model 1; 1 to 64 DPCH; PAR = 7.5 dB at 0.01% probability per carrier; 5 MHz carrier spacing.



- (1) dB PAR at 791 MHz.
- (2) dB PAR at 821 MHz.
- (3) 5 MHz ACPR, dBc at 791 MHz.
- (4) 5 MHz ACPR, dBc at 821 MHz.
- (5) 10 MHz ACPR, dBc at 791 MHz.
- (6) 10 MHz ACPR, dBc at 821 MHz.

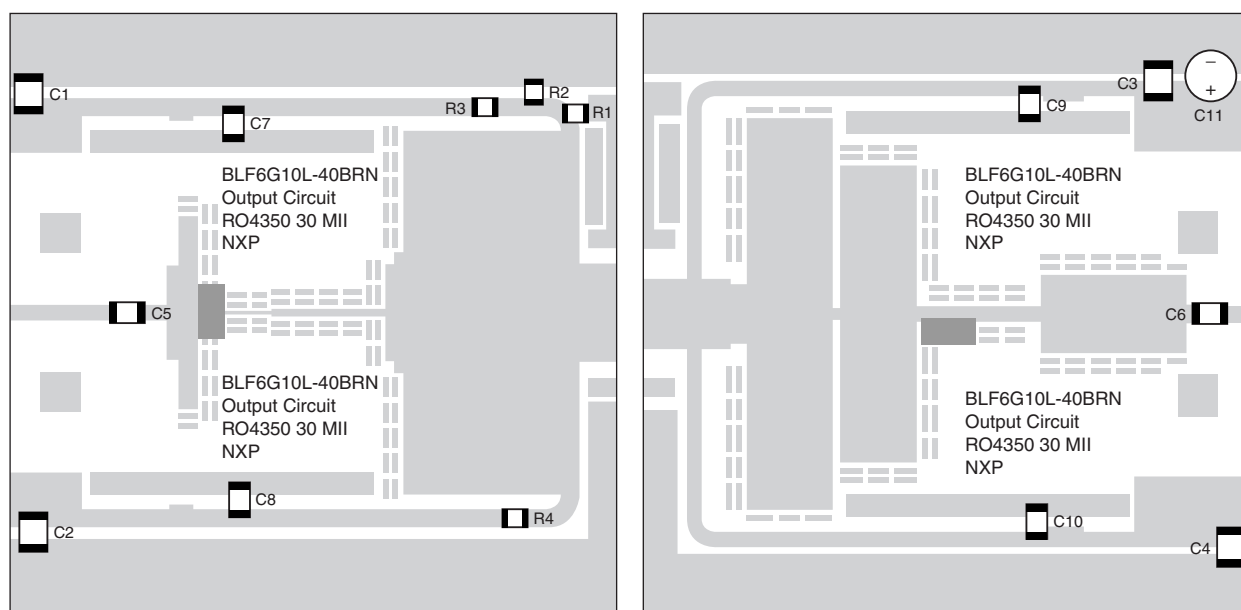
b. ACPR, and PAR as a function of average output power

Fig 4. Typical 2-carrier W-CDMA: power gain, drain efficiency and ACPR as a function of average output power

8. Test information

8.1 Test circuit

The PCB test circuit layout is shown in [Figure 5](#).



014aab232

When placing components, it is possible to use the vias as a reference.

The above layout shows the test circuit used to measure the devices in production. A more appropriate application demonstration for specific customer needs can be obtained from the RF Power and Base station group.

Fig 5. Input and output test circuit PCBs

8.2 Bill of materials (BOM)

A list of all the components needed to build the RF test circuit is shown in [Table 10](#).

Table 10. Bill of materials

Component	Description	Type	Value	Code number	Remarks
C1, C2, C3, C4	multi-layer ceramic chip capacitor	MURATA	10 μ F	-	-
C5, C6	multi-layer ceramic chip capacitor	ATC100B	47 pF	-	-
C7, C8	multi-layer ceramic chip capacitor	ATC100B	100 pF	-	-
C9, C10	multi-layer ceramic chip capacitor	ATC100B	30 pF	-	-
C11	electrolytic capacitor	-	470 μ F; 63 V	-	-
R1	chip resistor	Philips 1206	820 Ω	-	-
R2	chip resistor	Philips 1206	2.2 k Ω	-	-
R3, R4	chip resistor	Philips 1206	15 Ω	-	-
-	N-connector female	23N-50-057/1	-	-	Suhner
-	N-connector male	13N-50-057/1	-	-	Suhner
-	2 $\times$ contact block	-	6 $\times$ 5 mm	-	brass (milled)
-	2 $\times$ contact block	-	2.5 $\times$ 2.5 mm	-	brass (milled)
-	DC-connector 8 pin male	8140-115	-	-	Souriau (Farnell)
-	2 $\times$ DC-connector 2 pin male	8140-12	-	-	Souriau (Farnell)
-	solid copper wire (1 mm diameter)	-	30 mm	-	-
-	flexible copper wire	SIMX-F	0.75 mm ²	-	silicon isolated
-	input PCB	-	-	-	see PCB information
-	output PCB	-	-	-	see PCB information
-	8 $\times$ washer M2	-	-	-	brass (nickel plated)
-	14 $\times$ bolt M2	-	5 mm	-	brass (nickel plated)
-	4 $\times$ bolt M3	-	12 mm	-	chrome nickel steel
-	2 $\times$ bolt M3	-	30 mm	-	chrome nickel steel
-	2 $\times$ washer M3	-	-	-	chrome nickel steel
-	4 $\times$ spring washer M3	-	-	-	chrome nickel steel
-	10 $\times$ isolated paper washer M2	-	-	-	paper
-	auto bias ^[1]	28 V/I _{DS} = 8.2 mA	-	-	-
-	base plate ^[2]	-	-	-	-

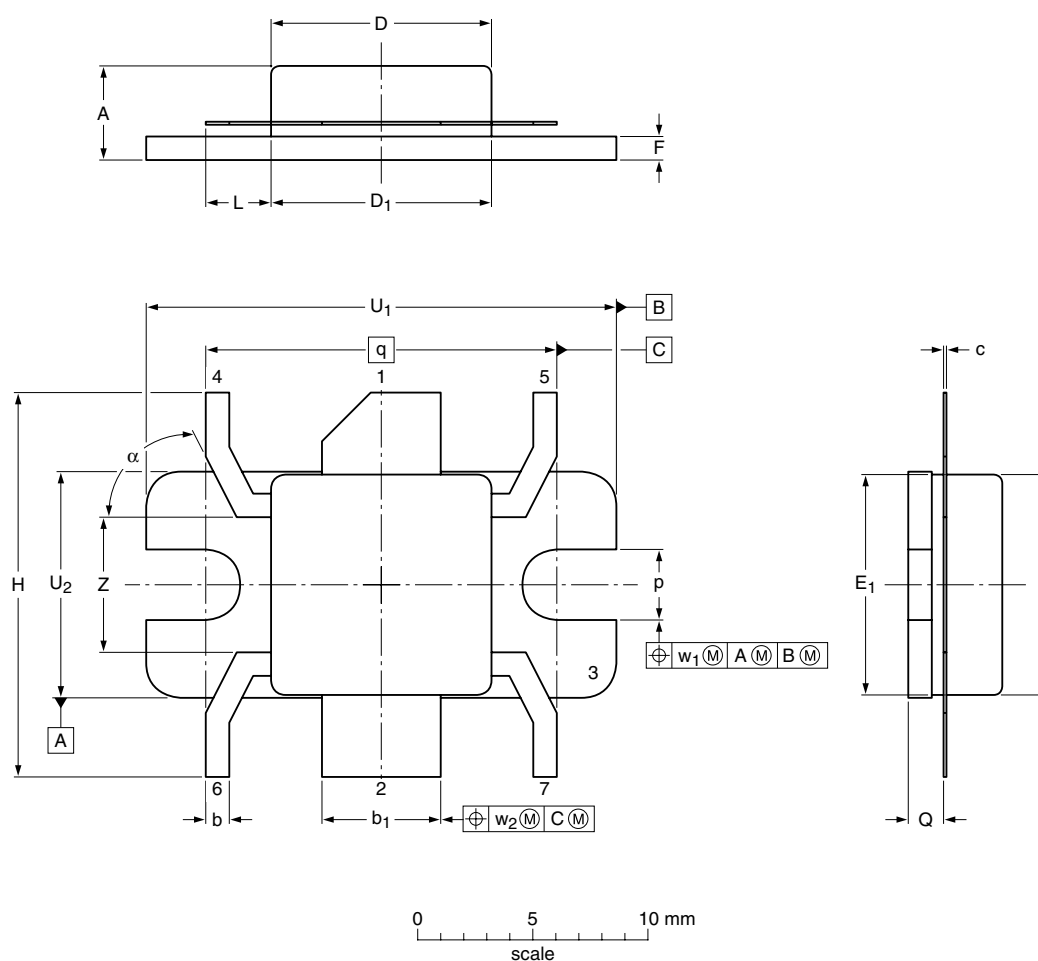
[1] Auto bias documentation available on request from RF Power and Base station group, NXP Semiconductors.

[2] Base plate mechanical drawing available on request from RF Power and Base station group, NXP Semiconductors.

9. Package outline

Flanged ceramic package; 2 mounting holes; 6 leads

SOT1112A



Dimensions

Unit ⁽¹⁾	A	b	b ₁	c	D	D ₁	E	E ₁	F	H	L	p	Q ⁽²⁾	q	U ₁	U ₂	w ₁	w ₂	Z	α
mm	max	4.65	1.14	5.26	0.18	9.65	9.65	9.65	9.65	1.14	17.12	3.00	3.30	1.70	20.45	9.91			5.97	64°
	nom													15.24			0.25	0.51		
	min	3.76	0.89	5.00	0.10	9.40	9.40	9.40	9.40	0.89	16.10	2.69	2.92	1.45	20.19	9.65			5.72	62°
inches	max	0.183	0.045	0.207	0.007	0.38	0.38	0.38	0.38	0.045	0.674	0.118	0.130	0.067	0.805	0.39			0.235	64°
	nom													0.6			0.01	0.02		
	min	0.148	0.035	0.197	0.004	0.37	0.37	0.37	0.37	0.035	0.634	0.106	0.115	0.057	0.795	0.38			0.225	62°

Note

1. millimeter dimensions are derived from the original inch dimensions.

2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1112a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1112A						-09-10-12- 10-02-02

Fig 6. Package outline SOT1112A

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LTE	Long Term Evolution
PAR	Peak-to-Average power Ratio
RF	Radio Frequency
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G10L-40BRN v.1	20100809	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

12.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

12.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

13. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	2
2	Pinning information	2
3	Ordering information	2
4	Limiting values	3
5	Thermal characteristics	3
6	Characteristics	3
7	Application information	4
7.1	Ruggedness in class-AB operation	4
7.2	Impedance information	4
7.3	Typical power sweep	5
7.3.1	CW	5
7.3.2	2-carrier W-CDMA (5 MHz spacing)	6
8	Test information	7
8.1	Test circuit	7
8.2	Bill of materials (BOM)	8
9	Package outline	9
10	Abbreviations	10
11	Revision history	10
12	Legal information	11
12.1	Data sheet status	11
12.2	Definitions	11
12.3	Disclaimers	11
12.4	Trademarks	12
13	Contact information	12
14	Contents	13

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2010.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 August 2010

Document identifier: BLF6G10L-40BRN