BLF6G20LS-140

Power LDMOS transistor

Rev. 01 — 27 February 2009 Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for base station applications at frequencies from 1800 MHz to 2000 MHz.

Table 1. Typical performance

RF performance at T_{case} = 25 °C in a common source class-AB production test circuit.

Mode of operation	f	V_{DS}	$P_{L(AV)}$	G_p	η_D	IMD3	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)	(dBc)
2-carrier W-CDMA	1930 to 1990	28	35.5	16.5	30	–37[1]	–40[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7 dB at 0.01 % probability on CCDF per carrier; carrier spacing 10 MHz.

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features

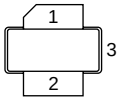
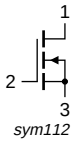
- Typical 2-carrier W-CDMA performance at frequencies of 1930 MHz and 1990 MHz, a supply voltage of 28 V and an I_{Dq} of 1000 mA:
  - Average output power = 35.5 W
  - Power gain = 16.5 dB (typ)
  - Efficiency = 30 %
  - IMD3 = –37 dBc
  - ACPR = –40 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1800 MHz to 2000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for GSM, GSM EDGE, W-CDMA and CDMA base stations and multi carrier applications in the 1800 MHz to 2000 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphical symbol
1	drain		
2	gate		
3	source [1]		

sym112

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G20LS-140	-	earless flanged LDMOST ceramic package; 2 leads	SOT502B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		–0.5	+13	V
I_D	drain current		-	39	A
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j\text{-}case)}$	thermal resistance from junction to case	T_{case} = 80 °C; P_L = 35 W	0.49	K/W

6. Characteristics

Table 6. Characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.5 mA	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 216 mA	1.4	2	2.4	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_D = 1000 mA	1.53	2	2.53	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 28 V	-	-	5	µA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	31	39	-	A
I_{GSS}	gate leakage current	V_{GS} = 13 V; V_{DS} = 0 V	-	-	450	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 10.8 A	9.7	13.5	15	S
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 7.56 A	-	0.07	-	Ω
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 28 V; f = 1 MHz	-	3.57	-	pF

7. Application information

Table 7. Application information

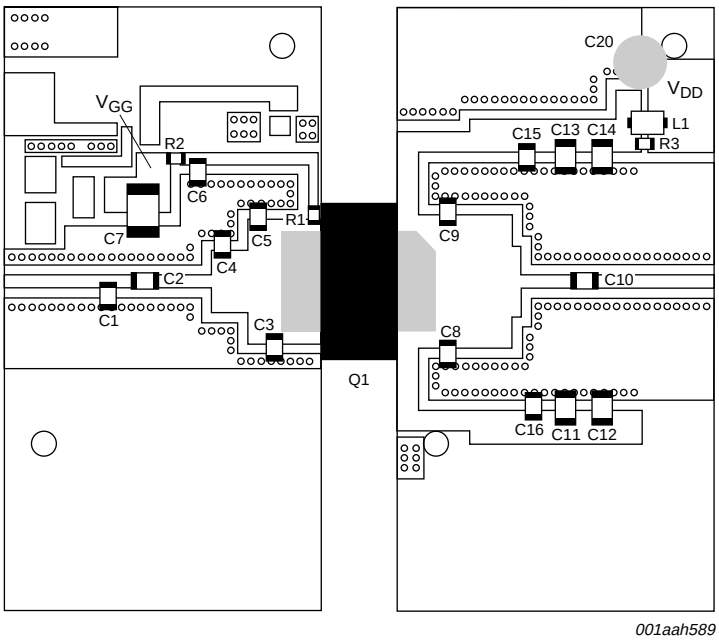
Mode of operation: 2-carrier W-CDMA; PAR 7 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 PDPCH; f_1 = 1932.5 MHz; f_2 = 1942.5 MHz; f_3 = 1977.5 MHz; f_4 = 1987.5 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 1000 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	35.5	-	W
G_p	power gain	$P_{L(AV)}$ = 35.5 W	15.5	16.5	-	dB
RL_{in}	input return loss	$P_{L(AV)}$ = 35.5 W	-	8	5	dB
η_D	drain efficiency	$P_{L(AV)}$ = 35.5 W	27	30	-	%
IMD3	third order intermodulation distortion	$P_{L(AV)}$ = 35.5 W	-	–37	–35	dBc
ACPR	adjacent channel power ratio	$P_{L(AV)}$ = 35.5 W	-	–40	–38	dBc

7.1 Ruggedness in class-AB operation

The BLF6G20LS-140 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 1000 mA; P_L = 140 W (CW); f = 1990 MHz.

8. Test information



The striplines are on a double copper-clad Taconic RF35 Printed-Circuit Board (PCB) with ε_r = 3.5 and thickness = 0.76 mm. See Table 8 for list of components.

Fig 1. Component layout

Table 8. List of components (see Figure 1)

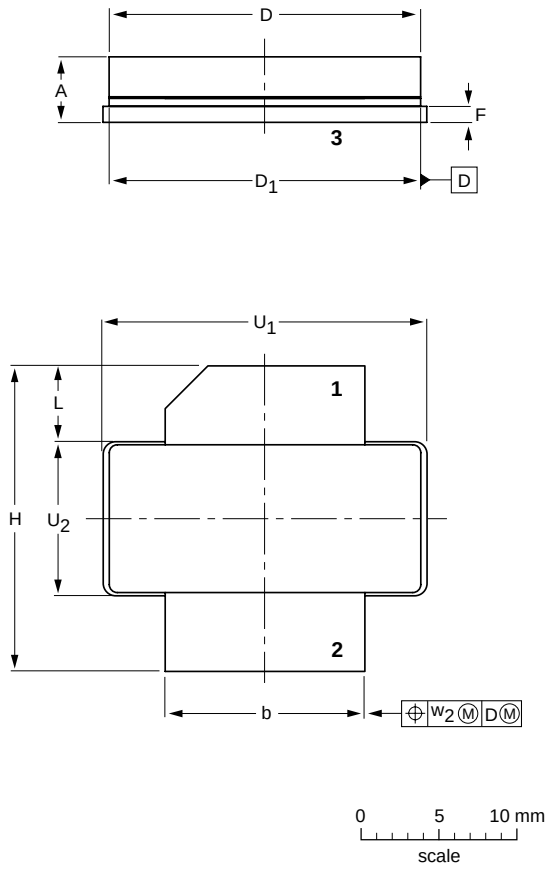
Component	Description	Value		Remarks
C1	multilayer ceramic chip capacitor	0.5 pF	[1]	
C2	multilayer ceramic chip capacitor	10 pF	[2]	
C3	multilayer ceramic chip capacitor	0.9 pF	[2]	
C4	multilayer ceramic chip capacitor	1.1 pF	[2]	
C5	multilayer ceramic chip capacitor	1.4 pF	[2]	
C6	multilayer ceramic chip capacitor	15 pF	[2]	
C7	multilayer ceramic chip capacitor	10 µF; 50 V		TDK C5750X7R1H106M or equivalent
C8, C9	multilayer ceramic chip capacitor	1.2 pF	[2]	
C10	multilayer ceramic chip capacitor	13 pF	[2]	
C11, C12, C13, C14	multilayer ceramic chip capacitor	4.7 µF; 50 V		TDK C4532X7R1H475M or equivalent
C20	electrolytic capacitor	220 µF; 35 V		
L1	ferrite SMD bead	-		Ferroxcube BDS 3/3/8.9-4S2 or equivalent
Q1	BLF6G20LS-140	-		
R1	SMD resistor	0 Ω		
R2	SMD resistor	3.3 kΩ		
R3	SMD resistor	9.1 Ω		

[1] American Technical Ceramics type 100A or capacitor of same quality.

[2] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

Earless flanged LDMOST ceramic package; 2 leads **SOT502B**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	w_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT502B						~~03-01-10~~ 07-05-09

Fig 2. Package outline SOT502B

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	Third Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CDMA	Code Division Multiple Access
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
EDGE	Enhanced Data rates for GSM Evolution
GSM	Global System for Mobile communications
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G20LS-140_1	20090227	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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