# BLF7G24L-160P; BLF7G24LS-160P

**Power LDMOS transistor**

AMPLEON

Rev. 6 — 1 September 2015

**Product data sheet**

## 1. Product profile

### 1.1 General description

160 W LDMOS power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

**Table 1. Typical performance**

*Typical RF performance at $T_{case}$ = 25 °C in a common source class-AB production test circuit.*

| Test signal | f (MHz) | $I_{Dq}$ (mA) | $V_{DS}$ (V) | $P_{L(AV)}$ (W) | $G_p$ (dB) | $\eta_D$ (%) | $ACPR_{885k}$ (dBc) |
|---|---|---|---|---|---|---|---|
| IS-95 | 2300 to 2400 | 1200 | 28 | 30 | 18.5 | 27.5 | –45.5[1] |

[1] Single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF. Channel bandwidth is 1.2288 MHz.

### 1.2 Features and benefits

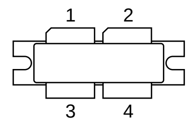
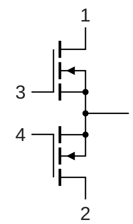
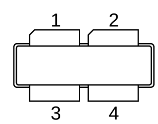
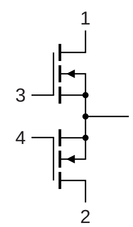
- Excellent ruggedness
- High efficiency
- Low $R_{th}$ providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range

## 2. Pinning information

**Table 2. Pinning**

| Pin | Description | Simplified outline | Graphic symbol |
|---|---|---|---|
| **BLF7G24L-160P (SOT539A)** | | | |
| 1 | drain1 |  |  sym117 |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source [1] | | |
| **BLF7G24LS-160P (SOT539B)** | | | |
| 1 | drain1 |  |  sym117 |
| 2 | drain2 | | |
| 3 | gate1 | | |
| 4 | gate2 | | |
| 5 | source [1] | | |

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BLF7G24L-160P | - | flanged balanced ceramic package; 2 mounting holes; 4 leads | SOT539A |
| BLF7G24LS-160P | - | earless flanged balanced ceramic package; 4 leads | SOT539B |

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | | - | 65 | V |
| $V_{GS}$ | gate-source voltage | | –0.5 | +13 | V |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $T_j$ | junction temperature | | - | 200 | °C |

# 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $R_{th(j-c)}$ | thermal resistance from junction to case | $T_{case}$ = 80 °C; $P_L$ = 30 W; $V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA | 0.2 | K/W |

# 6. Characteristics

**Table 6. Characteristics**

*$T_j$ = 25 °C per section, unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $V_{GS}$ = 0 V; $I_D$ = 1 mA | 65 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $V_{DS}$ = 10 V; $I_D$ = 102 mA | 1.5 | 1.9 | 2.3 | V |
| $I_{DSS}$ | drain leakage current | $V_{GS}$ = 0 V; $V_{DS}$ = 28 V | - | - | 2.8 | μA |
| $I_{DSX}$ | drain cut-off current | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $V_{DS}$ = 10 V | - | 19 | - | A |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 11 V; $V_{DS}$ = 0 V | - | - | 280 | nA |
| $g_{fs}$ | forward transconductance | $V_{DS}$ = 10 V; $I_D$ = 3.57 A | - | 6.9 | - | S |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS}$ = $V_{GS(th)}$ + 3.75 V; $I_D$ = 3.57 A | - | 0.15 | 0.23 | Ω |

# 7. Test information

**Remark:** All testing performed in a class-AB production test circuit.

**Table 7. Functional test information**

*Test signal: single carrier IS-95 with pilot, paging, sync and 6 traffic channels (Walsh codes 8 - 13). PAR = 9.7 dB at 0.01 % probability on the CCDF, channel bandwidth is 1.2288 MHz; $f_1$ = 2300 MHz; $f_2$ = 2400 MHz; RF performance at $V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA; $T_{case}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $G_p$ | power gain | $P_{L(AV)}$ = 30 W | 17.8 | 18.5 | - | dB |
| $RL_{in}$ | input return loss | $P_{L(AV)}$ = 30 W | - | −13.5 | −9 | dB |
| $\eta_D$ | drain efficiency | $P_{L(AV)}$ = 30 W | 25 | 27.5 | - | % |
| $ACPR_{885k}$ | adjacent channel power ratio (885 kHz) | $P_{L(AV)}$ = 30 W | - | −45.5 | −41.5 | dBc |

## 7.1 Ruggedness in class-AB operation

The BLF7G24L-160P and BLF7G24LS-160P are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA; $P_L$ = 160 W; f = 2300 MHz.

## 7.2 Impedance information

**Table 8. Typical impedance**

*Measured load-pull data. Typical values per section.*
*$I_{Dq}$ = 600 mA; main transistor $V_{DS}$ = 28 V. $Z_S$ and $Z_L$ defined in Figure 1.*

| f (MHz) | $Z_S$ (Ω) | $Z_L$ (Ω) |
|---|---|---|
| 2300 | 2.5 – j5.9 | 3.1 – j4.3 |
| 2400 | 4.6 – j7.2 | 2.9 – j4.2 |

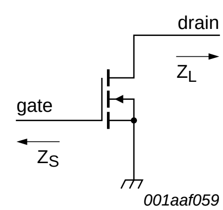
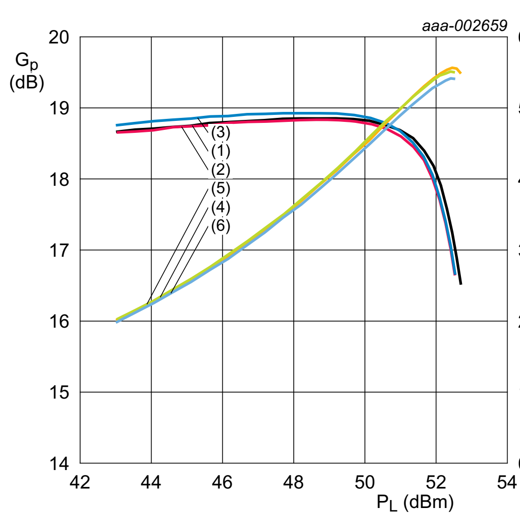



**Fig 1. Definition of transistor impedance**

## 7.3 Graphs

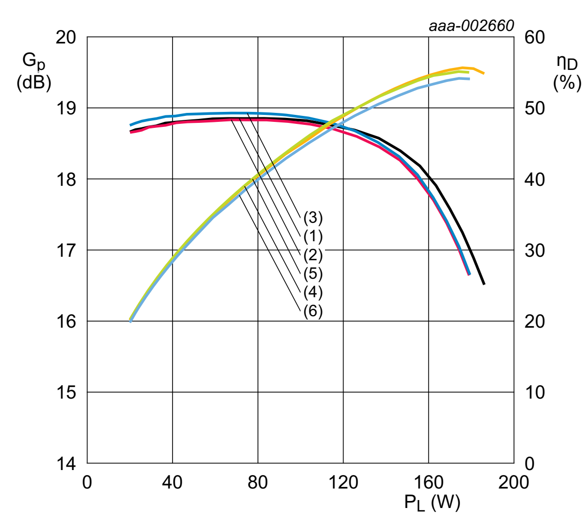
### 7.3.1 Pulsed CW




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA; δ = 10 %; $t_p$ = 0.10 ms.

(1) $G_p$ at f = 2300 MHz
(2) $G_p$ at f = 2350 MHz
(3) $G_p$ at f = 2400 MHz
(4) $\eta_D$ at f = 2300 MHz
(5) $\eta_D$ at f = 2350 MHz
(6) $\eta_D$ at f = 2400 MHz

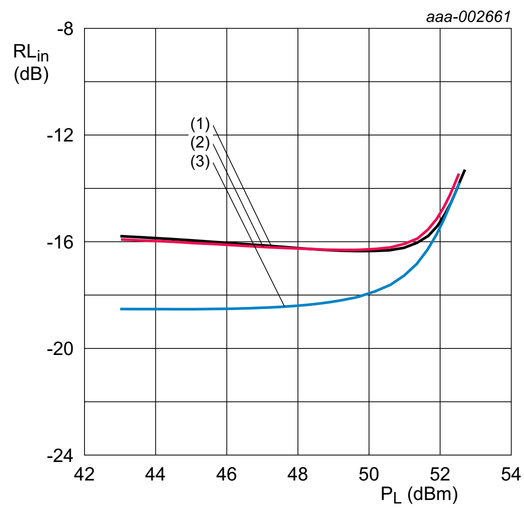
**Fig 2. Power gain and drain efficiency of pulsed CW as function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA; δ = 10 %; $t_p$ = 0.10 ms.

(1) $G_p$ at f = 2300 MHz
(2) $G_p$ at f = 2350 MHz
(3) $G_p$ at f = 2400 MHz
(4) $\eta_D$ at f = 2300 MHz
(5) $\eta_D$ at f = 2350 MHz
(6) $\eta_D$ at f = 2400 MHz

**Fig 3. Power gain and drain efficiency of pulsed CW as function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA; $\delta$ = 10 %; $t_p$ = 0.10 ms.

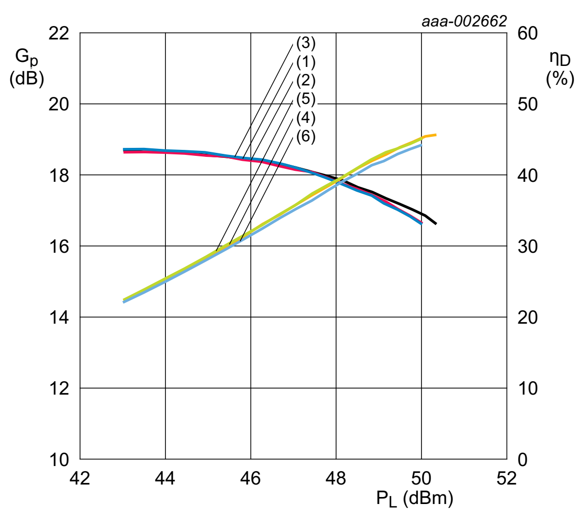
(1) f = 2300 MHz

(2) f = 2350 MHz

(3) f = 2400 MHz

**Fig 4. Input return loss of pulsed CW as a function of output power; typical values**

### 7.3.2 IS-95




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) $G_p$ at f = 2300 MHz

(2) $G_p$ at f = 2350 MHz

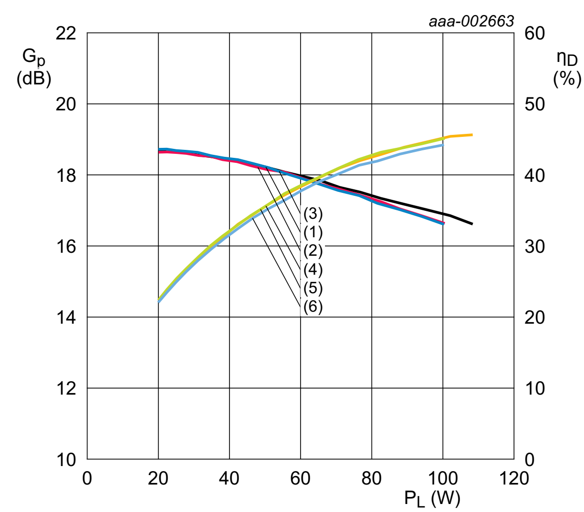
(3) $G_p$ at f = 2400 MHz

(4) $\eta_D$ at f = 2300 MHz

(5) $\eta_D$ at f = 2350 MHz

(6) $\eta_D$ at f = 2400 MHz

**Fig 5. Power gain and drain efficiency of IS-95 as function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) $G_p$ at f = 2300 MHz

(2) $G_p$ at f = 2350 MHz

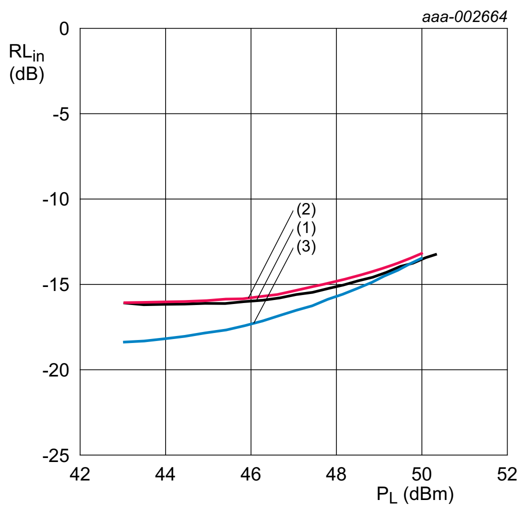
(3) $G_p$ at f = 2400 MHz

(4) $\eta_D$ at f = 2300 MHz

(5) $\eta_D$ at f = 2350 MHz

(6) $\eta_D$ at f = 2400 MHz

**Fig 6. Power gain and drain efficiency of IS-95 as function of output power; typical values**



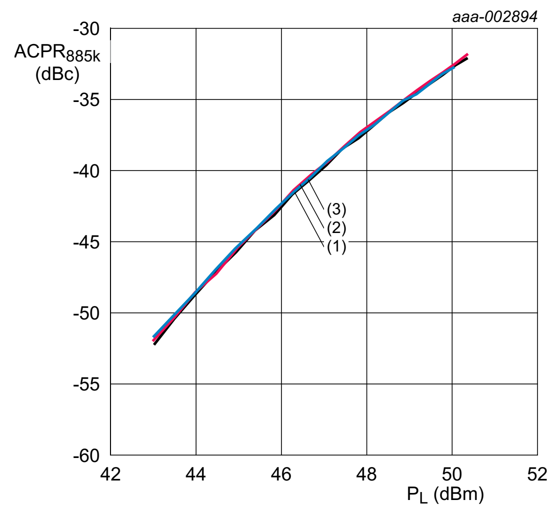

$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) f = 2300 MHz

(2) f = 2350 MHz

(3) f = 2400 MHz

**Fig 7. Input return loss of IS-95 as a function of output power; typical values**



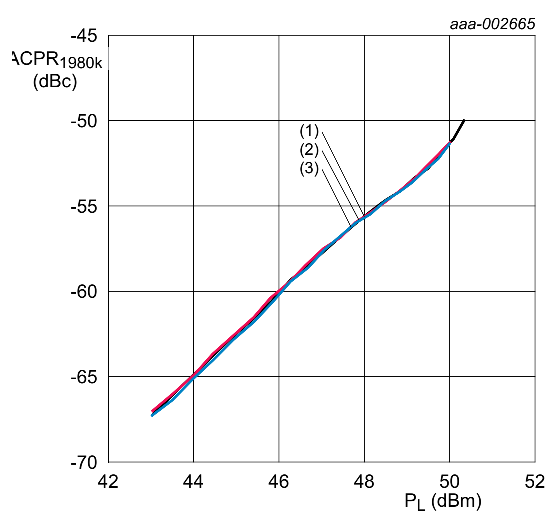

$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) f = 2300 MHz

(2) f = 2350 MHz

(3) f = 2400 MHz

**Fig 8. Adjacent channel power ratio (885 kHz) of IS-95 as a function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

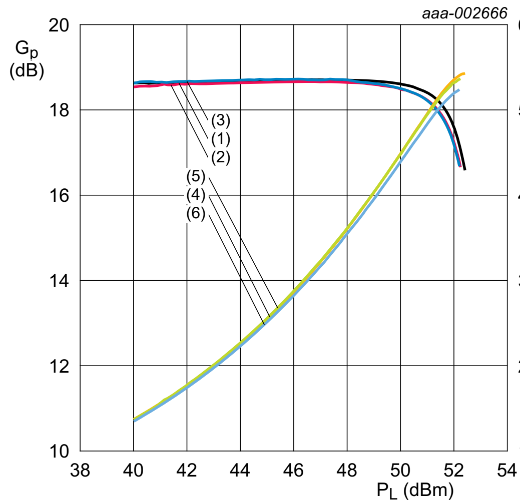
(1) f = 2300 MHz

(2) f = 2350 MHz

(3) f = 2400 MHz

**Fig 9. Adjacent channel power ratio (1980 kHz) of IS-95 as a function of output power; typical values**

### 7.3.3 CW




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) $G_p$ at f = 2300 MHz

(2) $G_p$ at f = 2350 MHz

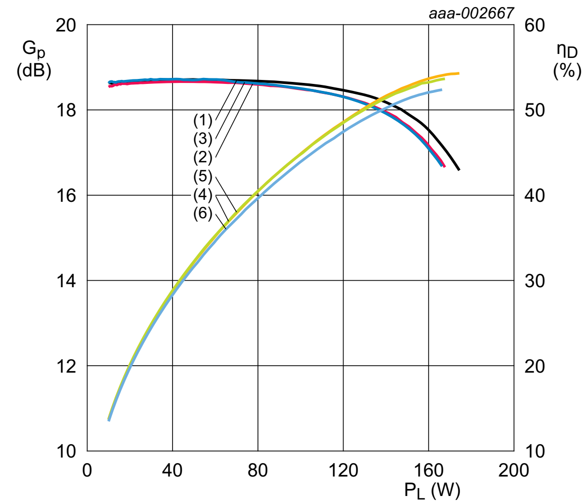
(3) $G_p$ at f = 2400 MHz

(4) $\eta_D$ at f = 2300 MHz

(5) $\eta_D$ at f = 2350 MHz

(6) $\eta_D$ at f = 2400 MHz

**Fig 10. Power gain and drain efficiency of CW as function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

(1) $G_p$ at f = 2300 MHz

(2) $G_p$ at f = 2350 MHz

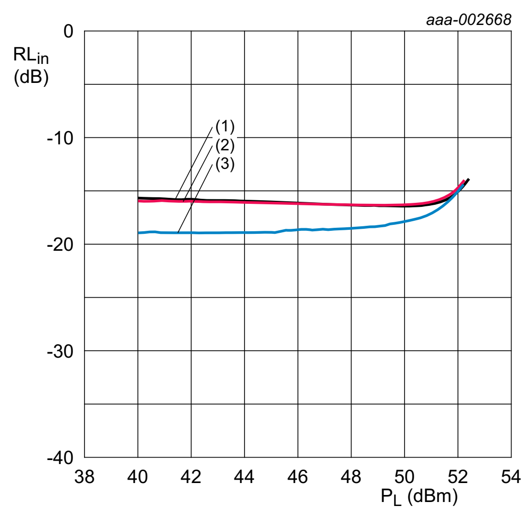
(3) $G_p$ at f = 2400 MHz

(4) $\eta_D$ at f = 2300 MHz

(5) $\eta_D$ at f = 2350 MHz

(6) $\eta_D$ at f = 2400 MHz

**Fig 11. Power gain and drain efficiency of CW as function of output power; typical values**




$V_{DS}$ = 28 V; $I_{Dq}$ = 1200 mA.

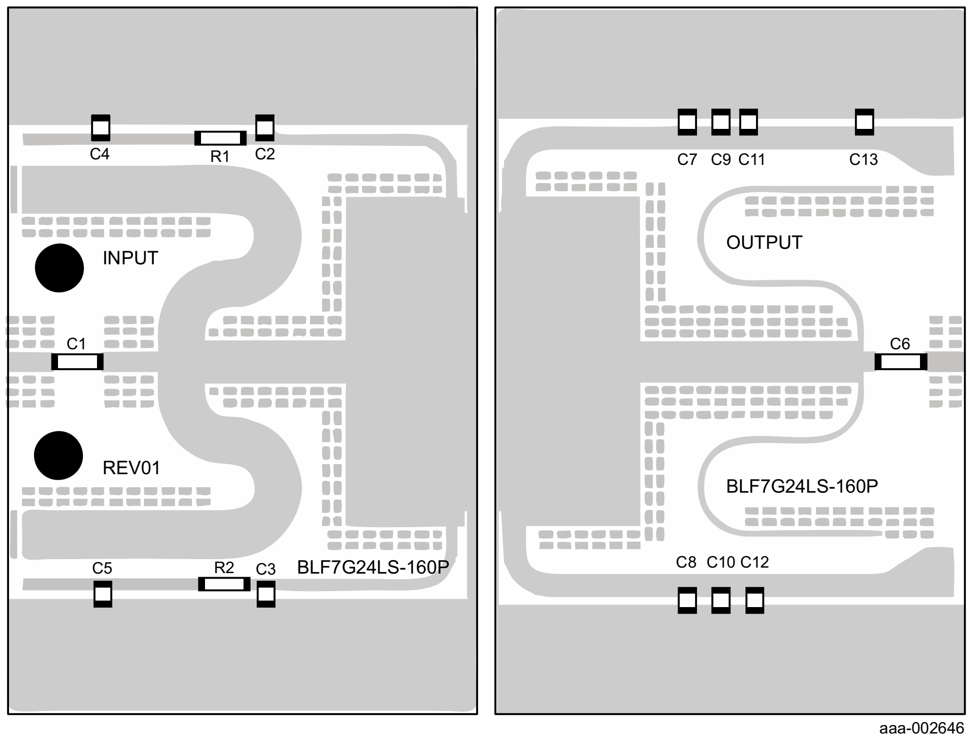
(1) f = 2300 MHz

(2) f = 2350 MHz

(3) f = 2400 MHz

**Fig 12. Input return loss of CW as a function of output power; typical values**

### 7.4 Test circuit




See Table 9 for a list of components.

**Fig 13. Component layout for test circuit**

**Table 9. List of components**

*For test circuit, see Figure 13.*

| Component | Description | Value | Remarks |
|---|---|---|---|
| C1, C6 | multilayer ceramic chip capacitor | 7.5 pF | [1] |
| C2, C3, C7, C8 | multilayer ceramic chip capacitor | 16 pF | [2] |
| C4, C5, C9, C10 | multilayer ceramic chip capacitor | 20 nF | [1] |
| C11, C12 | multilayer ceramic chip capacitor | 10 μF | [3] |
| C13 | electrolytic capacitor | 220 μF; 63 V | |
| R1, R2 | chip resistor | 2 Ω; SMD 805 | |

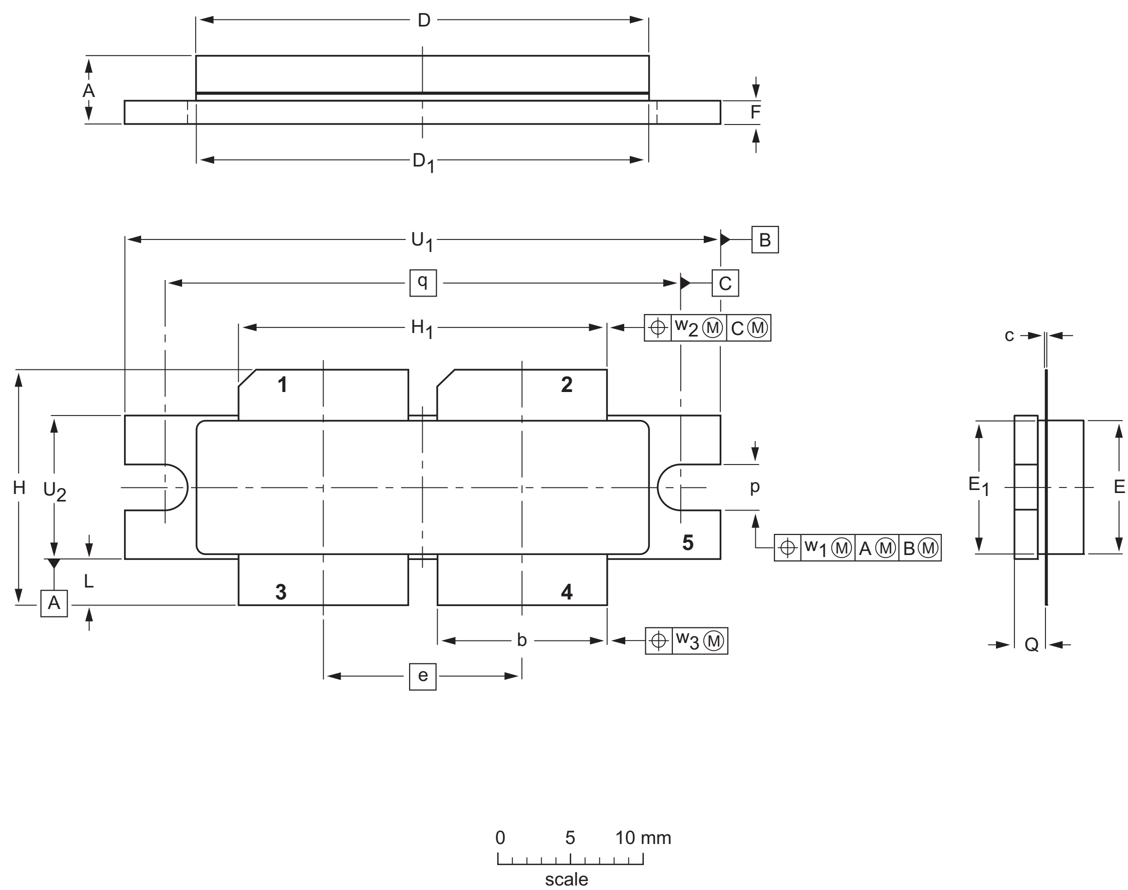
[1] American technical ceramics type 100B or capacitor of same quality.

[2] American technical ceramics type 100A or capacitor of same quality.

[3] TDK or capacitor of same quality.

## 8. Package outline

**Flanged balanced ceramic package; 2 mounting holes; 4 leads** **SOT539A**




**DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)**

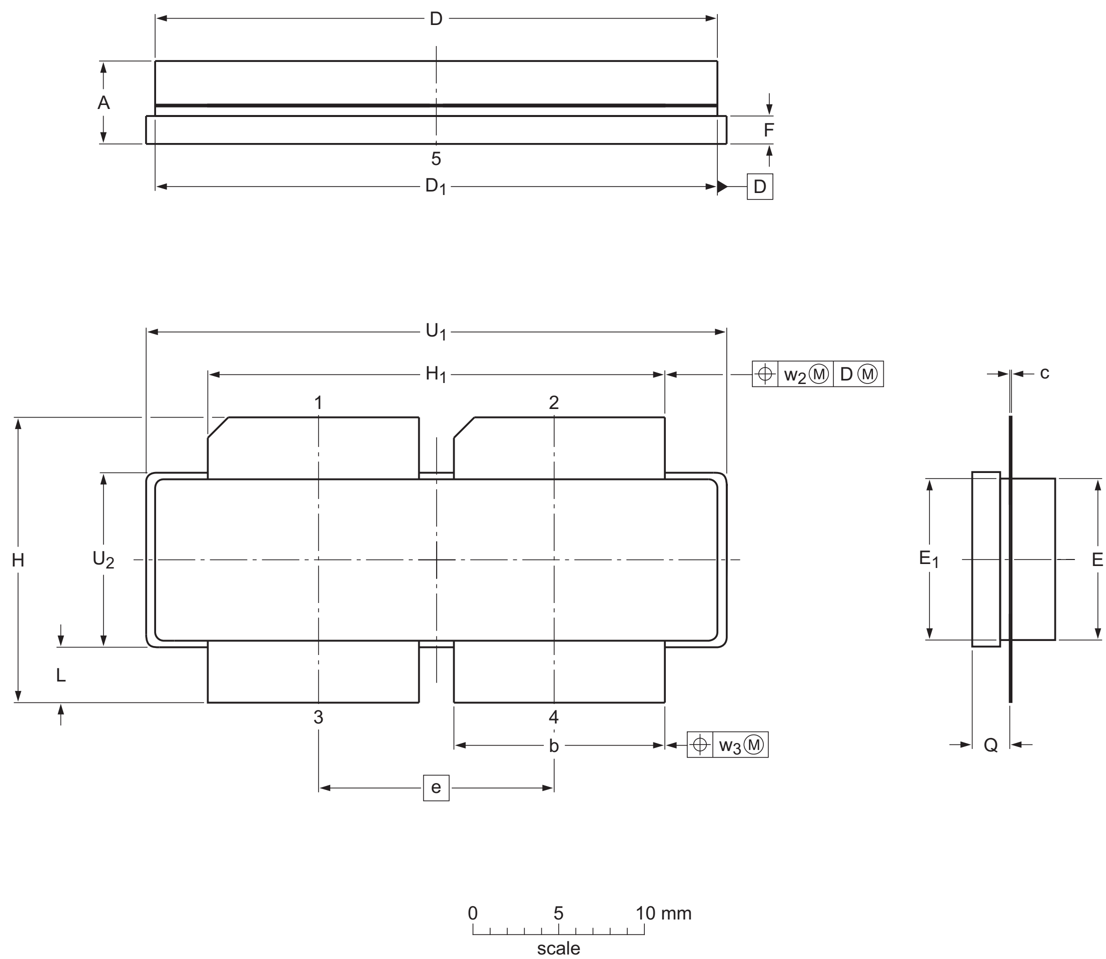
| UNIT | A | b | c | D | $D_1$ | e | E | $E_1$ | F | H | $H_1$ | L | p | Q | q | $U_1$ | $U_2$ | $w_1$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.7<br>4.2 | 11.81<br>11.56 | 0.18<br>0.10 | 31.55<br>30.94 | 31.52<br>30.96 | 13.72 | 9.50<br>9.30 | 9.53<br>9.27 | 1.75<br>1.50 | 17.12<br>16.10 | 25.53<br>25.27 | 3.48<br>2.97 | 3.30<br>3.05 | 2.26<br>2.01 | 35.56 | 41.28<br>41.02 | 10.29<br>10.03 | 0.25 | 0.51 | 0.25 |
| inches | 0.185<br>0.165 | 0.465<br>0.455 | 0.007<br>0.004 | 1.242<br>1.218 | 1.241<br>1.219 | 0.540 | 0.374<br>0.366 | 0.375<br>0.365 | 0.069<br>0.059 | 0.674<br>0.634 | 1.005<br>0.995 | 0.137<br>0.117 | 0.130<br>0.120 | 0.089<br>0.079 | 1.400 | 1.625<br>1.615 | 0.405<br>0.395 | 0.010 | 0.020 | 0.010 |

Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT539A | | | | | | ~~10-02-02~~<br>12-05-02 |

**Fig 14. Package outline SOT539A**

**Earless flanged balanced ceramic package; 4 leads** **SOT539B**




Dimensions

| Unit(1) | | A | b | c | D | $D_1$ | E | $E_1$ | e | F | H | $H_1$ | L | Q | $U_1$ | $U_2$ | $w_2$ | $w_3$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 4.7 | 11.81 | 0.18 | 31.55 | 31.52 | 9.5 | 9.53 | | 1.75 | 17.12 | 25.53 | 3.48 | 2.26 | 32.39 | 10.29 | | |
| | nom | | | | | | | | 13.72 | | | | | | | | 0.25 | 0.25 |
| | min | 4.2 | 11.56 | 0.10 | 30.94 | 30.96 | 9.3 | 9.27 | | 1.50 | 16.10 | 25.27 | 2.97 | 2.01 | 32.13 | 10.03 | | |
| inches | max | 0.185 | 0.465 | 0.007 | 1.242 | 1.241 | 0.374 | 0.375 | | 0.069 | 0.674 | 1.005 | 0.137 | 0.089 | 1.275 | 0.405 | | |
| | nom | | | | | | | | 0.54 | | | | | | | | 0.01 | 0.01 |
| | min | 0.165 | 0.455 | 0.004 | 1.218 | 1.219 | 0.366 | 0.365 | | 0.059 | 0.634 | 0.995 | 0.117 | 0.079 | 1.265 | 0.395 | | |

Note
1. millimeter dimensions are derived from the original inch dimensions.

*sot539b_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT539B | | | | | | ~~12-05-02~~<br>13-05-24 |

**Fig 15. Package outline SOT539B**

## 9. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| CCDF | Complementary Cumulative Distribution Function |
| IS-95 | Interim Standard 95 |
| ESD | ElectroStatic Discharge |
| LDMOS | Laterally Diffused Metal Oxide Semiconductor |
| PAR | Peak-to-Average Ratio |
| RF | Radio Frequency |
| VSWR | Voltage Standing Wave Ratio |

## 10. Revision history

**Table 11. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BLF7G24L-160P_7G24LS-160P#6 | 20150901 | Product data sheet | - | BLF7G24L-160P_7G24LS-160P v.5 |
| Modifications: | • The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| BLF7G24L-160P_7G24LS-160P v.5 | 20130712 | Product data sheet | - | BLF7G24L-160P_7G24LS-160P v.4 |
| BLF7G24L-160P_7G24LS-160P v.4 | 20120725 | Product data sheet | - | BLF7G24L-160P_7G24LS-160P v.3 |
| BLF7G24L-160P_7G24LS-160P v.3 | 20120420 | Preliminary data sheet | - | BLF7G24L-160P_7G24LS-160P v.2 |
| BLF7G24L-160P_7G24LS-160P v.2 | 20120301 | Objective data sheet | - | BLF7G24L-160P_7G24LS-160P v.1 |
| BLF7G24L-160P_7G24LS-160P v.1 | 20120210 | Objective data sheet | - | - |

# 11. Legal information

## 11.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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