BLF898; BLF898S

UHF power LDMOS transistor

Rev. 1 — 25 July 2017

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 900 W LDMOS RF power transistor for broadcast Doherty, class AB transmitter and ISM applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

Table 1. Application information

RF performance at V_{DS} = 50 V in a class AB broadband application demo.

Test signal	f	$P_{L(AV)}$	G_p	η_D	IMD_{shldr}	PAR
	(MHz)	(W)	(dB)	(%)	(dBc)	(dB)
DVB-T (8k OFDM)	800	180	20	32	–30	8 [1]
	590 to 690	180	18	33	–30	8 [1]

[1] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

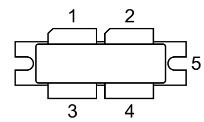
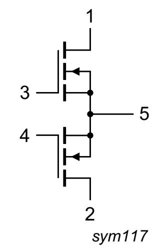
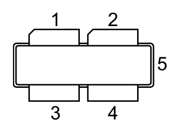
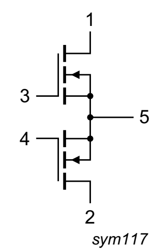
- Designed for symmetric and asymmetric Doherty operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Broadcast transmitter applications in the UHF band
- Digital broadcasting
- Industrial, Scientific and Medical applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF898 (SOT539A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF898S (SOT539B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF898	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF898S	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	120	V
V_{GS}	gate-source voltage		−6	+11	V
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 90 °C; V_{DS} = 50 V	0.12	K/W

6. Characteristics

Table 6. DC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 3.6 mA	124	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 360 mA	1.33	1.83	2.33	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	57	-	A
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 12.6 A	-	90	-	mΩ

Table 7. AC characteristics
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	315	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	105	-	pF
C_{rss}	reverse transfer capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	1.5	-	pF

Table 8. RF characteristics
RF characteristics in Ampleon production test circuit, T_{case} = 25 °C; unless otherwise specified.

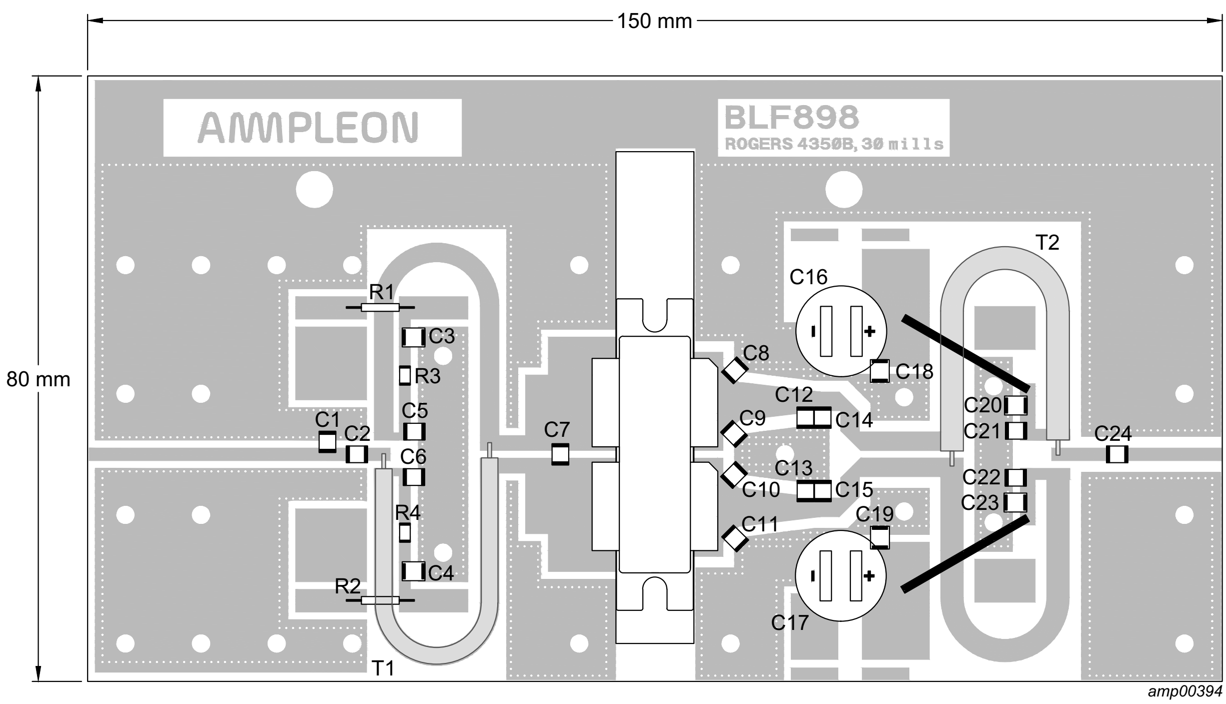
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DVB-T (8k OFDM), class-AB						
V_{DS}	drain-source voltage		-	50	-	V
I_{Dq}	quiescent drain current	per section	-	900	-	mA
$P_{L(AV)}$	average output power	f = 800 MHz	-	180	-	W
G_p	power gain	f = 800 MHz	19	20	-	dB
η_D	drain efficiency	f = 800 MHz	29	32	-	%
IMD_{shldr}	intermodulation distortion shoulder	f = 800 MHz	-	–30	–27	dBc
PAR	peak-to-average ratio	f = 800 MHz	-	8.0	-	dB

7. Test information

7.1 Ruggedness in Doherty operation

The BLF898 and BLF898S are capable of withstanding a load mismatch corresponding to VSWR ≥ 40 : 1 through all phases under the following conditions: V_{DS} = 50 V; f = 800 MHz at rated load power.

7.2 Test circuit



Printed-Circuit Board (PCB): Rogers 4350B: ε_r = 3.66 F/m, height = 0.762 mm; Cu (top/bottom metalization); thickness copper plating = 35 µm. See Table 9 for a list of components.

Fig 1. Component layout for production RF test circuit

Table 9. List of components

See Figure 1 for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	1.8 pF	ATC 100B
C2	multilayer ceramic chip capacitor	100 pF	ATC 100B
C3, C4	multilayer ceramic chip capacitor	4.7 µF, 50 V	TDK
C5, C6	multilayer ceramic chip capacitor	100 pF	ATC 100B
C7	multilayer ceramic chip capacitor	15 pF	ATC 100B
C8, C9, C10, C11	multilayer ceramic chip capacitor	20 pF	ATC 800B
C12, C13	multilayer ceramic chip capacitor	7.5 pF	ATC 800B
C14, C15	multilayer ceramic chip capacitor	6.2 pF	ATC 800B

Table 9. List of components *...continued*

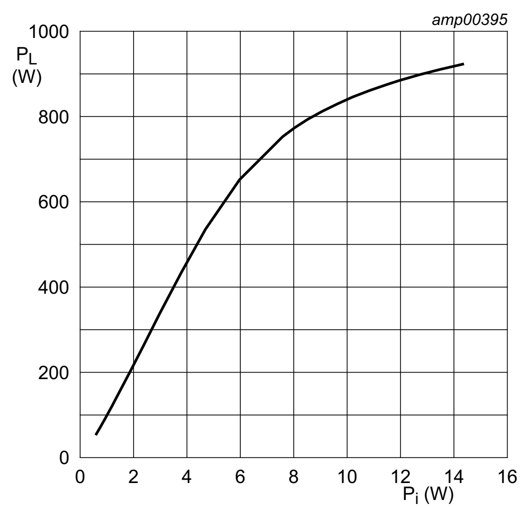
See Figure 1 for component layout.

Component	Description	Value	Remarks
C16, C17	electrolytic capacitor	470 μF, 63 V	
C18, C19	multilayer ceramic chip capacitor	4.7 μF, 63 V	TDK: C5750X7R2A475KT/A
C20, C23	multilayer ceramic chip capacitor	4.7 μF	Murata: GRM42-256X7S475K100H530
C21, C22	multilayer ceramic chip capacitor	200 pF	ATC 800B
C24	multilayer ceramic chip capacitor	220 pF	ATC 800B
R1, R2	wire resistor	100 Ω	
R3, R4	chip resistor	5.6 Ω	
T1	coaxial balun	L = 58 mm, 25 Ω	EZ 90-25
T2	coaxial balun	L = 58 mm, 50 Ω	EZ 141-CU-TP

7.3 Graphical data

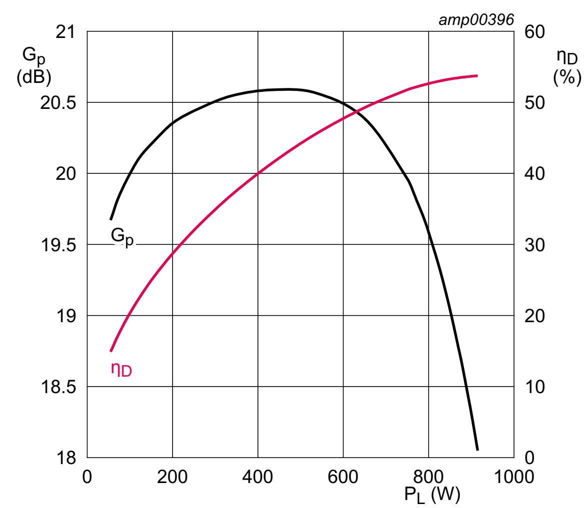
The following figures are measured in a narrowband RF production circuit.

7.3.1 Pulsed CW



V_{DS} = 50 V; I_{Dq} = 2 x 900 mA; t_p = 100 μs; δ = 10 %.

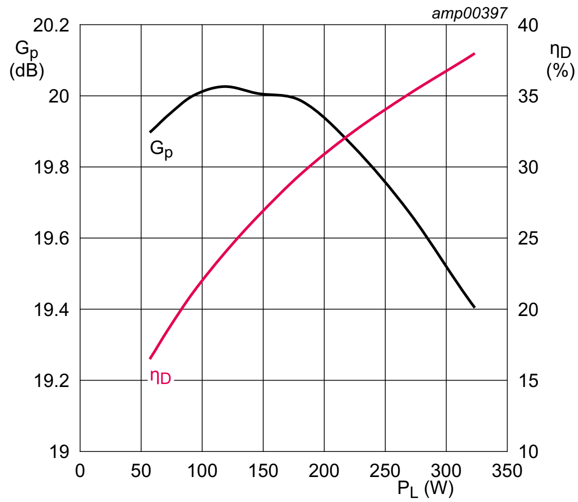
Fig 2. Output power as a function of input power; typical values



V_{DS} = 50 V; I_{Dq} = 2 x 900 mA; t_p = 100 μs; δ = 10 %.

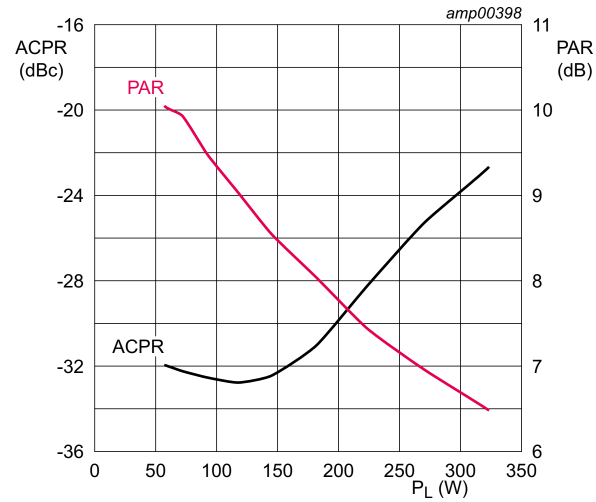
Fig 3. Power gain and drain efficiency as function of output power; typical values

7.3.2 DVB-T



V_{DS} = 50 V; I_{Dq} = 2 x 900 mA; PAR (of output signal) at 0.01 % probability on CDDF; PAR of input signal = 9.5 dB at 0.01 % probability on CDDF.

Fig 4. Power gain and drain efficiency as function of output power; typical values

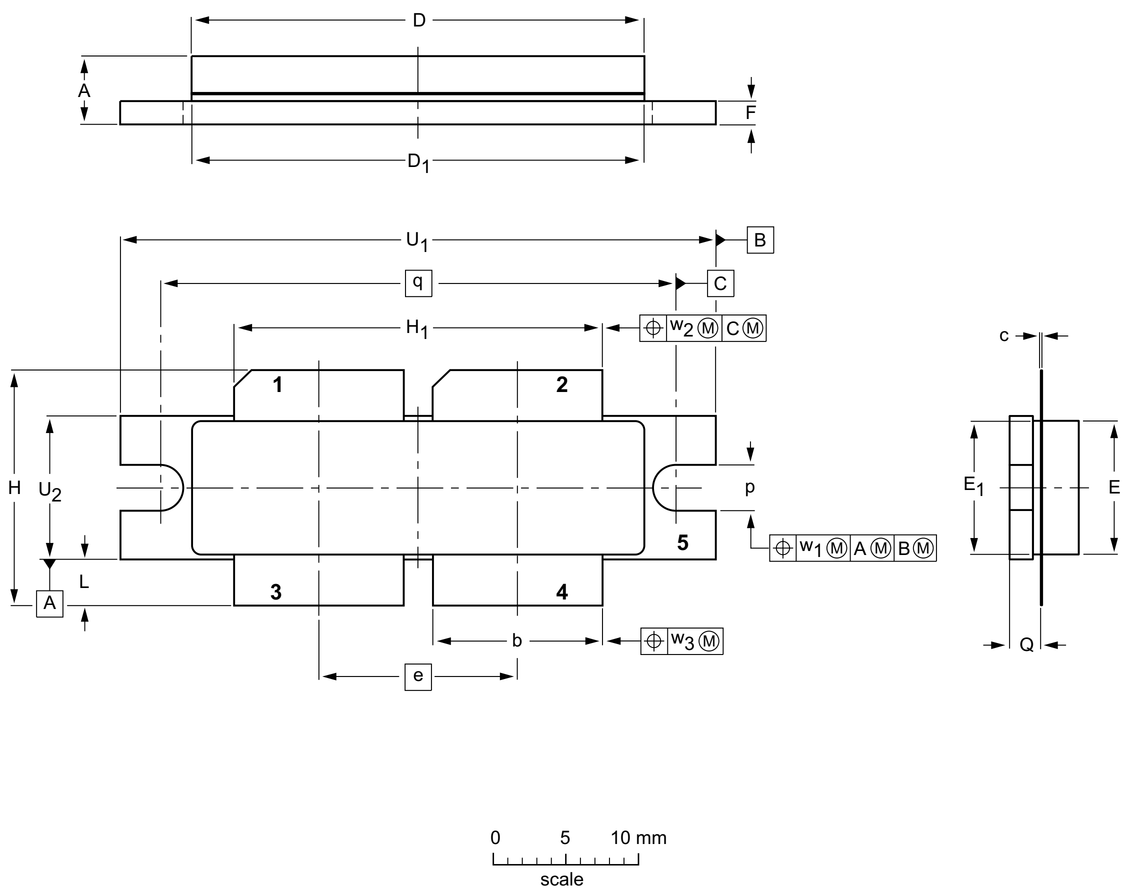


V_{DS} = 50 V; I_{Dq} = 2 x 900 mA; PAR (of output signal) at 0.01 % probability on CDDF; PAR of input signal = 9.5 dB at 0.01 % probability on CDDF.

Fig 5. Adjacent channel power ratio and peak-to-average ratio as function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

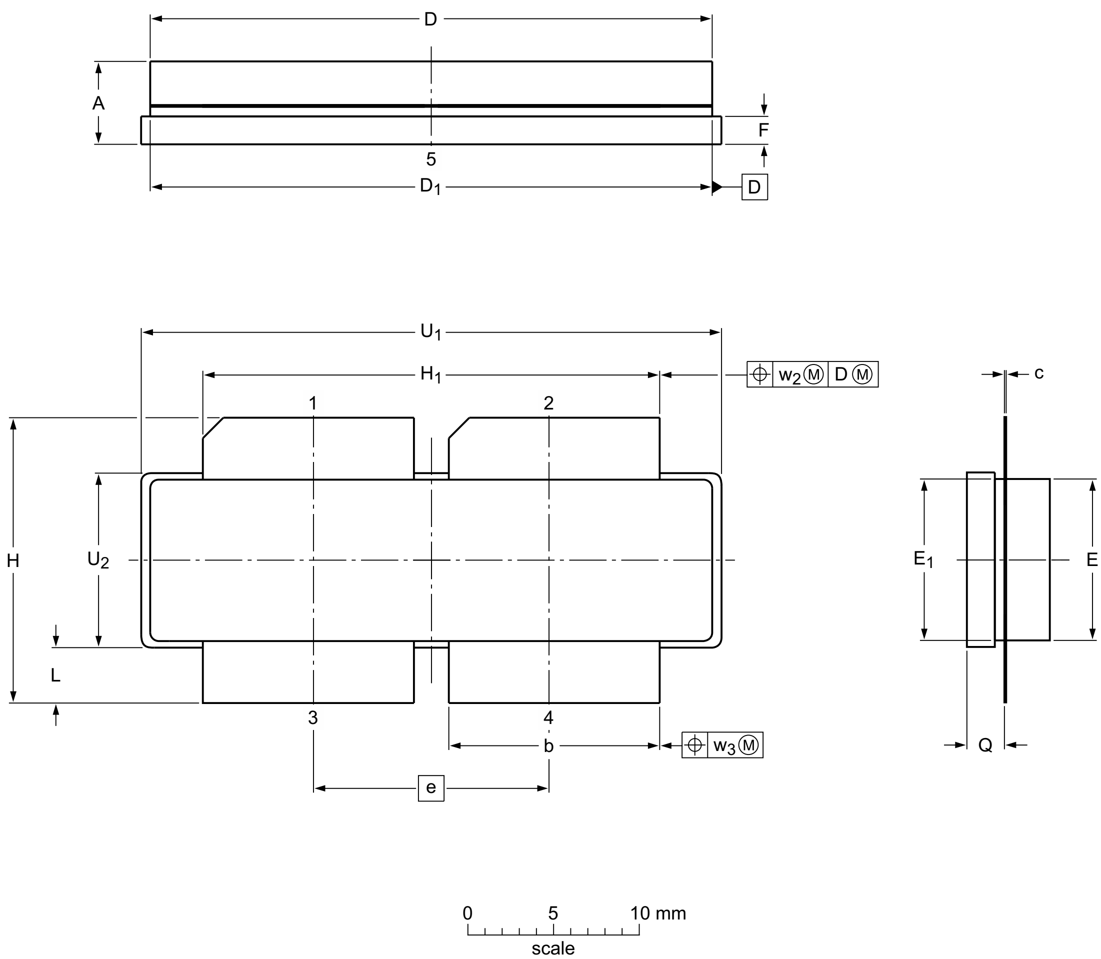
Note

1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						~~10-02-02~~ 12-05-02

Fig 6. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads **SOT539B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

Note

1. millimeter dimensions are derived from the original inch dimensions.

sot539b_po

Outline version	References: IEC	JEDEC	JEITA		European projection	Issue date
SOT539B						~~12-05-02~~ 13-05-24

Fig 7. Package outline SOT539B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
UHF	Ultra High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF898_BLF898S v.1	20170725	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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